PM5316

SPECTRA™ 4x155

SONET/SDH Payload Extractor/Aligner 4 x 155 Mbit/s

Data Sheet

Released

Issue No. 5: September 2002

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U.S. Patent No. 5,959,490; 6,246,738. Canadian Patent No. 2,254,285; 2,245,757

Other relevant patent grants may also exist.

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Revision History

Issue No.	Issue Date	Details of Change
Issue 5	September 2002	Update pin diagram to include reserved[1:5] and correct pin descriptions Add Reserved5, VBIAS[1:0], QAVD[2:1], QAVS[2:1] to pin description Add granted patents Replace all references to DISDV1 with ENDV1 Clarify apparent contradiction of IR drop across series resistors in power supply filtering diagram Add RTAL/TTAL FIFO initialization procedure to Section 13.1 Correct Figure 2 to show only 8-bit TelecomBus mode Correct typographical error: change RPOHCLK nominal frequency from 12.92MHz to 12.96MHz Removed references to TPOH.
Issue 4	Mar 2001	De-documented all Transport Path Overhead port (TPOH) functionality Added Overhead byte processing information in operation section.
Issue 3	Jan 2001	Removed TIU2E and TIU2I register bits from registers 1n2Dh and 1n31h respectively. DOPJ[1:0] register bit in the TTAL block (register 1nD1h) has been removed. DOPJ[1:0] register bit in the RTAL block (register 1n59h) has been redefined. PRBS monitoring mode needs two bits to be programmed. Mode setting in both the DPGM (register 1n7Ah) and APGM (register 1nFAh) is now defined via two mode bits MON_GMODE[1:0]. RSOP Section B1 error counters (0m16h and Om17h registers) may also be transferred upon a write to either register. Master test register bit 3 to 7 is defined as R/W instead of just W. Pin out diagram has changed format to improve readability but the pinout remains the SAME. Due to clear on write auxiliary interrupts, tZint timing is specified for microprocessor writes to clear device interrupt pin. Analog supplies AVD/AVS are specified at 5% instead of 10%. Consistent naming or STM1-CONCAT to STM1_CONCAT (underscore) register bit in registers 1n00h and 1n80h. Power supply board recommendations have been changed in section 13.8. Separate supplies are no longer recommended. Specific PECL input currents are given in section 17, D.C. Characteristics. RAD does not contain transmitted K1/K2 bytes under generation of AIS-L on the transmit stream. TAD port is limited to accumulating a maximum of 15 REI
Issue 2	Sept 2000	Additional feature explanations/ clarifications Timing Change on drop interface in 19.44 Mhz mode Addition of register bits CONCAT, TPOH_DIS, ATSI_FORCE and ATSI_RESET Definition changes of LOPCONRALM and PAISCONRALM.

Issue No.	Issue Date	Details of Change
		Added Section describing loopbacks DC Characteristics up to date and complete Added RTC_EN register bit.
Issue 1	June 2000	Preliminary release of datasheet

Table of Contents

List of Registers

List of Figures

List of Tables

1 Features

1.1 General

- Monolithic four channel SONET/SDH Payload Extractor/Aligner for use in STS-3 (STM-1/AU-3) or STS-3c (STM-1/AU-4) interface applications, operating at serial interface speeds of 155.52 Mbit/s.
- Provides integrated clock recovery and clock synthesis for direct interfacing with optical modules.
- On each channel, provides termination for SONET section and line, SDH Regenerator Section and Multiplexer Section transport overhead, and path overhead of three STS-1 (STM-0/AU-3) paths or a single STS-3c (STM-1/AU-4) path.
- On each channel, maps three STS-1 (STM-0/AU-3) payloads or a single STS-3c (STM-1/AU-4) payload to the system timing reference, accommodating plesiochronous timing offsets between the references through pointer processing.
- Provides Time Slot Interchange (TSI) function at the Telecom Add and Drop buses for grooming 12 STS-1 (STM-0/AU-3) paths.
- On each channel, provides clear-channel mapping of three 49.536 Mbit/s or 48.384 Mbit/s arbitrary data streams into an STS-3 (STM-1/AU-3) frame. Provides clear-channel mapping of a single 149.76 Mbit/s arbitrary data stream into an STS-3c (STM-1/AU-4) frame.
- Supports line loop back from the line side receive stream to the transmit stream and diagnostic loop back from a Telecom Add bus interface to a Telecom Drop bus interface.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 3.3 V CMOS with TTL compatible digital inputs and CMOS/TTL digital outputs. PECL inputs and outputs are 3.3 V and 5 V compatible.
- Industrial temperature range (-40 °C to +85 °C).
- 520 pin Super BGA package.
- Complies with Telcordia GR-253-CORE (1995) jitter tolerance, jitter transfer and intrinsic jitter criteria.

1.2 SONET Section and Line/SDH Regenerator and Multiplexer Section

- Frames to the STS-3/3c (STM-1/AU-3/AU-4) receive stream and inserts the framing bytes (A1, A2) and the STS identification byte (J0) into the transmit stream; descrambles the receive stream and scrambles the transmit stream.

- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream and calculates and inserts B1 and B2 in the transmit stream; accumulates near end errors (B1, B2) and far end errors (M1) and inserts line remote error indications (REI) into the Z2 (M1) growth byte based on received B2 errors.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.
- Extracts and serializes the order wire channels (E1, E2), the data communication channels (D1-D3, D4-D12) and the section user channel (F1) from the receive stream, and inserts the corresponding signals into the transmit stream.
- Extracts and serializes the automatic protection switch (APS) channel (K1, K2) bytes, filtering and extracting them into internal registers for the receive stream. Inserts the APS channel into the transmit stream.
- Extracts and filters the synchronization status message (Z1/S1) byte into an internal register for the receive stream. Inserts the synchronization status message (Z1/S1) byte into the transmit stream.
- Extracts a 64-byte or 16-byte section trace (J0) message using an internal register bank for the receive stream. Detects an unstable section trace message or mismatch with an expected message, and optionally inserts Line and Path AIS on the system Drop side upon either of these conditions. Inserts a 64-byte or 16-byte section trace (J0) message using an internal register bank for the transmit stream.
- Detects loss of signal (LOS), out-of-frame (OOF), loss-of-frame (LOF), line remote defect indication (RDI), line alarm indication signal (LAIS), and protection switching byte failure alarms on the receive stream. Optionally returns line RDI in the transmit stream.
- Provides a transmit and receive ring control port, allowing alarm and maintenance signal control and status to be passed between mate SPECTRA-155s for ring-based Add/Drop multiplexer and line multiplexer applications.
- Configurable to force Line AIS in the transmit stream.

1.3 SONET Path / SDH High Order Path

- Accepts a multiplex of three STS-1 (STM-0/AU-3) streams or a single STS-3c (STM-1/AU-4) stream, interprets the STS (AU) pointer bytes (H1, H2, and H3), extracts the synchronous payload envelope(s) and processes the path overhead for the receive stream.
- Constructs a byte serial multiplex of three STS-1 (STM-0/AU-3) streams or an STS-3c (STM-1/AU-4) stream on the transmit side.
- Detects loss of pointer (LOP), loss of tributary multi-frame (LOM), path alarm indication signal (PAIS) and path (auxiliary and enhanced) remote defect indication (RDI) for the receive stream. Optionally inserts PAIS, path RDI in the transmit stream.

- Extracts and serializes the entire path overhead from the three STS-1 (STM-0/AU-3) or the single STS-3c (STM-1/AU-4) receive streams. Inserts the path overhead bytes in the three STS-1 (STM-0/AU-3) or single STS-3c (STM-1/AU-4) stream for the transmit stream. The path overhead bytes may be sourced automatically or from internal registers. Path overhead insertion may also be disabled.
- Extracts the received path signal label (C2) byte into an internal register and detects for path signal label unstable and for signal label mismatch with the expected signal label that is downloaded by the microprocessor. Inserts the path signal label (C2) byte from an internal register for the transmit stream.
- Extracts a 64-byte or 16-byte path trace (J1) message using an internal register bank for the receive stream. Detects an unstable path trace message or mismatch with an expected message, and inserts Path RAI upon either of these conditions. Inserts a 64-byte or 16-byte path trace (J1) message using an internal register bank for the transmit stream.
- Detects received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.
- Counts received path REIs for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) basis on bit or block BIP-8 errors detected in the receive path. Reporting of BIP-8 errors is on a bit or block bases independent of the accumulation of BIP-8 errors.
- Maintains the existing tributary multi-frame sequence on the H4 byte until a new phase alignment has been verified.
- Provides a serial alarm port communication of path REI and path RDI alarms to the transmit stream of a mate SPECTRA 4x155 in the returning direction.
- Maintains the existing tributary multi-frame sequence on the H4 byte until a new phase alignment has been verified.

1.4 System Side Interfaces

- Supports TelecomBus interfaces by indicating/accepting the location of the STS identification byte (C1), optionally the path trace byte(s) (J1), optionally the first tributary overhead byte(s) (V1), and all synchronous payload envelope (SPE) bytes in the byte serial stream.
- Configurable to support four 19.44 MHz byte TelecomBus interfaces or a single 77.76 MHz byte TelecomBus interface.
- For TelecomBus interface, accommodates phase and frequency differences between the receive/transmit streams and the Add/Drop buses via pointer adjustments.
- Provides TSI function to interchange or groom 12 STS-1 (STM-0/AU-3) paths or four STS-3/3c (STM-1/AU-3/AU-4) paths at the Telecom Add/Drop buses.

2 Applications

- SONET/SDH Add Drop Multiplexers
- SONET/SDH Terminal Multiplexers
- SONET/SDH Line Multiplexers
- SONET/SDH Cross Connects
- SONET/SDH Test Equipment
- Switches and Hubs
- Routers

3 References

1. American National Standard for Telecommunications - Digital Hierarchy - Optical Interface Rates and Formats Specification, ANSI T1.105-1991.

2. American National Standard for Telecommunications - Layer 1 In-Service Digital Transmission Performance Monitoring, T1X1.3/93-005R1, April 1993.

3. Committee T1 Contribution, "Draft of T1.105 - SONET Rates and Formats", T1X1.5/94-033R2-1994.

4. Telcordia - GR-253-CORE "SONET Transport Systems: Common Generic Criteria", Issue 2 Revision 1, January 1995.

5. Telcordia - GR-436-CORE "Digital Network Synchronization Plan", Issue 1 Revision 1, June 1996.

6. ETS 300 417-1-1, "Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) Equipment", January 1996.

7. ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.

8. ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipment - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 Kbit/s Hierarchical Levels", July 1995.

9. ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 1996.

10. ITU Recommendation G.781, - "Structure of Recommendations on Equipment for the Synchronous Digital Hierarchy (SDH)", January 1994.

11. ITU Recommendation G.783, "Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks", 28 October 1996.

12. ITU Recommendation O.151, "Error Performance measuring Equipment Operating at the Primary Rate and Above", October, 1992.

13. ITU Recommendation I.432, "ISDN User Network Interfaces", March 93.

4 Document Conventions & Definitions

The following conventions are used along this document:

SIGNAL1-4: designated equivalent signals, either input our output. Each of these signals applies to the corresponding device channel.

SIGNAL±: designate a differential signal.

SIGNAL[N:0]: designate a bus of N+1 bit wide, bit N being the MSB, bit 0 the LSB.

The following table defines the abbreviations used in this document:

APGM	Add Bus PRBS Generator/Monitor
BIP	Bit Interleaved Parity
CRSI	CRU and SIPO
CRU	Clock Recovery Unit
CSPI	CSU and PISO
CSU	Clock Synthesis Unit
DPGM	Drop Bus PRBS Generator/Monitor
LAIS	Line Alarm Indication Signal
LOF	Loss of Frame
LOM	Loss of Tributary Multi-frame
LOP	Loss of Pointer
LOS	Loss of Signal
MSB	Most Significant Bit
OOF	Out-Of-Frame
OOM	Out-Of-Multi-frame State
PAIS	Path Alarm Indication Signal
PDLE	Parallel Diagnostic Loop
PLL	Phase Locked Loop
PISO	Parallel to Serial Converter
PRBS	Pseudo Random Bit/Byte Sequence
RASE	Receive APS, Synchronization Extractor and Bit Error Monitor
RDI	Remote Defect Indication
REI	Remote Error Indication
RLOP	Receive Line Overhead Processor
RTOC	Receive Transport Overhead Controller
RPOP	Receive Path Overhead Processor
RSOP	Receive Section Overhead Processor
RTAL	Receive Telecom Aligner
SD	Signal Degrade
SF	Signal Fail

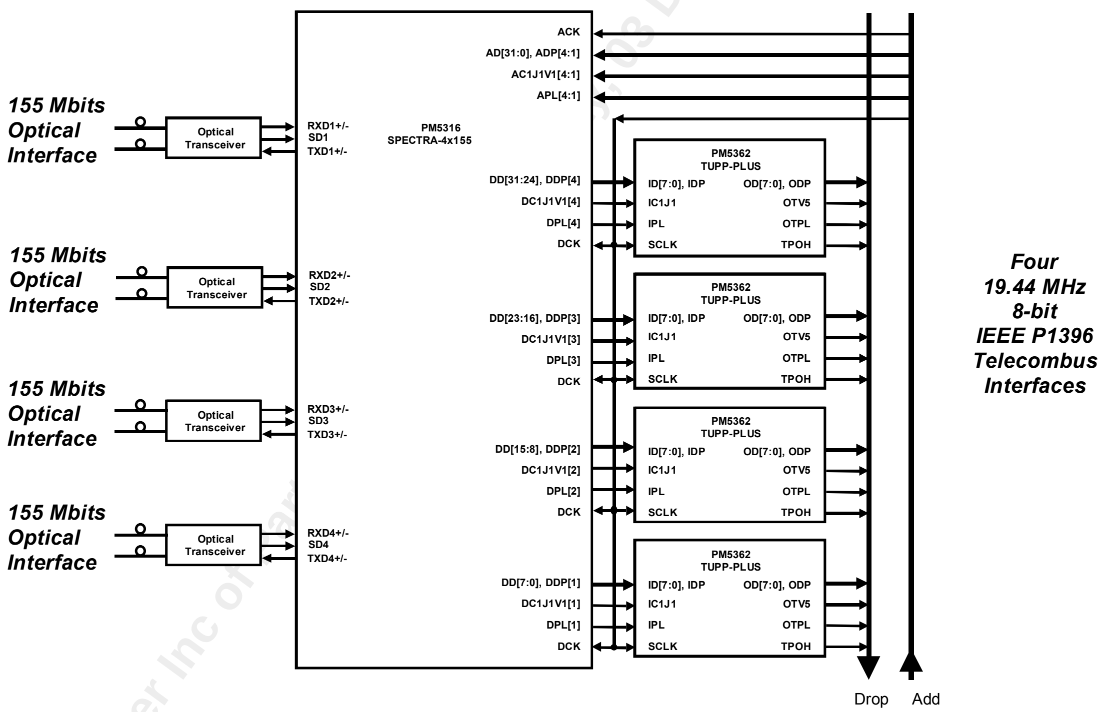
SDLE	Serial Diagnostic Loop back
SIPO	Serial-to-parallel Converter
SLLB	System Side Line Loop back
SPE	Synchronized Payload Envelope
SPTB	SONET/SDH Path Trace Buffer
SSTB	SONET/SDH Section Trace Buffer
TAP	Test Access Port
TLOP	Transmit Line Overhead Processor
TPOP	Transmit Path Overhead Processor
TPPS	Transmit Path Processing Slice
TPIP	Transmit Pointer Interpreter
TSI	Timeslot Interchange
TSOP	Transmit Section Overhead Processor
TTAL	Transmit Telecom Aligner
TTOC	Transmit Transport Overhead Controller
WANS	Wide Area Network Synchronization Controller

5 Application Examples

The PM5316 SPECTRA™ 4x155 device is designed for use in various SONET/SDH network elements including switches, terminal multiplexers, and Add/Drop multiplexers. In these applications, the line interface of the SPECTRA 4x155 typically interfaces directly with the electrical optical modules and the system side interface connects directly with a TelecomBus.

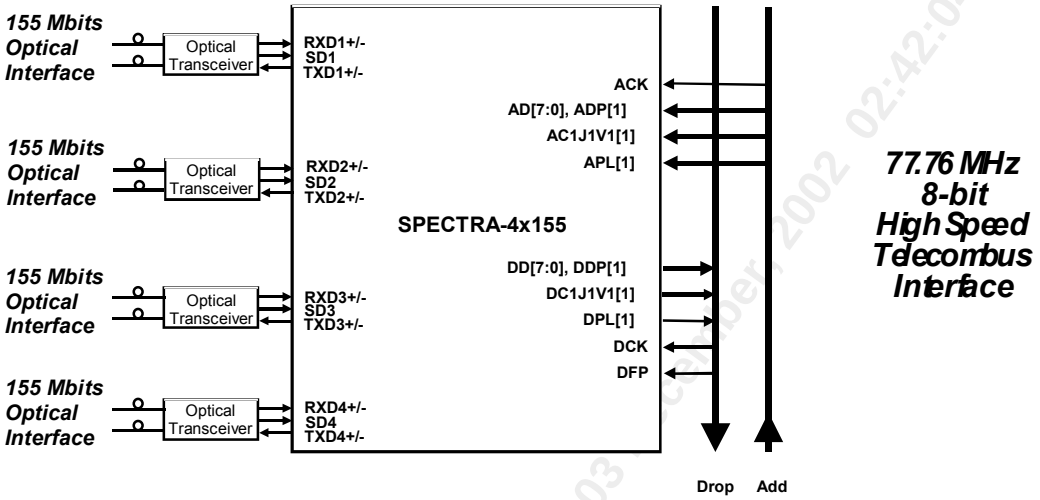
Figure 1 shows how the SPECTRA 4x155 is used to implement four 155 Mbit/s aggregate interfaces. In this application, the SPECTRA 4x155 performs SONET/SDH section, line, and path termination and the PM5362 TUPP™ PLUS performs tributary pointer processing and performance monitoring.

Figure 1 STS-3 (STM-0/AU-3) or STS-3c (STM-1/AU-4) Application with 19.44 MHz Byte TelecomBus Interface



The system side interface of the SPECTRA 4x155 can be configured to have a 77.76 MHz byte TelecomBus interface. Figure 2 shows how the SPECTRA 4x155 is used to implement a 622 Mbit/s aggregate interface using the high-speed TelecomBus on the system side interface. In this application, the SPECTRA 4x155 performs SONET/SDH section, line, and path termination.

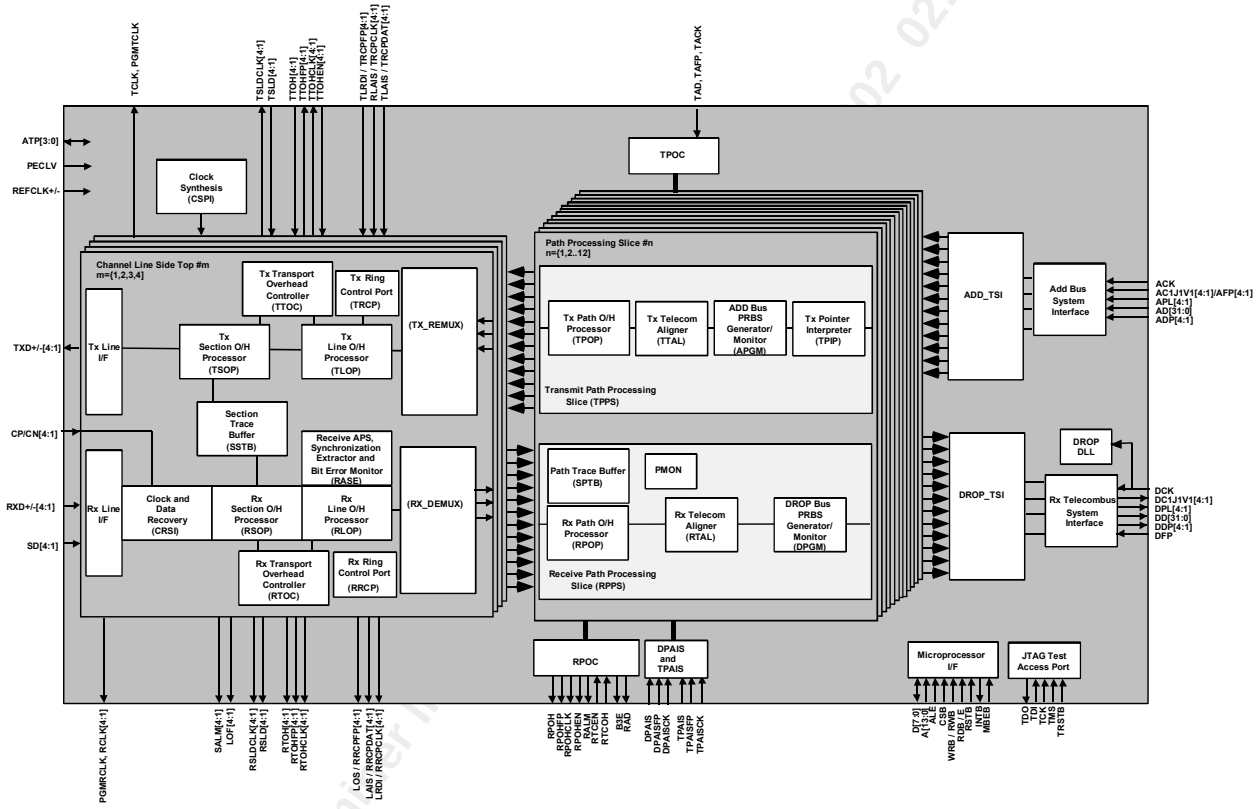
Figure 2 STS-3 (STM-1/AU-3) or STS-3c (STM-1/AU-4) Application with 77.76 MHz Byte TelecomBus Interface



The SPECTRA 4x155 can also be used to implement OC-3 interfaces on channelized high-speed IP switches and routers.

6 Block Diagram

Figure 3 Block Diagram



7 Functional Description

The PM5316 SPECTRA 4X155 SONET/SDH Payload Extractor/Aligner terminates the transport and path overhead of four STS-3 (STM-1/AU-3) and STS-3c (STM-1/AU-4) streams at 155 Mbit/s. The device implements significant receive and transmit functions for a SONET/SDH-compliant line interface.

In the receive direction, the SPECTRA 4x155 receives SONET/SDH frames via bit serial interfaces, recovers clock and data, and terminates the SONET/SDH section (regenerator section), line (multiplexer section), and path. The device performs framing (A1, A2), descrambling, alarm detection, and section and line bit interleaved parity (BIP) (B1, B2) monitoring, accumulating error counts at each level for performance monitoring purposes. The B2 errors are monitored to detect signal fail and degrade threshold-crossing alarms. As part of this process, the device accumulates line REIs (M1) and may buffer and compare the 16 or 64-byte section trace (J0) message against the expected message.

The device also interprets the received payload pointers (H1, H2), detects path alarm conditions, and detects and accumulates path BIPs (B3). The path REIs are monitored and accumulated. Also, the 16 or 64-byte path trace (J1) message is accumulated and compared against the expected result. The device then extracts the SPE (VC). All transport and path overhead bytes are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The extracted SPE (VC) is placed on a Telecom Drop bus. Frequency offsets, for example, due to plesiochronous network boundaries, or the loss of a primary reference timing source, and phase differences, due to normal network operation, between the received data stream and the Drop bus are accommodated by pointer adjustments in the Drop bus.

In the transmit direction, the SPECTRA 4x155 transmits SONET/SDH frames, via bit serial interfaces, and formats section (regenerator section), line (multiplexer section), and path overhead appropriately. The device provides transmit path origination for a SONET/SDH STS-3 (STM-1/AU-3) or STS-3c (STM-1/AU-4) stream. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section and line BIPs (B1, B2) as required to allow performance monitoring at the far end. Line REIs (M1) and a 16 or 64-byte section trace (J0) message may be optionally inserted. The device also generates the transmit payload pointers (H1, H2) and creates and inserts the path BIP. A 16 or 64-byte path trace (J1) message and the path status byte (G1) is optionally inserted.

In Addition to its basic processing of the transmit SONET/SDH overhead, the SPECTRA 4x155 provides convenient access to all overhead bytes, which are inserted serially on lower rate interfaces, allowing additional external sourcing of overhead, if desired. The SPECTRA 4x155 also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors and BIP errors, which are useful for system diagnostics and tester applications.

The inserted SPE (VC) is sourced from a TelecomBus Add stream. The SPECTRA 4x155 maps the SPE (VC) from a Telecom Add bus into the transmit stream. As with the TelecomBus Drop stream, frequency offsets and phase differences between the transmit data stream and the Add bus are accommodated by pointer adjustments in the transmit stream.

The SPECTRA 4x155 supports Time-Slot Interchange (TSI) on the Telecom Add and Drop buses. On the Drop side, the TSI views the receive stream as 12 independent time-division multiplexed columns of data (12 constituent STS-1 (STM-0/AU-3) or equivalent streams or time-slots or columns). Any column can be connected to any time-slot on the Drop bus, independently of the channel they originate from. Both column swapping and broadcast are supported. TSI is independent of the underlying payload mapping formats. Similarly, on the Add side, data from the Add bus is treated as 12 independent time-division multiplexed columns. Assignment of data columns to transmit time-slots (STS-1 (STM-0/AU-3) or equivalent streams) is arbitrary.

The transmitter and receiver are independently configurable to allow for asymmetric interfaces. Ring control ports are provide to pass control and status information between mate transceivers.

The SPECTRA 4x155 is configured, controlled and monitored via a generic 8-bit microprocessor bus interface.

The SPECTRA 4x155 is implemented in low power, +3.3 Volt, CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 520-pin SBGA package.

8 Pin Diagrams

The SPECTRA 4x155 is available in a 520-pin SBGA package having a body size of 40 mm by 40 mm and a ball pitch of 1.27 mm.

Figure 4 Pin Diagram of SPECTRA 4x155 (Bottom Top right going clockwise)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A	VDD	GND	GND	GND	RPOHCLK	GND	RESERVED3	TAD	N/C	LOF3	GND	D[4]	INTB	A[9]	A[4]	GND
B	GND	VDD	GND	DPAISFP	TPAISFP	RPOHEN	RESERVED5	TAFP	N/C	LOF2	RALM	D[5]	D[0]	A[10]	A[5]	GND
C	GND	GND	VDD	VDD	DPAIS	RPOHFP	RESERVED2	RTCOH	N/C	LOF1	B3E	D[6]	D[1]	A[12]	A[6]	VDD
D	GND	N/C	VDD	VDD	DPAISCK	TPAIS	RESERVED1	RTCEN	RAD	N/C	LOF4	D[7]	D[2]	A[11]	A[7]	VDD
E	ACK	APL[1]	AC1J1V1/AFP[1]	AD[0]	VDD	TPAISCK	RPOH	RESERVED4	TACK	N/C	VDD	VBIAS[1]	D[3]	A[13]	A[8]	VDD
F	GND	AD[1]	AD[2]	AD[3]	AD[4]											
G	AD[5]	AD[6]	AD[7]	ADP[1]	N/C											
H	DPL[1]	DC1J1V1[1]	DD[0]	DD[1]	DD[2]											
J	DD[3]	DD[4]	DD[5]	DD[6]	DD[7]											
K	DDP[1]	APL[2]	AC1J1V1/AFP[2]	AD[8]	AD[9]											
L	GND	AD[10]	AD[11]	AD[12]	VDD											
M	AD[13]	AD[14]	AD[15]	ADP[2]	N/C											
N	DPL[2]	DC1J1V1[2]	DD[8]	DD[9]	DD[10]											
P	DD[11]	DD[12]	DD[13]	DD[14]	DD[15]											
R	N/C	N/C	N/C	DDP[2]	N/C											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A[3]	ALE	SALM1	LRDI1/RRCPCLK1	GND	LOS4/RRCPFP4	TLRDI1/TRCPFP1	RLAIS3/TRCPCLK3	TLAIS4/TRCPDAT4	GND	N/C	GND	GND	GND	VDD	A
A[1]	RDB/E	SALM2	LAIS1/RRCPDAT1	LOS3/RRCPFP3	LRDI4/RRCPCLK4	RLAIS2/TRCPCLK2	TLAIS3/TRCPDAT3	N/C	RCLK3	N/C	REFCLK	GND	VDD	GND	B
A[2]	MBEB	SALM3	LOS2/RRCPFP2	LRDI3/RRCPCLK3	LAIS4/RRCPDAT4	TLRDI2/TRCPFP2	RLAIS4/TRCPCLK4	RCLK1	TCLK	N/C	VDD	VDD	GND	GND	C
A[0]	WRB/RWB	SALM4	LRDI2/RRCPCLK2	LAIS3/RRCPDAT3	RLAIS1/TRCPCLK1	TLAIS2/TRCPDAT2	TLRDI4/TRCPFP4	RCLK2	PGMRCLK	N/C	VDD	VDD	PECLV	GND	D
CSB	RSTB	LOS1/RRCPFP1	LAIS2/RRCPDAT2	VDD	TLAIS1/TRCPDAT1	TLRDI3/TRCPFP3	N/C	RCLK4	PGMTCLK	VDD	N/C	N/C	N/C	N/C	E
										N/C	N/C	N/C	QAVS_2	GND	F
										QAVD_2	RAVD1_B	CN1	CP1	N/C	G
										RAVS1_B	RAVS1_C	RAVD1_C	N/C	N/C	H
										N/C	N/C	TXD1P	TXD1N	N/C	J
										N/C	SD1	RXD1N	RXD1P	RAVS1_A	K
										VDD	RAVD1_A	TXD2P	TXD2N	GND	L
										RAVS2_A	RAVD2_A	SD2	RXD2N	RXD2P	M
										N/C	RAVS2_B	CP2	CN2	RAVD2_B	N
										RAVS2_C	RAVD2_C	N/C	N/C	N/C	P
										N/C	TAVD1_A	TAVS1_A	TAVD1_B	TAVS1_B	R

										VDD	VDD	VDD	GND	GND	T
										N/C	RAVS3_B	CP3	CN3	RAVD3_B	U
										ATP3	ATP1	ATP0	RAVS3_C	RAVD3_C	V
										N/C	N/C	TXD3N	TXD3P	ATP2	W
										RAVS3_A	RAVD3_A	SD3	RXD3N	RXD3P	Y
										VDD	N/C	TXD4N	TXD4P	GND	AA
										RAVD4_A	RAVS4_A	RXD4P	RXD4N	SD4	AB
										RAVS4_B	RAVS4_C	RAVD4_C	N/C	N/C	AC
										QAVD_1	RAVD4_B	CN4	CP4	N/C	AD
										N/C	N/C	N/C	N/C	QAVS_1	AE
										N/C	N/C	N/C	N/C	GND	AF
RSLDCLK2	RSLDCLK1	TTOHCLK4	TTOH3	VDD	TTOHEN2	RTOHFP2	TTOHCLK1	N/C	TMS	VDD	N/C	N/C	N/C	N/C	AG
RSLD2	RSLD1	TTOHFP4	N/C	TTOHCLK3	N/C	RTOH2	TTOHEN1	RTOHFP1	TDO	N/C	VDD	VDD	N/C	GND	AH
TSLDCLK2	TSLDCLK1	TTOHEN4	RTOHFP4	TTOHFP3	RTOHFP3	TTOHCLK2	TTOH1	RTOHCLK1	N/C	TRSTB	VDD	VDD	GND	GND	AJ
TSLD2	TSLD1	TTOH4	RTOHCLK4	TTOHEN3	RTOHCLK3	TTOHFP2	N/C	RTOH1	N/C	TDI	TCK	GND	VDD	GND	AK
N/C	N/C	N/C	RTOH4	GND	RTOH3	TTOH2	RTOHCLK2	TTOHFP1	GND	N/C	GND	GND	GND	VDD	AL
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

T	GND	GND	VDD	VDD	VDD											
U	APL[3]	AC1J1V1/AFP[3]	AD[16]	AD[17]	AD[18]											
V	AD[19]	AD[20]	AD[21]	AD[22]	AD[23]											
W	ADP[3]	N/C	DPL[3]	DC1J1V1[3]	DD[16]											
Y	DD[17]	DD[18]	DD[19]	DD[20]	DD[21]											
AA	GND	DD[22]	DD[23]	DDP[3]	VDD											
AB	APL[4]	AC1J1V1/AFP[4]	AD[24]	AD[25]	AD[26]											
AC	AD[27]	AD[28]	AD[29]	AD[30]	N/C											
AD	AD[31]	ADP[4]	N/C	DPL[4]	DC1J1V1[4]											
AE	DD[24]	DD[25]	DD[26]	DD[27]	DD[28]											
AF	GND	DD[29]	DD[30]	DDP[4]	N/C											
AG	DD[31]	N/C	DFP	N/C	VDD	N/C	N/C	N/C	N/C	N/C	VDD	N/C	N/C	N/C	N/C	VDD
AH	GND	DCK	VDD	VDD	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	TSLD4	TSLD3	VDD
AJ	GND	GND	VDD	VDD	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	TSLDCLK4	TSLDCLK3	VDD
AK	GND	VDD	GND	VBIAS[0]	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	RSLD4	RSLD3	GND
AL	VDD	GND	GND	GND	N/C	GND	N/C	N/C	N/C	N/C	GND	N/C	N/C	RSLDCLK4	RSLDCLK3	GND
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

9 Pin Description (SBGA 520)

The SPECTRA 4x155 is available in a 520-pin SBGA package having a body size of 40.0 mm by 40.0 mm and a ball pitch of 1.27 mm.

9.1 Serial Line side Interface Signals

Pin Name	Type	Pin No.	Function
REFCLK	Input	B4	The reference clock input (REFCLK) provides a jitter-free 19.44 MHz reference clock. It is used as the reference clock by both clock recovery and clock synthesis circuits. All channels share this pin.
RXD1- RXD1+ RXD2- RXD2+ RXD3- RXD3+ RXD4- RXD4+	Diff PECL Input	K3 K2 M2 M1 Y2 Y1 AB2 AB3	The receive differential data inputs (RXD[4:1]+, RXD[4:1]-) contain the 155.52 Mbit/s receive STS-3/3c (STM-1/AU-3/AU-4) stream of each channel. The receive clocks are recovered from the RXD+/- bit stream. RXD[4:1]+/- inputs are expected to be NRZ encoded.
SD1 SD2 SD3 SD4	Single-Ended PECL Input	K4 M3 Y3 AB1	The Signal Detect pin (SD[4:1]) indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. A PECL high indicates the presence of valid data and a PECL low indicates a Loss of Signal (LOS). It is mandatory that SD[4:1] be terminated into the equivalent network that RXD1-4+/- is terminated into. This pin is available independently for each channel.
TXD1- TXD1+ TXD2- TXD2+ TXD3- TXD3+ TXD4- TXD4+	Diff. TTL Output (Externally converted to PECL)	J2 J3 L2 L3 W3 W2 AA3 AA2	The transmit differential data outputs (TXD[4:1]+, TXD[4:1]-) contain the 155.52 Mbit/s transmit STS-3/3c (STM-1/AU-3/AU-4) stream. TXD[4:1]+/- outputs are NRZ encoded.
TCLK	Output	C6	The transmit byte clock (TCLK) output provides a timing reference for the SPECTRA 4x155 self-timed channels. TCLK always provides a divide-by-eight of the synthesized line rate clock and thus has a nominal frequency of 19.44 MHz. TCLK does not apply to internally loop-timed channels, in which case the channel's RCLK1-4 provides transmit timing information. When not used, TCLK can be held low using the TCLKEN bit in the SPECTRA 4x155 Clock Control register.

Pin Name	Type	Pin No.	Function
RCLK1 RCLK2 RCLK3 RCLK4	Output	C7 D7 B6 E7	The Receive Clock (RCLK1-4) signal provides a timing reference for the SPECTRA 4x155 receive line interface outputs. The signal is nominally 19.44 MHz. It is a divide-by-eight of the recovered clock. When not used, RCLK1-4 can be held low using the RCLKEN bit in the SPECTRA 4x155 Clock Control register.
PGMRCLK	Output	D6	The programmable receive clock (PGMRCLK) signal provides timing reference for the receive line interface. PGMRCLK is a divided version of one of the RCLK clocks. The PGMRCHSEL bits of the Master Clock Control register are used to select which of the four clocks is the source for PRGMRCLK. When the PGMRCLKSEL bit of the Master Clock Control register is set low, PGMRCLK is a nominal 19.44 MHz, 40-60% duty cycle clock. When PGMRCLKSEL register bit is set to high, PGMRCLK is a nominal 8 KHz, 40-60% duty cycle clock. PGMRCLK output can be disabled and held low by programming the PGMRCLKEN bit in the Master Clock Control register.
PGMTCLK	Output	E6	The programmable transmit clock (PGMTCLK) signal provides timing reference for the transmit line interface. PGMTCLK is a divided version of the TCLK clock. When the PGMTCLKSEL register bit is set low, PGMTCLK is a nominal 19.44 MHz, 40-60% duty cycle clock. When the PGMTCLKSEL bit of the Master Clock Control register is set high, PGMTCLK is a nominal 8 KHz, 40-60% duty cycle clock. PGMTCLK output can be disabled and held low by programming the PGMTCLKEN bit in the Master Clock Control register.
CP1 CN1 CP2 CN2 CP3 CN3 CP4 CN4	Analog	G2 G3 N3 N2 U3 U2 AD2 AD3	The analog CP1-4 and CN1-4 pins are provided for applications that must meet SONET/SDH jitter transfer specifications. A 220 nF X7R 10% ceramic capacitor can be attached across each CP1-4 and CN1-4 pair.
PECLV	Input	D2	The PECL receiver input voltage (PECLV) pin configures the PECL receiver level shifter. When PECLV is set to logic zero, the PECL receivers are configured to operate with a 3.3V input voltage. When PECLV is set to logic one, the PECL receivers are configured to operate with a 5.0 V input voltage.

9.2 Section/Line/Path Status and Alarm Signals

Pin Name	Type	Pin No.	Function
SALM1 SALM2 SALM3 SALM4	Output	A13 B13 C13 D13	The section alarm (SALM1-4) output may be set high when an OOF, LOS, LOF, LAIS, LRDI, section trace identifier mismatch (RS-TIM), section trace identifier unstable (RS-TIU), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using bits in the Section Alarm Output Control #1 and #2 registers. SALM1-4 is set low when none of the enabled alarms are active. SALM1-4 is updated on the rising edge of RCLK1-4.
LOF1 LOF2 LOF3 LOF4	Output	C22 B22 A22 D21	The Loss of Frame (LOF1-4) output is set high when an OOF condition exists for a total OOF period of 3 ms during which there is no continuous, in-frame period of 3 ms. LOF1-4 is cleared when an in-frame condition exists for a continuous period of 3 ms The LOF1-4 output is updated on the rising edge of RCLK1-4
LOS1/ LOS2/ LOS3/ LOS4/	Output	E13 C12 B11 A10	Loss of Signal (LOS1-4) is active when the ring control port is disabled. LOS1-4 is set high when a violating period (20 ± 2.5 µs) of consecutive all zeros patterns is detected in the incoming stream. LOS1-4 is set low when two valid framing words (A1, A2) are detected, and during the intervening time (125 µs), there are no other violating period with all zeros patterns is observed. LOS1-4 is updated on the rising edge of RCLK1-4.
/RRCPFP1 /RRCPFP2 /RRCPFP3 /RRCPFP4		E13 C12 B11 A10	The Receive ring control port frame position (RRCPFP1-4) signal identifies bit positions in the receive ring control port data (RRCPDAT1-4) when the ring control port is enabled. RRCPFP1-4 is set high during the filtered K1 and K2 bit positions, the change of APS value bit position, the protection switch byte failure bit position, and the send line AIS and send line RDI bit positions of the RRCPDAT1-4 streams (21 bits). RRCPFP1–4 is set low during the reserved L-REI clock cycles. RRCPFP1-4 can be connected directly to the TRCPFP1-4 inputs of a mate SPECTRA 4x155 in ring-based Add/Drop multiplexer applications. The RCPEN bit in the Ring Control register of the corresponding channel controls the enabling and disabling of the ring control port. The RRCPFP1-4 signal is updated on the falling edge of RRCPCLK1-4.

Pin Name	Type	Pin No.	Function
LRDI1/ LRDI2/ LRDI3/ LRDI4/ /RRCPCLK1 /RRCPCLK2 /RRCPCLK3 /RRCPCLK4	Output	A12 D12 C11 B10 A12 D12 C11 B10	The RDI (LRDI1-4) signal is active when the ring control port is disabled. LRDI1-4 is set high when line RDI is detected in the corresponding incoming stream. LRDI is declared when the 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. LRDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LRDIDET bit in the RLOP Control and Status register of the corresponding channel controls the selection of three or five consecutive frames. LRDI1-4 is updated on the rising edge of RCLK1-4. The Receive ring control port clock (RRCPCLK1-4) signal provides timing for the receive ring control port when the ring control port is enabled. RRCPCLK1-4 is nominally a 3.24 MHz clock and can be connected directly to the TRCPCLK1-4 inputs of a mate SPECTRA 4x155 in ring-based Add-Drop multiplexer applications. The RCPEN bit in the Ring Control register of the corresponding channel controls the enabling and disabling of the ring control port. The RRCPFP1-4 and RRCPDAT1-4 signals are updated on the falling edge of RRCPCLK1-4.
LAIS1/ LAIS2/ LAIS3/ LAIS4/ /RRCPDAT1 /RRCPDAT2 /RRCPDAT3 /RRCPDAT4	Output	B12 E12 D11 C10 B12 E12 D11 C10	The line alarm indication (LAIS1-4) signal is active when the ring control port is disabled. LAIS1-4 is set high when line AIS is detected in the corresponding incoming stream. Line AIS is declared when the 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LAISDET bit in the RLOP Control and Status register of the corresponding channel controls the selection of three or five consecutive frames. The LAIS1-4 outputs are updated on the rising edge of RCLK1-4. The Receive ring control port data (RRCPDAT1-4) signal contains the receive ring control port data stream when the ring control port is enabled. The receive ring control port data consists of the filtered K1, K2 byte values, the change of APS value bit position, the protection switch byte failure status bit position, the send line AIS and send line RDI bit positions, and the line REI bit positions. RRCPDAT1-4 can be connected directly to the TRCPDAT1-4 inputs of a mate SPECTRA 4x155 in ring-based Add-Drop multiplexer applications. The RCPEN bit in the Ring Control register of the corresponding channel controls the enabling and disabling of the ring control port. The RRCPDAT1-4 signal is updated on the falling edge of RRCPCLK1-4.

Pin Name	Type	Pin No.	Function
RLAIS1/ RLAIS2/ RLAIS3/ RLAIS4/	Input	D10 B9 A8 C8	The receive line AIS insertion (RLAIS1-4) signal controls the insertion of line AIS in the received stream by the RSOP block, when the ring control port is disabled. When one of the RLAIS1-4 pins is set high, line AIS is inserted in the corresponding received stream. When RLAIS1-4 is set low, line AIS may be optionally inserted automatically upon detection of LOS, LOF, section trace alarms or line AIS in the incoming stream. The Receive LAIS Control register contains the register bits that control the alarms that are inserted using the RLAIS pin of the corresponding channel. RLAIS signals are internally retimed. RLAIS1-4 must be asserted for a minimum period of one SONET/SHD frame (125 us) to be detected by the SPECTRA 4x155. Line AIS must be held for a minimum of three SONET/SDH frames to be compliant to the SONET/SDH standards.
/TRCPCLK1 /TRCPCLK2 /TRCPCLK3 /TRCPCLK4		D10 B9 A8 C8	The Transmit ring control port clock (TRCPCLK1-4) signal provides timing for the transmit ring control port when the ring control port is enabled. The TRCPCLK1-4 signal is nominally a 3.24 MHz clock and can be connected directly to the RRCPCLK output of a mate SPECTRA 4x155 in ring-based Add/Drop multiplexer applications. The RCPEN bit in the Ring Control register of the corresponding channel controls the enabling and disabling of the ring control port. The TRCPFP1-4 and TRCPDAT1-4 signals are sampled on the rising edge of TRCPCLK1-4.

Pin Name	Type	Pin No.	Function
TLRDI1/ TLRDI2/ TLRDI3/ TLRDI4/	Input	A9 C9 E9 D8	The active high transmit RDI (TLRDI1-4) signal controls the insertion of a remote defect indication in the transmit outgoing stream when the ring control port is disabled. When TLRDI1-4 is set high, bits 6, 7, and 8 of the K2 byte are set to the pattern 110. When TLRDI1-4 is set low, line RDI may also be inserted using the LRDI bit in the TLOP Control register of the corresponding channel. Line RDI may also be inserted upon detection of LOS, LOF, or line AIS in the receive stream, using the bits in the Transmit Line RDI Control register of the corresponding channel. The TLRDI1-4 input takes precedence over the TTOH1-4 and TTOHEN1-4 inputs. TLRDI signals are internally retimed. TLRDI1-4 must be asserted for a minimum period of one SONET/SHD frame (125 us) to be detected by the SPECTRA 4x155. Line RDI must be held for a minimum of three SONET/SDH frames to be compliant to the SONET/SDH standards.
/TRCPFP1 /TRCPFP2 /TRCPFP3 /TRCPFP4		A9 C9 E9 D8	The Transmit ring control port frame position (TRCPFP1-4) signal identifies bit positions in the transmit ring control port data (TRCPDAT1-4) when the ring control port is enabled. TRCPFP1-4 is high during the send line AIS and the send line RDI bit positions in the TRCPDAT1-4 stream. TRCPFP1-4 is set high for 19 bits locations prior to those 2 bit locations. These 19 bit locations are reserved. TRCPFP1–4 is set low during the reserved L-REI clock cycles. TRCPFP1-4 can be connected directly to the RRCPFP1-4 output of a mate SPECTRA 4x155 in ring-based Add-Drop multiplexer applications. The RCPEN bit in the Ring Control register of the corresponding channel controls the enabling and disabling of the ring control port. The TRCPFP1-4 signal is sampled on the rising edge of TRCPCLK1-4.

Pin Name	Type	Pin No.	Function
TLAIS1/ TLAIS2/ TLAIS3/ TLAIS4/ /TRCPDAT1 /TRCPDAT2 /TRCPDAT3 /TRCPDAT4	Input	E10 D9 B8 A7 E10 D9 B8 A7	The active high transmit AIS (TLAIS1-4) controls the insertion of line AIS in the transmit outgoing stream when the ring control port is disabled. When TLAIS1-4 is set high, the complete frame (except the section overhead or line/regenerator section) is overwritten with the all-ones pattern (before scrambling). The TLAIS1-4 input takes precedence over the TTOH1-4 and TTOHEN1-4 inputs. TLAIS signals are internally retimed. TLAIS1-4 is required to be asserted for a minimum period of one SONET/SHD frame (125 us) to be detected by the SPECTRA 4x155. Line AIS must be held for a minimum of three SONET/SDH frames to be compliant to the SONET/SDH standards. The Transmit ring control port data (TRCPDAT1-4) signal contains the transmit ring control port data stream when the ring control port is enabled. The transmit ring control port data consists of the send line AIS and the send line RDI bit positions, and the line REI bit positions. TRCPDAT1-4 can be connected directly to the RRCPDAT1-4 output of a mate SPECTRA 4x155 in ring-based Add/Drop multiplexer applications. The K1/K2, COAPSI, PSBFI and PSBFV position of the RRCPDAT lines are not used by the TRCPDAT. The RCPEN bit in the Ring Control register of the corresponding channel controls the enabling and disabling of the ring control port. TRCPDAT1-4 is sampled on the rising edge of TRCPCLK1-4.

9.3 Receive Section/Line/Path Overhead Extraction Signals

Pin Name	Type	Pin No.	Function
RTOHCLK1 RTOHCLK2 RTOHCLK3 RTOHCLK4	Output	AJ7 AL8 AK10 AK12	The receive transport overhead clock (RTOHCLK1-4) output is used to update the received transport overhead outputs (RTOH1-4 and RTOHFP1-4). RTOHCLK1-4 is nominally a 5.184 MHz clock generated by gapping a 6.48 MHz clock. RTOHCLK1-4 has a 33% high duty cycle. The RTOHFP1-4 and RTOH1-4 outputs are updated on the falling edge of RTOHCLK1-4.
RTOH1 RTOH2 RTOH3 RTOH4	Output	AK7 AH9 AL10 AL12	The receive transport overhead (RTOH1-4) bit serial output signal contains the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) from the incoming stream. The RTOH1-4 output is updated on the falling edge of RTOHCLK1-4 and should be sampled externally on the rising edge of RTOHCLK1-4.

Pin Name	Type	Pin No.	Function
RTOHFP1 RTOHFP2 RTOHFP3 RTOHFP4	Output	AH7 AG9 AJ10 AJ12	The receive transport overhead frame position (RTOHFP1-4) signal is used to locate the most significant bit (MSB) on the RTOH1-4 serial stream. RTOHFP1-4 is set high when bit 1 (the most significant bit) of the first framing byte (A1) is present in the RTOH1-4 stream. RTOHFP1-4 can also be sampled on the rising edge of RSLDCLK1-4 to locate the MSB of the RSLD1-4 serial output stream. The generation of this clock is aligned with the generation of RTOHFP1-4. RTOHFP1-4 is updated on the falling edge of RTOHCLK1-4.
RPOHCLK	Output	A27	The receive path overhead clock (RPOHCLK1-4) provides timing to process the B3E signal, receive alarm port (RAD), path Z5 growth byte (tandem path incoming error count and data link), and to sample the extracted path overhead of the four STS-3/3c (STM-1/AU-3/AU-4) streams. RPOHCLK is a nominally 12.96 MHz, 50% duty cycle clock. RTCEN and RTCOH are sampled on the rising edge of the RPOHCLK signal. B3E, RAD, RALM, RPOH, RPOHEN and RPOHFP are updated on the falling edge of the RPOHCLK signal.
RPOHFP	Output	C26	The receive path overhead frame position signal (RPOHFP) may be used to locate the individual path overhead bits in the path overhead data stream (RPOH). RPOHFP signal is logic one when bit 1 (the most significant bit) of the path trace byte (J1) of channel one’s first STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) is present in the RPOH stream. RPOHFP may also be used to locate the BIP error count and path RDI indication bits on the receive alarm port data signal (RAD). RPOHFP is logic one when the first of eight BIP error positions of channel one’s first STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) stream is present on the receive alarm data signal (RAD). RPOHFP is also used to help find the alignment of the B3E output and RTCEN/RTCOH inputs. RPOHFP signal is updated on the falling edge of the RPOHCLK signal.
RPOH	Output	E25	The receive path overhead data signal (RPOH) contains the path overhead bytes (J1, B3, C2, G1, F2, H4, Z3, Z4, and Z5) extracted from the path overhead of the three STS-1 (STM-0/AU-3) streams or STS-3c (STM-1/AU-4) streams in all four channels. The corresponding RPOHEN signal is set high to identify the valid overhead bytes that are presented. RPOH is updated on the falling edge of RPOHCLK.
RPOHEN	Output	B26	The receive path overhead enable signal (RPOHEN) indicates the validity of the path overhead bytes extracted to the RPOH from the path overhead of the three STS-1 (STM-0/AU-3) streams or STS-3c (STM-1/AU-4) streams in all four channels. When RPOHEN signal is set high, the corresponding path overhead byte presented on the RPOH is valid. When RPOHEN is set low, the corresponding path overhead byte presented on the RPOH is invalid. RPOHEN

Pin Name	Type	Pin No.	Function
			also validates the B3E output. RPOHEN is updated on the falling edge of RPOHCLK.
RAD	Output	D23	The receive alarm port data signal (RAD) contains the path BIP error count and the path remote alarm indication status of the three STS-1 (STM-0/AU-3) streams or STS-3c (STM-1/AU-4) streams for all four channels. In Addition, the RAD contains the transmit K1 and K2 bytes of the four transmit streams when not generating AIS-L on the transmit stream. RPOHFP is used to determine the alignment of the RAD output. RAD is updated on the falling edge of RPOHCLK.
B3E	Output	C21	The bit interleaved parity error signal (B3E) carries the path BIP-8 error detected for each STS-1 (STM-0/AU-3) and STS-3c (STM-1/AU-4) in the receive stream. It is set high for one RPOHCLK period for each path BIP-8 error detected (up to eight per frame) or when errors are treated on a block basis, is set high for only one RPOHCLK period if any of the path BIP-8 bits are in error. Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed BIP-8 for the previous frame. The B3E signal toggles during the B3 time periods on RPOH and is valid only during RPOHEN set high. RPOHFP is used to determine the alignment of the B3E output. B3E is updated on the falling edge of RPOHCLK.
RTCEN	Input	D24	The receive tandem connection overhead insert enable signal (RTCEN) controls the insertion of incoming error count and data link into the tandem connection maintenance byte (Z5) on the Drop bus, on a bit-by-bit basis for each STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) stream. When RTCEN is set high, the data on the corresponding RTCOH stream is inserted into the associated bit in the Z5 byte. RTCEN has significance only during the J1 byte positions in the RPOHCLK clock sequence where RPOHEN is also set high and is ignored at all other times. Setting low the RTC_EN control bit in the RPOP Z5 Growth Control Register disables the RTCEN and RTCOH ports completely. RTCEN is sampled on the rising edge of RPOHCLK.
RTCOH	Input	C24	The receive tandem connection overhead data signal (RTCOH) contains the incoming error count and data link message to be inserted into the tandem connection maintenance byte (Z5) in each STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) stream. When RTCEN is set high and RPOHEN is high, the values sampled on RTCOH are inserted into the Z5 byte of the corresponding stream on the Drop bus. When RTCEN is set low, the received Z5 byte is passed through unmodified. Setting low the RTC_EN control bit in the RPOP Z5 Growth Control Register disables the RTCEN and RTCOH ports completely. RTCOH is sampled on the rising edge of RPOHCLK.
RALM	Output	B21	The Receive Alarm (RALM) signal is a multiplexed output of individual alarms of the receive STS-1 (STM-0/AU3) or STS-

Pin Name	Type	Pin No.	Function
			3c (STM-1/AU4) streams. Each alarm represents the logical OR of the LOP, PAIS, PRDI, PERDI, LOM, LOPCON, PAISCON, UNEQ, PSLU, PSLM, TIU-P, TIM-P status of the corresponding stream. In Addition to these alarms, the LOS (LOS), LOF (LOF) or line AIS (LAIS) in the corresponding STS-3 (STM-1) SONET/SDH streams can also be reported on RALM. The RPPS RALM Output Control #1 and #2 registers control the selection of alarms to be reported. RALM is updated on the falling edge of RPOHCLK and may transition anywhere during the individual STS-1 time slot period. The loss of pointer signal (LOP) indicates the loss of pointer state in the corresponding STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) SONET/SDH stream. LOP is set high when invalid pointers are received in eight consecutive frames, or if eight consecutive enabled NDFs are detected in the stream. The path alarm indication signal (PAIS) indicates the path AIS state of the corresponding STS-1 (STM-0/AU3) or STS-3c (STM-1/AU4) SONET/SDH stream. PAIS is set high when an all-ones pattern is observed in the pointer bytes (H1 and H2) for three consecutive frames in the stream. The path remote defect indication signal (PRDI) indicates the path remote state of the corresponding STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) SONET/SDH stream. PRDI is set high when the path RDI alarm bit (bit 5) of the path status (G1) byte is set high for five or ten consecutive frames. The RDI10 bit in the RPOP Pointer MSB register controls whether five or ten consecutive frames will cause a PRDI indication. The path enhanced remote defect indication signal (PERDI) indicates the path enhanced remote state of the corresponding STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) SONET/SDH stream. PERDI is set high when the path ERDI alarm code (bits 5,6,7) of the path status (G1) byte is set to the same alarm codepoint for five or ten consecutive frames. The RDI10 bit in the RPOP Pointer MSB register controls whether five or ten consecutive frames will cause a PRDI indication. The loss of multi-frame signal (LOM) indicates the tributary multi-frame synchronization status of the corresponding STS-1 (STM-0/AU3) or STS-3c (STM-1/AU-4) SONET/SDH stream. LOM is set high if a correct four-frame sequence is not detected in eight frames. The loss of pointer concatenation and path AIS concatenation signals (LOPCON and PAISCON) are the concatenated alarms for STS-3c (STM-1/AU-4) SONET/SDH streams. The receive path unequipped status (UNEQ) indicates the unequipped status of the path signal label of the corresponding STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) SONET/SDH stream. UNEQ is set high when the filtered path signal label indicates unequipped and is dependent on the selected UNEQ mode. The receive path signal label unstable status (PSLU) reports the stable/unstable status (mode 1) of the path signal label in

Pin Name	Type	Pin No.	Function
			the corresponding STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) SONET/SDH stream. PSLU is set high when the current received C2 byte differs from the previous C2 byte for five consecutive frames. The receive path signal label mismatch (PSLM) status reports the match/mismatch status (mode 1 and mode 2) for the path signal label of the corresponding STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) SONET/SDH stream. In mode 1, PSLM is set high when the accepted PSL differs from the expected PSL written by the microprocessor. In mode 2, PSLM is set high when 5 consecutive mismatches have been declared The receive path trace identifier unstable status (TIU-P) reports the stable/unstable status (mode 1 and mode 2) of the path trace identifier framer of the corresponding STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) SONET/SDH stream. In mode 1, TIU is set high when the current message differs from its immediate predecessor for eight consecutive frames. In mode 2, TIU is set high when three consecutive 16-byte windows of trace bytes are detected to have errors. TIU2 is set low when the same trace byte is received in forty-eight consecutive SONET/SDH frames. The receive path trace identifier mismatch (TIM-P) status reports the match/mismatch status (mode 1) of the path identifier message framer of the corresponding STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) SONET/SDH stream. TIM-P is set high when the accepted identifier message differs from the expected message written by the microprocessor. Please refer to the individual alarm interrupt descriptions and Functional Description Section for more details on each alarm.

9.4 Transmit Section/Line/Path Overhead Insertion Signals

Pin Name	Type	Pin No.	Function
TTOHCLK1 TTOHCLK2 TTOHCLK3 TTOHCLK4	Output	AG8 AJ9 AH11 AG13	The transmit transport overhead clock (TTOHCLK1-4) is used to clock in the transport overhead (TTOH1-4) to be transmitted along with the overhead enable (TTOHEN1-4). TTOHCLK1-4 is nominally a 5.184 MHz clock generated by gapping a 6.48 MHz clock. TTOHCLK1-4 has a 33% high duty cycle. TTOHFP1-4 and TTOH1-4.are updated on the falling edge of TTOHCLK1-4.
TTOH1 TTOH2 TTOH3 TTOH4	Input	AJ8 AL9 AG12 AK13	The transmit transport overhead (TTOH1-4) bit serial input signal contains the transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2) to be transmitted and errors masks to be applied on the B1, B2, H1 and H2 transmitted bytes. Insertion of the bytes must be accompanied by a high TTOHEN1-4 signal. TTOH1-4 is sampled on the rising edge of TTOHCLK1-4.

Pin Name	Type	Pin No.	Function
TTOHEN1 TTOHEN2 TTOHEN3 TTOHEN4	Input	AH8 AG10 AK11 AJ13	The transmit transport overhead insert enable (TTOHEN1-4) signal controls the source of the transport overhead data which is inserted in the outgoing stream. When TTOHEN1-4 is high during bit 1 (most significant bit) of a TOH byte on TTOH, the sampled TOH byte is inserted into the corresponding transport overhead byte positions (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). While TTOHEN1-4 is low during the most significant bit of a TOH byte on TTOH, that sampled byte is ignored and the default values are inserted into these transport overhead bytes. The overhead byte enabled by the TTOHEN input takes precedence over the TSLD input. When TTOHEN1-4 is high during the most significant bit of the H1, H2, B1 or B2 TOH byte positions on TTOH1-4, the sampled TOH byte is logically XORed with the associated incoming byte to force bit errors on the outgoing byte. A logic low bit in the TTOH1-4 byte allows the incoming bit to go through while a bit set to logic high will toggle the incoming bit. A low level on TTOHEN1-4 during the MSB of the TOH byte disables the error forcing for the entire byte. When the transmit trace enable (TREN) bit in the TTOC Transport Overhead Byte Control register of the corresponding channel is a logic one, the J0 byte contents are sourced from the section trace buffer, regardless of the state of TTOHEN1-4. TTOHEN1-4 is sampled on the rising edge of TTOHCLK1-4.
TTOHFP1 TTOHFP2 TTOHFP3 TTOHFP4	Output	AL7 AK9 AJ11 AH13	The transmit transport overhead frame position (TTOHFP1-4) signal is used to locate the most significant bit (MSB) on the TTOH1-4 serial stream. TTOHFP1-4 is set high when bit 1 (the most significant bit) of the first framing byte (A1) should be present on the TTOH1-4 stream. TTOHFP1-4 can be sampled on the rising edges of TSLDCLK1-4 to locate the MSB of the TSLD serial input stream. The generation of this clock is aligned with the generation of TTOHFP1-4. TTOHFP1-4 is updated on the falling edge of TTOHCLK1-4.
TAD	Input	A24	The transmit alarm port data signal (TAD) contains the path REI count and the path RDI status to be inserted into the four STS-3/3c (STM-1/AU-3/AU-4) streams. In Addition, the TAD input contains the K1 and K2 bytes from a mate SPECTRA 4x155 to be inserted into the four channels transport overhead. TAD ~~TTOHEN1-4~~ takes precedence over TTOHEN1-4 when enabled~~TAD~~. The RXSEL[1:0] bits in the TPPS Path Configuration register control the source of the transmit P-REI and P-RDI. TAD is sampled on the rising edge of TACK.
TAFP	Input	B24	The transmit alarm port frame pulse signal (TAFP) marks the first bit of the transmit alarm message in each SONET/SDH frame. TAFP is pulsed high to mark the first path REI bit location of channel one's first STS-1 (STM-0/AU-3) stream or

Pin Name	Type	Pin No.	Function
			the first path REI bit location of the STS-3c (STM-1/AU-4) stream. TAFP is sampled on the rising edge of TACK.
TACK	Input	E23	The transmit alarm port clock (TACK) provides timing for transmit alarm port. TACK is nominally a 12.96 MHz, 50% duty cycle clock. Inputs TAD and TAFP are sampled on the rising edge of TACK.

9.5 Receive Section/Line DCC Extraction Signals

Pin Name	Type	Pin No.	Function
RSLDCLK1 RSLDCLK2 RSLDCLK3 RSLDCLK4	Tristate Output	AG14 AG15 AL17 AL18	The receive section or line data communication channel (DCC) clock (RSLDCLK1-4) is used to update the received section or line DCC (RSLD1–4). When selecting to clock the section DCC, RSLDCLK1-4 is a 192 kHz clock with nominal 50% duty cycle. When selecting to clock the line DCC, RSLDCLK1-4 is a 576 kHz clock with nominal 50% duty cycle. RTOHFP1-4 may be sampled high at the same time as bit 1 (MSB) on RSLD1-4. The RTOC Overhead Control register of the corresponding channel contains the RSLDSEL register bit used to select the section or line DCC. The same register also contains the RSLD_TS register bit that can be used to tri-state RSLDCLK1-4 and RSLD1-4 outputs. In both cases, RSLD1-4 is updated on the falling edge of RSLDCLK1-4.
RSLD1 RSLD2 RSLD3 RSLD4	Tristate Output	AH14 AH15 AK17 AK18	The receive section or line DCC (RSLD1-4) bit serial output signal contains the received section data communication channel (D1-D3) or the line data communication channel (D4-D12). The RTOC Overhead Control register of the corresponding channel contains the RSLDSEL register bit used to select the section or line DCC. The same register also contains the RSLD_TS register bit that can be used to tri-state RSLDCLK1-4 and RSLD1-4 outputs. RSLD1-4 is updated on the falling edge of RSLDCLK1-4 and should be sampled externally on the rising edge of RSLDCLK1-4.

9.6 Transmit Section/Line DCC Insertion Signals

Pin Name	Type	Pin No.	Function
TSLDCLK1 TSLDCLK2 TSLDCLK3 TSLDCLK4	Tristate Output	AJ14 AJ15 AJ17 AJ18	The transmit section or line data communication channel (DCC) clock (TSLDCLK1-4) is used to clock in the transmit section or line DCC (TSLD1-4). When clocking the section DCC, TSLDCLK1-4 is a 192 kHz clock with nominal 50% duty cycle. When clocking the line

Pin Name	Type	Pin No.	Function
			DCC, TSLDCLK1-4 is a 576 kHz clock with nominal 50% duty cycle. TTOHFP1-4 is used to identify when bit 1 (MSB) of the first A1 byte should be present on TSLD1-4. The TTOC Overhead Control register of the corresponding channel contains the TSLD_SEL register bit used to select the section or line DCC. The same register also contains the TSLD_TS register bit that can be used to tri-state the TSLDCLK1-4 output. In both cases, TSLD1-4 is sampled on the rising edge of TSLDCLK1-4.
TSLD1 TSLD2 TSLD3 TSLD4	Input	AK14 AK15 AH17 AH18	The transmit section or line DCC (TSLD) bit serial input signal contains the section data communication channel (D1-D3) or the line data communication channel (D4-D12) to be transmitted. TTOHFP1-4 is used to identify the required alignment of TSLD. The TTOH1-4 and TTOHEN1-4 inputs take precedence over TSLD1-4. The TTOC Overhead Control register of the corresponding channel contains the TSLD_SEL register bit used to select the section or line DCC. The same register also contains the TSLD_VAL register bit used to specify a value for the DCC not inserted via TSLD. TSLD1-4 is sampled on the rising edge of TSLDCLK1-4.

9.7 Transmit Path AIS Insertion Signals

Pin Name	Pin Type	Pin No.	Function
DPAISCK	Input	D27	The Drop bus path alarm indication clock signal (DPAISCK) provides timing for system Drop path alarm indication signal (DPAIS). DPAISCK is a clock of arbitrary phase and frequency within the limits specified in the A.C. Timing section of this document. Inputs DPAIS and DPAISFP are sampled on the rising edge of DPAISCK.
DPAISFP	Input	B28	The active high Drop bus path alarm indication frame pulse signal (DPAISFP) is used to identify the alignment of the DPAIS signal. DPAISFP is set high to mark the path request of channel one’s the first Drop bus STS-1 (STM-0/AU-3) stream or STS-3c (STM-1/AU-4) stream. In the absence of a frame pulse, the device will maintain the last alignment and wrap around on its own. DPAISFP is sampled on the rising edge of DPAISCK.
DPAIS	Input	C27	The active high Drop bus path alarm indication signal (DPAIS) is a timeslot multiplexed signal that controls the insertion of path alarm indication signal (PAIS) on the Drop bus (DD[31:24], DD[23:16], DD[15:8], DD[7:0]) on a per STS-1/STM-1(AU3) or STS-3c/STM1(AU4)basis. A high level on DPAIS during a specific timeslot forces the insertion of the all-ones pattern into the corresponding SPE and

Pin Name	Pin Type	Pin No.	Function
			the payload pointer bytes (H1, H2, and H3) presented on the Drop bus. A high during the first time slot of a channel carrying an STS-3c/STM-1(AU4) stream will force the entire concatenated SPE to all-ones. A high during the second or third time slot of a channel carrying an STS-3c/STM-1(AU4) will have no effect. Path AIS can also be inserted by setting the IPAIS control bit in the RTAL Control register or in response to receive alarms by the RPPS Path AIS Control #1 and #2 registers. DPAIS may be enabled or disabled on a per slice basis via the DPAIS_EN bit in the RPPS Path AIS Control register #1. DPAIS is sampled on the rising edge of DPAISCK.
TPAISCK	Input	E26	The Transmit path alarm indication clock signal (TPAISCK) provides timing for system Add side path alarm indication signal (PAIS) assertion. TPAISCK is a clock of arbitrary phase and frequency within the limits specified in the A.C. Timing section of this document. Inputs TPAIS and TPAISFP are sampled on the rising edge of TPAISCK.
TPAISFP	Input	B27	The active high Transmit path alarm indication frame pulse signal (TPAISFP) is used to identify the alignment of the TPAIS signal. TPAISFP is set high to mark the path request of channel one's the first transmit STS-1 (STM-0/AU-3) stream or STS-3c (STM-1/AU-4) stream. In the absence of a frame pulse, the device will maintain the last alignment and wrap around on its own. TPAISFP is sampled on the rising edge of TPAISCK.
TPAIS	Input	D26	The active high Transmit path alarm indication signal (TPAIS) is a timeslot multiplexed signal that controls the insertion of path in the transmit stream on a per STS-1/STM-1(AU3) or STS-3c/STM1(AU4) basis. A high level on TPAIS during a specific timeslot forces the insertion of the all-ones pattern into the corresponding SPE and the payload pointer bytes (H1, H2, and H3). A high during the first time slot of a channel carrying an STS-3c/STM-1(AU4) stream will force the entire concatenated SPE to all-ones. A high during the second or third time slot of a channel carrying an STS-3c/STM-1(AU4) will have no effect. Path AIS can also be inserted by setting the PAIS control bit in the TTAL Control register or in response to Add Bus alarms by the TPPS Path AIS Control register. TPAIS may be enabled or disabled on a per slice basis via the TPAIS_EN bit in the TPPS Path AIS Control register. TPAIS is sampled on the rising edge of TPAISCK.

9.8 Drop Bus Telecom Interface Signals

Pin Name	Pin Type	Pin No.	Function
DCK	Input	AH30	The Drop bus clock (DCK) provides timing for the Drop bus

Pin Name	Pin Type	Pin No.	Function
			interface. DCK is nominally a 77.76 MHz, 50% duty cycle clock when the Drop interface is configured as a single bus interface. DCK is nominally a 19.44 MHz, 50% duty cycle clock when the Drop interface is configured as a quad STS-3 (STM-1) interface. Frequency offsets between line side clock (or divided by 4 version of) and DCK are accommodated by pointer justification events on the Drop bus. DFP is sampled on the rising edge of DCK. Outputs DPL[4:1], DC1J1V1[4:1], DDP[4:1] and DD[31:0] are updated on the rising edge of DCK when used.
DFP	Input	AG29	The active high Drop bus reference frame position signal (DFP) indicates when the first byte of the synchronous payload envelope (SPE byte #1) is available on the DD[7:0], DD[15:8], DD[23:16] and DD[31:24] buses. For the single bus interface the first SPE byte of channel one STS-1 #1 is identified. For the quad bus STS-3 (STM-1) interface the first SPE byte of all channels STS-1 #1 on the four output buses identified. Note that DFP has a fixed relationship to the SONET/SDH frame; the start of payload is determined by the STS (AU) pointer and may change relative to DFP. Forced changes of the Drop bus frame alignment by displacing of the regular DFP pulse will cause errors and will force the need to resynchronize or regenerate the RPPS PRBS monitors and generators. The SPECTRA 4x155 will flywheel in the absence of a DFP pulse. DFP is sampled on the rising edge of DCK.
DD[0] DD[1] DD[2] DD[3] DD[4] DD[5] DD[6] DD[7]	Output	H29 H28 H27 J31 J30 J29 J28 J27	In single Drop bus interface mode, the Drop bus data (DD[7:0]) contains the multiplexed STS-3/3c(STM-1/AU-3/AU-4) received SONET/SDH payload data of all four channels. In quad Drop bus interface STS-3(STM-1) mode, the Drop bus data (DD[7:0]) contains the channel one STS-3/3c (STM-1/AU-3/AU-4) received SONET/SDH payload data. When the Drop bus TSI functionality is disabled, the Dropped payload multiplexing corresponds to the SONET/SDH data received on channel #1. TSI may be used to reorder this multiplexing on the Drop bus. STS-1/STM-1(AU3)'s within a channel or between channels, along with entire channels may be swapped. The transport overhead bytes, with the exception of the H1, H2 pointer bytes and when there are no negative pointer justifications the H3, are set to zeros. The fixed framing patterns for the A1 and A2 framing bytes may be inserted. The GEN_A1A2_EN bit in the DPGM Generator Control #1 register enables insertion of the A1 and A2 framing bytes. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. The H4BYP and CLRFS bits in the RTAL Control register control the insertion of the H4 byte and the value of the fixed stuff columns. DD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DD[7:0] is updated on the rising edge of DCK. The Drop interface mode is set via the DTMODE register bit in the Drop

Pin Name	Pin Type	Pin No.	Function
			Bus Configuration register.
DD[8] DD[9] DD[10] DD[11] DD[12] DD[13] DD[14] DD[15]	Output	N29 N28 N27 P31 P30 P29 P28 P27	In single Drop bus interface mode, the Drop bus data (DD[15:8]) is forced low. In quad Drop bus interface STS-3(STM-1) mode, the Drop bus data (DD[15:8]) contains the channel two STS-3/3c (STM-1/AU-3/AU-4) received SONET/SDH payload data. When the Drop bus TSI functionality is disabled, the Dropped payload corresponds to the SONET/SDH data received on channel #2. TSI may be used to reorder this multiplexing on the Drop bus. STS-1/STM-1(AU3)'s within a channel or between channels, along with entire channels may be swapped. The transport overhead bytes, with the exception of the H1, H2 pointer bytes and when there are no negative pointer justifications the H3, are set to zeros. The fixed framing patterns for the A1 and A2 framing bytes may be inserted. The GEN_A1A2_EN bit in the DPGM Generator Control #1 register enables insertion of the A1 and A2 framing bytes. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. The H4BYP and CLRFS bits in the RTAL Control register control the insertion of the H4 byte and the value of the fixed stuff columns. DD[15] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DD[8] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DD[15:8] is updated on the rising edge of DCK. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register.
DD[16] DD[17] DD[18] DD[19] DD[20] DD[21] DD[22] DD[23]	Output	W27 Y31 Y30 Y29 Y28 Y27 AA30 AA29	In single Drop bus interface mode, the Drop bus data (DD[23:16]) is forced low. In quad bus interface STS-3(STM-1) mode, the Drop bus data (DD[15:8]) contains the channel three STS-3/3c (STM-1/AU-3/AU-4) received SONET/SDH payload data. When the Drop bus TSI functionality is disabled, the Dropped payload corresponds to the SONET/SDH data received on channel #3. TSI may be used to reorder this multiplexing on the Drop bus. STS-1/STM-1(AU3)'s within a channel or between channels, along with entire channels may be swapped. The transport overhead bytes, with the exception of the H1, H2 pointer bytes and when there are no negative pointer justifications the H3, are set to zeros. The fixed framing patterns for the A1 and A2 framing bytes may be inserted. The GEN_A1A2_EN bit in the DPGM Generator Control #1 register enables insertion of the A1 and A2 framing bytes. The H4 byte may also be inserted. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. The H4BYP and CLRFS bits in the RTAL Control register control the insertion of the H4 byte and the value of the fixed stuff columns. DD[23] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DD[16] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DD[23:16] is updated on the rising edge of DCK. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register.
DD[24]	Output	AE31	In single Drop bus interface mode, the Drop bus data

Pin Name	Pin Type	Pin No.	Function
DD[25] DD[26] DD[27] DD[28] DD[29] DD[30] DD[31]		AE30 AE29 AE28 AE27 AF30 AF29 AG31	(DD[31:24]) is forced low. In quad bus interface STS-3(STM-1) mode, the Drop bus data (DD[31:24]) contains the channel four STS-3/3c (STM-1/AU-3/AU-4) received SONET/SDH payload data. When the Drop bus TSI functionality is disabled, the Dropped payload corresponds to SONET/SDH data received on channel #4. TSI may be used to reorder this multiplexing on the Drop bus. STS-1/STM-1(AU3)'s within a channel or between channels, along with entire channels may be swapped. The transport overhead bytes, with the exception of the H1, H2 pointer bytes and when there are no negative pointer justifications the H3, are set to zeros. The fixed framing patterns for the A1 and A2 framing bytes may be inserted. The GEN_A1A2_EN bit in the DPGM Generator Control #1 register enables insertion of the A1 and A2 framing bytes. The H4 byte may also be inserted. The fixed stuff columns in a tributary mapped SPE (VC) may also be optionally set to zero or NPI. The H4BYP and CLRFS bits in the RTAL Control register control the insertion of the H4 byte and the value of the fixed stuff columns. DD[31] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). DD[24] is the least significant bit (corresponding to bit 8 of each serial word, the last bit received). DD[31:24] is updated on the rising edge of DCK. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register.
DPL[1]	Output	H31	The active high Drop bus payload active signal #1 (DPL[1]) indicates when the DD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL[1] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. DPL[1] is updated on the rising edge of DCK. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register.
DPL[2]	Output	N31	The active high Drop bus payload active signal #2 (DPL[2]) indicates when the DD[15:8] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL[2] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. DPL[2] is updated on the rising edge of DCK. This output is forced low in single Drop bus mode. The Drop interface mode is set via the DTMODE register bits in the Drop Bus Configuration register.
DPL[3]	Output	W29	The active high Drop bus payload active signal #3 (DPL[3]) indicates when the DD[23:16] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL[3] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event.

Pin Name	Pin Type	Pin No.	Function
			DPL[3] is updated on the rising edge of DCK. This output is forced low in single Drop bus mode. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register.
DPL[4]	Output	AD28	The active high Drop bus payload active signal #4 (DPL[4]) indicates when the DD[31:24] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. DPL[4] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. DPL[4] is updated on the rising edge of DCK. This output is forced low in single Drop bus mode. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register.
DC1J1V1[1]	Output	H30	The Drop bus composite timing signal #1 (DC1J1V1[1]) indicates the frame, payload and tributary multi-frame boundaries on the Drop data bus signals DD[7:0]. DC1J1V1[1] pulses high with the Drop bus payload active signal (DPL[1]) set low to mark the first STS-1 (STM-0/AU-3) Identification byte or equivalently the STM identification byte (C1). DC1J1V1[1] pulses high with DPL[1] set high to mark the path trace byte (J1). Optionally, the DC1J1V1[1] signal pulses high on the V1 byte to indicate tributary multi-frame boundaries using the ENDV1 bit in the SPECTRA 4x155 RPPS Path Configuration register. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register. DC1J1V1[1] is updated on the rising edge of DCK.
DC1J1V1[2]	Output	N30	The Drop bus composite timing signal #2 (DC1J1V1[2]) indicates the frame, payload and tributary multi-frame boundaries on the Drop data bus signals DD[15:8]. DC1J1V1[2] pulses high with the Drop bus payload active signal (DPL[2]) set low to mark the first STS-1 (STM-0/AU-3) Identification byte or equivalently the STM identification byte (C1). DC1J1V1[2] pulses high with DPL[2] set high to mark the path trace byte (J1). Optionally, the DC1J1V1[2] signal pulses high on the V1 byte to indicate tributary multi-frame boundaries using the ENDV1 bit in the SPECTRA 4x155 RPPS Path Configuration register. This output is forced low in single Drop bus mode. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register. DC1J1V1[2] is updated on the rising edge of DCK.
DC1J1V1[3]	Output	W28	The Drop bus composite timing signal #3 (DC1J1V1[3]) indicates the frame, payload and tributary multi-frame boundaries on the Drop data bus signals DD[23:16]. DC1J1V1[3] pulses high with the Drop bus payload active signal (DPL[3]) set low to mark the first STS-1 (STM-0/AU-3) Identification byte or equivalently the STM identification byte (C1). DC1J1V1[3] pulses high with DPL[3] set high to mark the path trace byte (J1). Optionally, the DC1J1V1[3] signal pulses high on the V1 byte to indicate tributary multi-frame boundaries using the ENDV1 bit in the SPECTRA 4x155 RPPS Path Configuration register. This output is forced low in single Drop

Pin Name	Pin Type	Pin No.	Function
			bus mode. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register. DC1J1V1[3] is updated on the rising edge of DCK.
DC1J1V1[4]	Output	AD27	The Drop bus composite timing signal #4 (DC1J1V1[4]) indicates the frame, payload and tributary multi-frame boundaries on the Drop data bus signals DD[31:24]. DC1J1V1[4] pulses high with the Drop bus payload active signal (DPL[4]) set low to mark the first STS-1 (STM-0/AU-3) Identification byte or equivalently the STM identification byte (C1). DC1J1V1[4] pulses high with DPL[4] set high to mark the path trace byte (J1). Optionally, the DC1J1V1[4] signal pulses high on the V1 byte to indicate tributary multi-frame boundaries using the ENDV1 bit in the SPECTRA 4x155 RPPS Path Configuration register. This output is forced low in single Drop bus mode. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register. DC1J1V1[4] is updated on the rising edge of DCK.
DDP[1]	Output	K31	The Drop bus data parity signal #1 (DDP[1]) indicates the parity of the Drop bus signals. The Drop data bus signals (DD[7:0]) are always included in parity calculations. Register bits in the Drop Bus Configuration register control the inclusion of the DPL[1] and DC1J1V1[1] signals in parity calculation and the sense (odd/even) of the parity. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register. DDP[1] is updated on the rising edge of DCK.
DDP[2]	Output	R28	The Drop bus data parity signal #2 (DDP[2]) indicates the parity of the Drop bus signals. The Drop data bus signals (DD[15:8]) are always included in parity calculations. Register bits in the Drop Bus Configuration register control the inclusion of the DPL[2] and DC1J1V1[2] signals in parity calculation and the sense (odd/even) of the parity. This output is forced low in single Drop bus mode. The Drop interface mode is set via the DTMODE register bit in the Drop Bus Configuration register. DDP[2] is updated on the rising edge of DCK.
DDP[3]	Output	AA28	The Drop bus data parity signal #3 (DDP[3]) indicates the parity of the Drop bus signals. The Drop data bus signals (DD[23:16]) are always included in parity calculations. Register bits in the Drop Bus Configuration register control the inclusion of the DPL[3] and DC1J1V1[3] signals in parity calculation and the sense (odd/even) of the parity. This output is forced low in single Drop bus mode. The Drop interface mode is set via DTMODE register bit in the Drop Bus Configuration register. DDP[3] is updated on the rising edge of DCK.
DDP[4]	Output	AF28	The Drop bus data parity signal #4 (DDP[4]) indicates the parity of the Drop bus signals. The Drop data bus signals (DD[31:24]) are always included in parity calculations. Register bits in the Drop Bus Configuration register control the inclusion of the DPL[4] and DC1J1V1[4] signals in parity calculation and the sense (odd/even) of the parity. This output is forced low single Drop bus mode. The Drop interface mode is set via DTMODE register bit in the Drop Bus Configuration register.

Pin Name	Pin Type	Pin No.	Function
			DDP[4] is updated on the rising edge of DCK.

9.9 Add Bus Telecom Interface Signals

Pin Name	Pin Type	Pin No.	Function
ACK	Input	E31	The Add bus clock (ACK) provides timing for the Add bus interface. ACK is nominally a 77.76 MHz, 50% duty cycle clock when the Add interface is configured as a single bus interface. ACK is nominally a 19.44 MHz, 50% duty cycle clock when the Add interface is configured as a quad STS-3 (STM-1) interface. Inputs AD[31:0], APL[4:1], ADP[4:1], and AC1J1V1[4:1]/AFP[4:1] are sampled on the rising edge of ACK.
AD[0] AD[1] AD[2] AD[3] AD[4] AD[5] AD[6] AD[7]	Input	E28 F30 F29 F28 F27 G31 G30 G29	In single Add bus interface mode, the Add bus data (AD[7:0]) contains the STS-3/c(STM-1/AU-3/AU-4) SONET/SDH payload data to transmit on the four channels. In quad Add bus interface STS-3 (STM-1) mode, the Add bus data (AD[7:0]) contains the 1st STS-3/3c (STM-1/AU-3/AU-4) SONET/SDH payload data to transmit. When Add bus TSI functionality is disabled, the SONET/SDH payload data provided on AD[7:0] will be transmitted on channel #1. When Add bus TSI functionality is enabled, the association of Add bus payloads to the transmitted payloads is software configurable in the SPECTRA 4x155 Add Bus STM-1 #1..4 AU-3 #1..3 Select registers. The Add bus transport overhead bytes are ignored with the programmable exception of the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame is determined by the Add bus composite timing signal (AC1J1V1[1]) or optionally by interpreting the H1 and H2 pointer bytes. AD[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD[7:0] is sampled on the rising edge of ACK. The Add interface mode is set via ATMODE register bit in the Add Bus Configuration register.
AD[8] AD[9] AD[10] AD[11] AD[12] AD[13] AD[14] AD[15]	Input	K28 K27 L30 L29 L28 M31 M30 M29	In single Add bus interface mode, the Add bus data (AD[15:8]) is disabled. In quad Add bus interface STS-3 (STM-1) mode, the Add bus data (AD[15:8]) contains the 2nd STS-3/3c (STM-1/AU-3/AU-4) SONET/SDH payload data to transmit. When Add bus TSI functionality is enabled, the association of Add bus payloads to the transmitted payloads is software configurable in the SPECTRA 4x155 Add Bus STM-1 #1..4 AU-3 #1..3 Select registers. The Add bus transport overhead bytes are ignored with the programmable exception of the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame is determined by the Add bus composite timing signal (AC1J1V1[2]) or optionally by interpreting the H1 and H2 pointer bytes. AD[15] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[8] is the least significant bit (corresponding to

Pin Name	Pin Type	Pin No.	Function
			bit 8 of each serial word, the last bit transmitted). AD[15:8] is sampled on the rising edge of ACK. The Add interface mode is set via ATMODE register bit in the Add Bus Configuration register.
AD[16] AD[17] AD[18] AD[19] AD[20] AD[21] AD[22] AD[23]	Input	U29 U28 U27 V31 V30 V29 V28 V27	In single Add bus interface mode, the Add bus data (AD[23:16]) is disabled. In quad Add bus interface STS-3 (STM-1) mode, the Add bus data (AD[23:16]) contains the 3rd STS-3/3c (STM-1/AU-3/AU-4) SONET/SDH payload data to transmit. When Add bus TSI functionality is enabled, the association of Add bus payloads to the transmitted payloads is software configurable in the SPECTRA 4x155 Add Bus STM-1 #1..4 AU-3 #1..3 Select registers. The Add bus transport overhead bytes are ignored with the programmable exception of the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame is determined by the Add bus composite timing signal (AC1J1V1[3]) or optionally by interpreting the H1 and H2 pointer bytes. AD[23] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[16] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD[23:16] is sampled on the rising edge of ACK. The Add interface mode is set via ATMODE register bit in the Add Bus Configuration register.
AD[24] AD[25] AD[26] AD[27] AD[28] AD[29] AD[30] AD[31]	Input	AB29 AB28 AB27 AC31 AC30 AC29 AC28 AD31	In single Add bus interface mode, the Add bus data (AD[31:24]) is disabled. In quad Add bus interface STS-3 (STM-1) mode, the Add bus data (AD[31:24]) contains the 4th STS-3/3c (STM-1/AU-3/AU-4) SONET/SDH payload data to transmit. When Add bus TSI functionality is enabled, the association of Add bus payloads to the transmitted payloads is software configurable in the SPECTRA 4x155 Add Bus STM-1 #1..4 AU-3 #1..3 Select registers. The Add bus transport overhead bytes are ignored with the programmable exception of the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame is determined by the Add bus composite timing signal (AC1J1V1[4]) or optionally by interpreting the H1 and H2 pointer bytes. AD[31] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). AD[24] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). AD[31:24] is sampled on the rising edge of ACK. The Add interface mode is set via ATMODE register bit in the Add Bus Configuration register.
APL[1]	Input	E30	The Add bus payload active signal #1 (APL[1]) indicates when AD[7:0] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL[1] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. The APL[1] input must be strapped low when the AFPEN bit in the Add Bus Configuration register is set high. The INCAPL bit in the Add Bus Configuration #1 register controls whether APL[1] is to be included in the Add

Pin Name	Pin Type	Pin No.	Function
			Bus parity ADP[1] or the activity monitor. APL[1] is sampled on the rising edge of ACK.
APL[2]	Input	K30	The Add bus payload active signal #2 (APL[2]) indicates when AD[15:8] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL[2] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. The APL[2] input must be strapped low when the AFPEN bit in the Add Bus Configuration register is set high. The INCAPL bit in the Add Bus Configuration #1 register controls whether APL[2] is to be included in the Add Bus parity ADP[2] or the activity monitor. APL[2] is sampled on the rising edge of ACK.
APL[3]	Input	U31	The Add bus payload active signal #3 (APL[3]) indicates when AD[23:16] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL[3] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. The APL[3] input must be strapped low when the AFPEN bit in the Add Bus Configuration register is set high. The INCAPL bit in the Add Bus Configuration #1 register controls whether APL[3] is to be included in the Add Bus parity ADP[3] or the activity monitor. APL[3] is sampled on the rising edge of ACK.
APL[4]	Input	AB31	The Add bus payload active signal #4 (APL[4]) indicates when AD[31:24] is carrying a payload byte. It is set high during path overhead and payload bytes and low during transport overhead bytes. APL[4] is set high during the H3 byte to indicate a negative pointer justification event and set low during the byte following H3 to indicate a positive pointer justification event. The APL[4] input must be strapped low when the AFPEN bit in the Add Bus Configuration register is set high. The INCAPL bit in the Add Bus Configuration #1 register controls whether APL[4] is to be included in the Add Bus parity ADP[4] or the activity monitor. APL[4] is sampled on the rising edge of ACK.
AC1J1V1[1]/	Input	E29	The Add bus composite timing signal #1 (AC1J1V1[1]) is defined when the AFPEN bit in the Add Bus Configuration register is set low. AC1J1V1[1] identifies the frame and optionally the payload and tributary multi-frame boundaries on the Add data bus signals AD[7:0]. AC1J1V1[1] pulses high with the Add bus payload active signal #1 (APL[1]) set low to mark the first STS-1 (STM-0/AU-3) Identification byte (C1). Optionally, the AC1J1V1[1] pulses high with APL[1] set high to mark the path trace byte (J1). Optionally, the AC1J1V1[1] signal pulses high on the V1 byte to indicate tributary multi-frame boundaries. Optional marking of the J1 and V1 bytes is controlled using the DISJ1V1 bit in the SPECTRA 4x155 TPPS Path Configuration register. Setting DISJ1V1 bit high enables pointer

Pin Name	Pin Type	Pin No.	Function
			interpretation on the Add bus. Valid H1 and H2 pointer bytes must be provided on the Add data bus signals (AD[7:0]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the Add data bus signals (AD[7:0]) to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] Add buses must be frame aligned with the C1 pulses of the associated AC1J1V1 signals. All C1 pulses must be aligned. If the AC1J1V1[1] frame alignment changes, all the slices are affected by the realignment. Errors may occur in some or all slices and the APGMs need to be manually regenerated or resynchronized if used. The ATSI_ISOLATE bit can be used to disable the realignment of the 12 TPPS slice clocks by AC1J1V1/AFP[1] Add BUS. This bit should only be used when all 12 TPPS slices are placed in Autonomous mode and the AC1J1V1/AFP[1] (and/or APL) Add BUS interface cannot maintain a constant frame alignment. AC1J1V1[1] is sampled on the rising edge of ACK.
AFP[1]		E29	The active high Add bus reference frame position signal #1 (AFP[1]) is defined when the AFPEN bit in the Add Bus Configuration register is set high. AFP[1] indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) of the SONET/SDH stream is available on the AD[7:0] bus. Note that AFP[1] has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to AFP[1]. The DISJ1V1 bit in the SPECTRA 4x155 TPPS Path Configuration register must be set high in this mode to enable pointer interpretation on the Add bus. Valid H1 and H2 pointer bytes must be provided on the Add data bus (AD[7:0]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the Add data bus to allow the V1 position to be identified. The AD[7:0], AD[15:8], AD[23:16] and AD[31:24] Add buses must be frame aligned with the C1 pulses of the associated AC1J1V1 signals. All C1 pulses must be aligned. If the AC1J1V1[1] frame alignment changes, all the slices are affected by the realignment. Errors may occur in some or all slices and the APGMs need to be manually regenerated or resynchronized if used. The ATSI_ISOLATE bit can be used to disable the realignment of the 12 TPPS slice clocks by AC1J1V1/AFP[1] Add BUS. This bit should only be used when all 12 TPPS slices are placed in Autonomous mode and the AC1J1V1/AFP[1] (and/or APL) Add BUS interface cannot maintain a constant frame alignment. AFP[1] is sampled on the rising edge of ACK.
AC1J1V1[2]/	Input	K29	The Add bus composite timing signal #2 (AC1J1V1[2]) is defined when the AFPEN bit in the Add Bus Configuration register is set low. AC1J1V1[2] identifies the frame and optionally the payload and tributary multi-frame boundaries on

Pin Name	Pin Type	Pin No.	Function
			the Add data bus signals AD[15:8]. AC1J1V1[2] pulses high with the Add bus payload active signal #2 (APL[2]) set low to mark the first STS-1 (STM-0/AU-3) Identification byte (C1). Optionally, the AC1J1V1[2] pulses high with APL[2] set high to mark the path trace byte (J1). Optionally, the AC1J1V1[2] signal pulses high on the V1 byte to indicate tributary multi-frame boundaries. Optional marking of the J1 and V1 bytes is controlled using the DISJ1V1 bit in the SPECTRA 4x155 TPPS Path Configuration register. Setting DISJ1V1 bit high enables pointer interpretation on the Add bus. Valid H1 and H2 pointer bytes must be provided on the Add data bus signals (AD[15:8]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the Add data bus signals (AD[15:8]) to allow the V1 position to be identified. When using the Add bus TSI functionality, the AD[7:0], AD[15:8], AD[23:16] and AD[31:24] Add buses must be frame aligned to have the C1 pulses of the associated AC1J1V1 signals high simultaneously. AC1J1V1[2] is sampled on the rising edge of ACK.
AFP[2]		K29	The active high Add bus reference frame position signal #2 (AFP[2]) is defined when the AFPEN bit in the Add Bus Configuration register is set high. AFP[2] indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) of the SONET/SDH stream is available on the AD[15:8] bus. Note that AFP[2] has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to AFP[2]. The DISJ1V1 bit in the SPECTRA 4x155 TPPS Path Configuration register must be set high in this mode to enable pointer interpretation on the Add bus. Valid H1 and H2 pointer bytes must be provided on the Add data bus (AD[15:8]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the Add data bus to allow the V1 position to be identified. When using the Add bus TSI functionality, the AD[7:0], AD[15:8], AD[23:16] and AD[31:24] Add buses must be frame aligned to have the C1 pulses of the associated AC1J1V1 signals high simultaneously. AFP[2] is sampled on the rising edge of ACK.
AC1J1V1[3]/	Input	U30	The Add bus composite timing signal #3 (AC1J1V1[3]) is defined when the AFPEN bit in the Add Bus Configuration register is set low. AC1J1V1[3] identifies the frame and optionally the payload and tributary multi-frame boundaries on the Add data bus signals AD[23:16]. AC1J1V1[3] pulses high with the Add bus payload active signal #3 (APL[3]) set low to mark the first STS-1 (STM-0/AU-3) Identification byte (C1). Optionally, the AC1J1V1[3] pulses high with APL[3] set high to mark the path trace byte (J1). Optionally, the AC1J1V1[3] signal pulses high on the V1 byte to indicate tributary multi-frame boundaries. Optional marking of the J1 and V1 bytes is controlled using the DISJ1V1 bit in the TPPS Path Configuration register. Setting

Pin Name	Pin Type	Pin No.	Function
			DISJ1V1 bit high enables pointer interpretation on the Add bus. Valid H1 and H2 pointer bytes must be provided on the Add data bus signals (AD[23:16]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the Add data bus signals (AD[23:16]) to allow the V1 position to be identified. When using the Add bus TSI functionality, the AD[7:0], AD[15:8], AD[23:16] and AD[31:24] Add buses must be frame aligned to have the C1 pulses of the associated AC1J1V1 signals high simultaneously. AC1J1V1[3] is sampled on the rising edge of ACK.
AFP[3]		U30	The active high Add bus reference frame position signal #3 (AFP[3]) is defined when the AFPEN bit in the Add Bus Configuration register is set high. AFP[3] indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) of the SONET/SDH stream is available on the AD[31:24] bus. Note that AFP[3] has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to AFP[3]. The DISJ1V1 bit in the SPECTRA 4x155 TPPS Path Configuration register must be set high in this mode to enable pointer interpretation on the Add bus. Valid H1 and H2 pointer bytes must be provided on the Add data bus (AD[23:16]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the Add data bus to allow the V1 position to be identified. When using the Add bus TSI functionality, the AD[7:0], AD[15:8], AD[23:16] and AD[31:24] Add buses must be frame aligned to have the C1 pulses of the associated AC1J1V1 signals high simultaneously. AFP[3] is sampled on the rising edge of ACK.
AC1J1V1[4]/	Input	AB30	The Add bus composite timing signal #4 (AC1J1V1[4]) is defined when the AFPEN bit in the Add Bus Configuration is set low. AC1J1V1[4] identifies the frame and optionally the payload and tributary multi-frame boundaries on the Add data bus signals AD[31:24]. AC1J1V1[4] pulses high with the Add bus payload active signal #4 (APL[1]) set low to mark the first STS-1 (STM-0/AU-3) Identification byte (C1). Optionally, the AC1J1V1[4] pulses high with APL[4] set high to mark the path trace byte (J1). Optionally, the AC1J1V1[4] signal pulses high on the V1 byte to indicate tributary multi-frame boundaries. Optional marking of the J1 and V1 bytes is controlled using the DISJ1V1 bit in the TPPS Path Configuration register. Setting DISJ1V1 bit high enables pointer interpretation on the Add bus. Valid H1 and H2 pointer bytes must be provided on the Add data bus signals (AD[31:24]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the Add data bus signals (AD[31:24]) to allow the V1 position to be identified. When using the Add bus TSI functionality, the AD[7:0], AD[15:8], AD[23:16] and AD[31:24] Add buses must be frame aligned to have the C1 pulses of the associated AC1J1V1 signals high simultaneously.

Pin Name	Pin Type	Pin No.	Function
			AC1J1V1[4] is sampled on the rising edge of ACK.
AFP[4]		AB30	The active high Add bus reference frame position signal #4 (AFP[4]) is defined when the AFPEN bit in the Add Bus Configuration is set high. AFP[4] indicates when the first byte of the synchronous payload envelope (SPE byte 1 of STS-1 #1) of the SONET/SDH stream is available on the AD[31:24] bus. Note that AFP[4] has a fixed relationship to the SONET/SDH frame; the start of the SPE is determined by the STS (AU) pointer and may change relative to AFP[4]. The DISJ1V1 bit in the TPPS Path Configuration register must be set high in this mode to enable pointer interpretation on the Add bus. Valid H1 and H2 pointer bytes must be provided on the Add data bus (AD[31:24]) to allow the J1 position to be identified. Optionally, the H4 byte could be provided on the Add data bus to allow the V1 position to be identified. When using the Add bus TSI functionality, the AD[7:0], AD[15:8], AD[23:16] and AD[31:24] Add buses must be frame aligned to have the C1 pulses of the associated AC1J1V1 signals high simultaneously. AFP[4] is sampled on the rising edge of ACK.
ADP[1]	Input	G28	The Add bus data parity signal #1 (ADP[1]) indicates the parity of the Add bus #1 signals. The Add data bus (AD[7:0]) is always included in parity calculations. Register bits in the Add Bus Configuration register control the inclusion of the APL[1] and AC1J1V1[1]/AFP[1] signals in parity calculations and the sense (odd/even) of the parity. ADP[1] is sampled on the rising edge of ACK.
ADP[2]	Input	M28	The Add bus data parity signal #2 (ADP[2]) indicates the parity of the Add bus #2 signals. The Add data bus (AD[15:8]) is always included in parity calculations. Register bits in the Add Bus Configuration register control the inclusion of the APL[2] and AC1J1V1[2]/AFP[2] signals in parity calculations and the sense (odd/even) of the parity. ADP[2] is sampled on the rising edge of ACK.
ADP[3]	Input	W31	The Add bus data parity signal #3 (ADP[3]) indicates the parity of the Add bus #3 signals. The Add data bus (AD[23:16]) is always included in parity calculations. Register bits in the Add Bus Configuration register control the inclusion of the APL[3] and AC1J1V1[3]/AFP[3] signals in parity calculations and the sense (odd/even) of the parity. ADP[3] is sampled on the rising edge of ACK.
ADP[4]	Input	AD30	The Add bus data parity signal #4 (ADP[4]) indicates the parity of the Add bus #4 signals. The Add data bus (AD[31:24]) is always included in parity calculations. Register bits in the Add Bus Configuration register control the inclusion of the APL[4] and AC1J1V1[4]/AFP[4] signals in parity calculations and the sense (odd/even) of the parity. ADP[4] is sampled on the rising edge of ACK.

9.10 Microprocessor Interface Signals

Pin Name	Type	Pin No.	Function
MBEB	Input	C14	The active low Motorola bus enable (MBEB) signal configures the SPECTRA 4x155 for Motorola bus mode where the RDB/E signal functions as E, and the WRB/RWB signal functions as RWB. When MBEB is high, the SPECTRA 4x155 is configured for Intel bus mode where the RDB/E signal functions as RDB. The MBEB input has an integral pull up resistor.
CSB	Schmidt TTL Input	E15	The active low chip select (CSB) signal is low during SPECTRA 4x155 register accesses. Note that when not being used, CSB must be tied low. If CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB/	Input	B14	The active low read enable (RDB) signal is low during a SPECTRA 4x155 read access. The SPECTRA 4x155 drives the D[7:0] bus with the contents of the Addressed register while RDB and CSB are low.
E		B14	The active high external access signal (E) is set high during SPECTRA 4x155 register access while in Motorola bus mode.
WRB/	Input	D14	The active low write strobe (WRB) signal is low during a SPECTRA 4x155 register write access. The D[7:0] bus contents are clocked into the Addressed register on the rising WRB edge while CSB is low.
RWB		D14	The read/write select signal (RWB) selects between SPECTRA 4x155 register read and write accesses while in Motorola bus mode. The SPECTRA 4x155 drives the data bus D[7:0] with the contents of the Addressed register while CSB is low and RWB and E are high. The contents of D[7:0] are clocked into the Addressed register on the falling E edge while CSB and RWB are low.
D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	D20 C20 B20 A20 E19 D19 C19 B19	The bi-directional data bus, D[7:0], is used during SPECTRA 4x155 read and write accesses.
A[13]	Input	E18	The test register select signal (A[13]) selects between normal and test mode register accesses. A[13] is high during test mode register accesses, and is low during normal mode register accesses. A[13] may be tied low.
A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4]	Input	C18 D18 B18 A18 E17 D17 C17 B17 A17	The Address bus (A[13:0]) selects specific registers during SPECTRA 4x155 register accesses.

Pin Name	Type	Pin No.	Function
A[3] A[2] A[1] A[0]		A15 C15 B15 D15	
RSTB	Schmidt TTL Input	E14	The active low reset (RSTB) signal provides an asynchronous SPECTRA 4x155 reset. RSTB is a Schmidt triggered input with an integral pull-up resistor.
ALE	Input	A14	The Address latch enable (ALE) is an active-high signal and latches the Address bus A[13:0] when low. When ALE is high, the internal Address latches are transparent. It allows the SPECTRA 4x155 to interface to a multiplexed Address/data bus. The ALE input has an integral pull up resistor.
INTB	OD Output	A19	The active low interrupt (INTB) is set low when a SPECTRA 4x155 enabled interrupt source is active. The SPECTRA 4x155 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. INTB is an open drain output.

9.11 Analog Miscellaneous Signals

Pin Name	Type	Pin No.	Function
ATP[0] ATP[1] ATP[2] ATP[3]	Analog	V3 V4 W1 V5	Four analog test ports (ATP0, ATP1, ATP2, ATP3) are provided for production testing only. These pins must be tied to analog ground (AVS) during normal operation.

9.12 JTAG Test Access Port (TAP) Signals

Pin Name	Type	Pin No.	Function
TCK	Schmidt TTL Input	AK4	The test clock (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	AG6	The test mode select (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	AK5	When the SPECTRA 4x155 is configured for JTAG operation, the test data input (TDI) signal carries test data into the SPECTRA 4x155 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.
TDO	Tristate Output	AH6	The test data output (TDO) signal carries test data out of the SPECTRA 4x155 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output that is inactive except when scanning of data is in progress.
TRSTB	Schmidt TTL Input	AJ5	The active low test reset (TRSTB) signal provides an asynchronous SPECTRA 4x155 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmidt triggered input with an integral pull up resistor. In the event that TRSTB

			is not used, it must be connected to RSTB.

9.13 Power and Ground

Pin Name	Pin Type	PIN No.	Function
Reserved1	Output	D25	This output can be left floating.
Reserved2	Output	C25	This output can be left floating.
Reserved3	Input	A25	This input pin must be grounded.
Reserved4	Input	E24	This input pin must be grounded.
Reserved5	Output	B25	This output can be left floating
VBIAS[0] VBIAS[1]	Bias Voltage	AK28 E20	Digital input biases. When tied to +5V, the VBIAS[1:0] inputs are used to bias the wells of the digital inputs so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. When VBIAS is tied to +3.3V, the digital inputs will only tolerate 3.3V level voltages.
AVD	Analog Power	L4 G4 H3 M4 N1 P4 Y4 U1 V1 AB5 AD4 AC3 R4 R2 G5 AD5	RAVD1_A - Channel #1 PECL Input Buffer RAVD1_B – Channel #1 CRU RAVD1_C – Channel #1 CRU RAVD2_A – Channel #2 PECL Input Buffer RAVD2_B – Channel #2 CRU RAVD2_C – Channel #2 CRU RAVD3_A – Channel #3 PECL Input Buffer RAVD3_B – Channel #3 CRU RAVD3_C – Channel #3 CRU RAVD4_A – Channel #4 PECL Input Buffer RAVD4_B – Channel #4 CRU RAVD4_C – Channel #4 CRU TAVD1_A – CSU TAVD1_B – CSU QAVD2 QAVD1 The analog power (AVD) pins for the analog core. The AVD pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.
AVS	Analog Ground	K1 H5 H4 M5 N4 P5 Y5 U4 V2 AB4 AC5 AC4 R3 R1 F2 AE1	RAVS1_A - Channel #1 PECL Input Buffer RAVS1_B - Channel #1 CRU RAVS1_C - Channel #1 CRU RAVS2_A - Channel #2 PECL Input Buffer RAVS2_B - Channel #2 CRU RAVS2_C - Channel #2 CRU RAVS3_A - Channel #3 PECL Input Buffer RAVS3_B - Channel #3 CRU RAVS3_C - Channel #3 CRU RAVS4_A - Channel #4 PECL Input Buffer RAVS4_B - Channel #4 CRU RAVS4_C - Channel #4 CRU TAVS1_A – CSU TAVS1_B – CSU QAVS1 QAVS2 The analog ground (AVS) pins for the analog core. The AVS

Pin Name	Pin Type	PIN No.	Function
			pins should be connected to the analog ground of the analog power supply. Please see the Operation section for detailed information.
VDD	Digital Power	The digital power (VDD) pins should be connected to a well-decoupled +3.3 V digital power supply. A1, A31, B2, B30, C3, C4, C16, C28, C29, D3, D4, D16, D28, D29, E5, E11, E16, E21, E27, L5, L27, T3, T4, T5, T27, T28, T29, AA5, AA27, AG5, AG11, AG16, AG21, AG27, AH3, AH4, AH16, AH28, AH29, AJ3, AJ4, AJ16, AJ28, AJ29, AK2, AK30, AL1, AL31	
VSS	Digital Ground	The digital ground (VSS) pins should be connected to the digital ground of the digital power supply. A2, A3, A4, A6, A11, A16, A21, A26, A28, A29, A30, B1, B3, B16, B29, B31, C1, C2, C30, C31, D1, D31, F1, F31, L1, L31, T1, T2, T30, T31, AA1, AA31, AF1, AF31, AH1, AH31, AJ1, AJ2, AJ30, AJ31, AK1, AK3, AK16, AK29, AK31, AL2, AL3, AL4, AL6, AL11, AL16, AL21, AL26, AL28, AL29, AL30	

Notes on Pin Description:

1. All SPECTRA 4x155 inputs and bi-directional pins present minimum capacitive loading and operate at TTL logic levels except the SD and RXD± inputs, which operate at pseudo-ECL (PECL) logic levels.
2. The SPECTRA 4x155 digital outputs and bi-directionals that have a 2 mA drive capability are: D[7:0], B3E, INTB, LOF1-4, LAIS/RRCPDAT1-4, LRDI/RRCPCLK1-4, LOS/RRCPFP1-4, RTOH1-4, RTOHCLK1-4, RTOHFP1-4, RSLD1-4, RSLDCLK1-4, RAD, RALM, RPOH, RPOHCLK, RPOHEN, RPOHFP, SALM1-4, TDO, Reserved1, Reserved2, Reserved5, TSLDCLK1-4, TTOHCLK1-4, TTOHFP1-4.
3. The SPECTRA 4x155 digital outputs and bi-directionals that have a 6 mA drive capability are: DC1JV1[4:1], DD[31:0], DDP[4:1], DPL[4:1], PGMRCLK, PGMTCLK, RCLK1-4, TCLK.
4. The SPECTRA 4x155 digital outputs that are not 5 volt tolerant are: DC1JV1[4:1], DD[31:0], DDP[4:1], DPL[4:1], PGMRCLK, PGMTCLK, RCLK1-4, TCLK. All other outputs are 5 volt tolerant.
5. The inputs ALE, MBEB, RSTB, TMS, TDI, and TRSTB have internal pull-up resistors.
6. The differential pseudo-ECL inputs and outputs should be terminated in a passive network and interface at PECL levels as described in the Operations section.
7. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.
8. It is mandatory that every digital power pin (VDD) be connected to the printed circuit board power plane to ensure reliable device operation.
9. All analog power ~~and ground~~ pins can be sensitive to noise. They must be isolated from the digital power ~~and ground~~. Care must be taken to correctly decouple these pins. Please refer to the Operations sections
10. Due to ESD protection structures in the pads, caution must be taken when powering the device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing described in the Operation section of this document.
11. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operations section.
12. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

13. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.
14. Ensure that all digital power is applied simultaneously, and applied before or simultaneously with the analog power. Refer to the Power Sequencing description in the Operations section.

10 Functional Description

10.1 Receive Line Interface and CRSI

The Receive Line Interface and the Clock Recover/Serial-to-Parallel Converter (CRSI) blocks perform PECL conversion, clock and data recovery on the incoming 155.52 Mbit/s data stream, and serial-to-parallel conversion based on the recovered SONET/SDH A1/A2 framing pattern. The blocks allow the SPECTRA 4x155 to directly interface with optical modules (ODLs) or other medium interfaces.

10.1.1 Clock Recovery Unit (CRU)

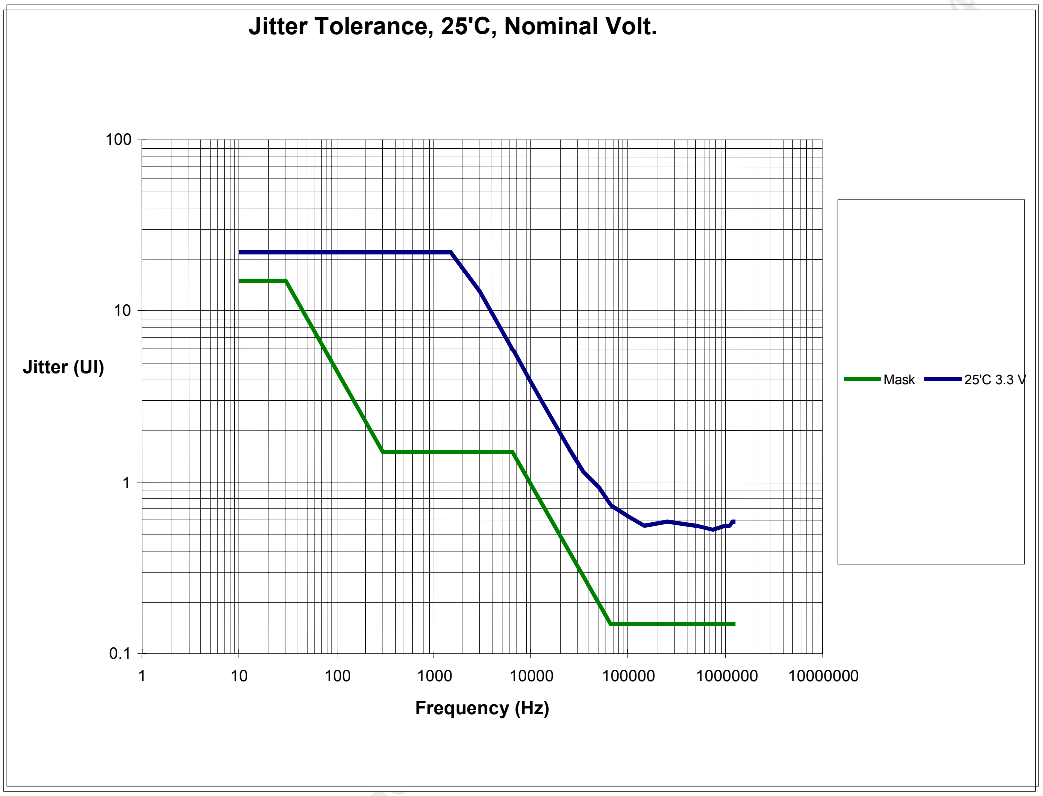
The clock recovery unit (CRU) inside the CRSI block recovers a clock from the incoming bit serial data stream. The CRU is fully compliant with SONET/SDH jitter tolerance requirements. It uses a low frequency 19.44 MHz reference clock to train and monitor its clock recovery phase-locked loop (PLL). Under LOS conditions, the CRU will continue to output a line rate clock that is locked to this reference for keep-alive purposes. As part of its feature set, the CRU provides status bits that indicate whether it is locked to data or to the reference clock. The unit also supports diagnostic loop back and a LOS input that squelches normal input data.

Initially, the PLL locks to the reference clock, REFCLK. Once the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL will revert to the reference clock if no data transitions occur in 80 bit periods or if the recovered clock drifts beyond approximately 488 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the REFCLK reference accuracy under LOS conditions. In applications that are required to meet the Telcordia GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-20 ppm. When not loop timed, the REFCLK accuracy may be relaxed to +/-50 ppm.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET/SDH data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance proposed for SONET equipment by GR-253-CORE as shown in Figure 5.

Figure 5 SPECTRA 4x155 Typical Jitter Tolerance



10.1.2 Serial-to-Parallel Converter (SIPO)

The Serial-to-Parallel Converter (SIPO) inside the CRSI converts the received bit serial SONET/SDH stream into a byte serial stream. The SIPO searches for the SONET/SDH framing pattern (A1, A2) in the incoming stream and performs serial-to-parallel conversion on octet boundaries.

While out-of-frame, the CRSI block monitors the receive bit-serial STS-3 (STM-1) data stream for an occurrence of the framing pattern (A1, A2). The CRSI adjusts its byte alignment of the SIPO when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The CRSI informs the RSOP Framer block when the framing pattern has been detected to reinitialize the RSOP to the new frame alignment. While in-frame, the CRSI maintains the byte alignment of the SIPO until RSOP declares OOF.

10.2 Receive Section Overhead Processor (RSOP)

The Receive Section Overhead Processor (RSOP) block processes the section overhead (regenerator section) of the receive STS-3 (STM-1) stream, providing frame synchronization, de-scrambling, section level alarm, and performance monitoring.

The RSOP may also force Line AIS. AIS-L is inserted in the receive data stream using input RLAIS or, optionally, automatically when LOS, LOF, or when section trace mismatch or unstable events occur. Line AIS may also be inserted automatically on signal degrade or signal failure events. This line AIS is forced after the RLOP. The automatic insertion of receive line AIS is controlled by the Receive Line AIS Control Register.

The RSOP-declared OOF, LOF, and LOS events can be optionally reported on the SALM or RALM outputs.

The RSOP block provides descrambled data and frame alignment indication signals for use by the Receive Line Overhead Processor (RLOP).

10.2.1 Framer

The Framer Block of RSOP determines the in-frame/OOF status of the receive stream.

While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. OOF is declared when four consecutive frames containing one or more framing pattern errors have been received.

The RSOP block frames to the data stream by operating with an upstream pattern detector (the SIPO block) that searches for occurrences of the framing pattern (A1, A2) in the bit serial data stream. Once the SIPO has found byte alignment, the RSOP block monitors for the next occurrence of the framing pattern 125 µs or later. The block declares frame alignment when either all A1 and A2 bytes are seen error-free or when only the first A1 byte and the first four bits of the last A2 byte are seen error-free. The first algorithm examines 24 bytes of A1 and A2 in the STS-3 (STM-1) stream. The second algorithm examines only the first occurrence of A1 and the first four bits of the last occurrence of A2 in the sequence. Once in-frame, the RSOP block monitors the framing pattern sequence and declares an OOF when one or more bit errors in each framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes are examined for bit errors in each frame, or only the A1 byte and the first four bits of the last A2 byte (that is, 12 bits total) are examined for bit errors in each frame.

These framing algorithms perform robustly in the presence of bit errors and random data. When searching for frame alignment, each algorithm's performance is dominated by the SIPO's alignment algorithm, which always examines all framing bits. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the SPECTRA 4x155 continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 1.3 seconds in STS-3 (STM-1) SONET/SDH mode. The second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

10.2.2 Descramble

The Descramble Block of RSOP uses a frame-synchronous descrambler to process the receive stream. The generating polynomial is $x^7 + x^6 + 1$ and the sequence length is 127. Details of the de-scrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the trace/growth bytes (J0/Z0) are not descrambled. A register bit is provided to disable the de-scrambling operation.

10.2.3 Error Monitor

The Error Monitor Block of RSOP calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-3c (STM-1) frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section-level bit errors in a 16-bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to zero or one, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

10.2.4 Loss of Signal (LOS)

The LOS Block of RSOP monitors the scrambled data of the receive stream for the absence of all-ones. When 20 ± 3 µs of all zeros patterns is detected, a LOS is declared. LOS is cleared when two valid framing words are detected and during the intervening time, no LOS condition is detected. The LOS signal is optionally reported on the RALRM output pin when enabled by the LOSEN Receive Alarm Control Register bit.

10.2.5 Loss of Frame (LOF)

The LOF Block monitors the in-frame/OOF status of the Framer Block of RSOP. A LOF is declared when an OOF condition persists for 3 ms. It is cleared when an in-frame condition persists for a period of 3 ms. To provide for intermittent OOF (or in-frame) conditions, the 3 ms timer is not reset to zero until an in-frame (or OOF) condition persists for 3 ms. The LOF and OOF signals are optionally reported on the RALRM output pin when they are enabled by the LOFEB and OOFEN Receive Alarm Control Register bits.

10.3 Receive Section Trace Buffer (SSTB)

In mode 1 operation, the receive portion of the SONET/SDH Section Trace Buffer (SSTB) captures the received section trace identifier message (J0 byte) into microprocessor readable registers. It contains four pages of trace message memory:

- The transmit message page.
- The capture page.
- The accepted page.

- The expected page.

Section trace identifier data bytes from the receive stream are written into the capture page. The expected identifier message is downloaded by the microprocessor into the expected page. On receipt of a trace identifier byte, it is written into the next location in the capture page. The received byte is compared with the data from the previous message in the capture page. The identifier message is accepted if it is received unchanged three times, or optionally, five times. The accepted message is then compared with the expected message.

If enabled, an interrupt is generated if the accepted message changes from “matching” the expected message to “mismatching” and vice versa. If the current message differs from the previous message for eight consecutive messages, the received message is declared unstable. The received message is declared stable once the received message passes the persistency criterion (three or five identical receptions) for being accepted. Note: An interrupt may be optionally generated on entry to and exit from the unstable state. Optionally, line AIS may be inserted in the received stream when the receive message is in the mismatched or unstable state.

The length of the section trace identifier message is selectable between 16-bytes and 64-bytes. When programmed for 16-byte messages, the section trace buffer synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64-byte messages, the section trace buffer synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the head of the capture page. This enables the section trace message to be appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled. In this case, the memory acts as a circular buffer.

Mode 2 section trace identifier operation is also supported. For mode 2 support, a stable message is declared when forty-eight of the same section trace identifier message (J0) bytes are received. Once in the stable state, an unstable state is declared when one or more errors are detected in three consecutive 16-byte windows.

10.4 Receive Line Overhead Processor (RLOP)

The Receive Line Overhead Processor block (RLOP) processes the line overhead (multiplexer section) of the receive STS-3 (STM-1) stream. The block declares the LAIS and LRDI alarms. In Addition the RLOP detects and accumulates B2 errors, accumulated L-REI and extracts the K1/K2 APS bytes. The extracted automatic protection switch bytes (K1, K2) are supplied to the RASE block for further processing and alarm declaration.

An interrupt output is provided that may be activated by declaration or removal of line AIS, line RDI, protection switching byte failure alarm, a change of APS code value, a single B2 error event, or a single line REI event. Each interrupt source is individually maskable.

10.4.1 Line RDI Detect

The Line RDI Detect Block within the RLOP detects the presence of remote defect indication (LRDI) in the receive stream. Line RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LRDI signal is optionally reported on the SALM output pin when enabled by the LRDISALM Section Alarm Output Control #2 Register bit.

10.4.2 Line AIS Detect

The Line AIS Block detects the presence of an alarm indication signal (LAIS) in the receive stream. Line AIS is declared when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LRDI signal is optionally reported on the SALM output pin when enabled by the LAISSALM Section Alarm Output Control #1 Register bit.

10.4.3 Error Monitor Block

The Error Monitor Block calculates the received line BIP-8 error detection codes based on the Line Overhead bytes and SPEs of the STS-3 (STM-1) stream. The line BIP-8 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the following frame. Any differences indicate that a line layer bit error has occurred. As well, the RLOP can be configured to count a maximum of only one BIP error per frame. Accumulated B2 errors are passed to the RASE block for processing and the declaration of signal degrade and signal failure.

This block also extracts the line REI code from the M1 byte. The REI code is contained in bits 2 to 8 of the M1 byte, and represents the number of line BIP-8 errors that were detected in the last frame by the far end. The REI code value has 25 legal values (0 to 24) for an STS-3 (STM-1) stream. Illegal values are interpreted as zero errors.

The Error Monitor Block accumulates B2 error events and REI events in two 20-bit saturating counters that can be read via the microprocessor interface. The contents of these counters may be transferred to internal holding registers by writing to any one of the counter addresses, or by using the TIP register bit feature. During a transfer, the counter value is latched and the counter is reset to zero (or one, if there is an outstanding event). Note: these counters should be polled at least once per second to avoid saturation.

The B2 error event and REI event counters can be optionally configured to accumulate only "word" errors. A B2 word error is defined as the occurrence of one or more B2 bit error events during a frame. In STS-3 (STM-1) framing, a REI word event is defined as the occurrence of one or more REI bit events during a frame. The B2 error or REI event counter is incremented by one for each frame in which a B2 word error or REI event occurs.

10.5 The Receive APS, Synchronization Extractor and Bit Error Monitor (RASE)

The RASE block performs APS control, monitors the bit error rate, and extracts the synchronization status.

10.5.1 Automatic Protection Switch (APS) Control

The Automatic Protection Switch (APS) control block of RASE filters and captures the receive APS channel bytes (K1 and K2) allowing them to be read via the RASE APS K1 register and the RASE APS K2 register. The bytes are filtered for three frames before being written to these registers. A protection switching byte-failure-alarm is declared when 12 successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the RASE APS K1 Register and the RASE APS K2 Register.

10.5.2 Bit Error Rate Monitor (BERM)

The Bit Error Monitor Block (BERM) of RASE calculates the received line BIP-24 error detection code (B2) based on the line overhead and SPE of the STS-3c (STM-1) receive data stream. The line BIP-24 code is a BIP calculation using even parity. Details are provided in the references. The calculated BIP-24 code is compared with the BIP-24 code extracted from the B2 byte(s) of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 192000 (24 BIP/frame x 8000 frames/second) bit errors can be detected per second for STS-3c (STM-1) rate.

The BERM accumulates these line layer bit errors in a 20-bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to zero (or one, if there is an outstanding event). Note this counter should be polled at least once per second to avoid saturation that in turn may result in missed bit error events.

The BERM block is able to simultaneously monitor for SF or SD threshold crossing and provide alarms through software interrupts. The bit error rates associated with the SF or SD alarms are programmable over a range of 10^{-3} to 10^{-9}. Details are provided in the Operations section.

In both declaring and clearing detection states, the accumulated BIP count is continuously compared against the threshold. This allows to rapidly declaring in the presence of error bursts or error rates that significantly exceed the monitored BER. This behavior allows meeting the ITU-T G.783 detection requirements at various error rates (where the detection time is a function of the actual BER, for a given monitored BER.

10.5.3 Synchronization Status Extraction

The Synchronization Status Extraction (SSE) Block of RASE extracts the synchronization status (S1) byte from the line overhead. The SSE block can be configured to capture the S1 nibble after three or after eight frames with the same value (filtering turned on) or after any change in the value (filtering turned off). The S1 nibble can be read via the microprocessor interface. Optionally, the SSE can be configured to perform filtering based on the whole S1 byte. Although this mode of operation is not standard, it might become useful in the future.

10.6 Receive Transport Overhead Controller (RTOC)

The Receive Transport Overhead Controller block (RTOC) extracts the entire receive transport overhead on RTOH1-4, along with the nominal 5.184 MHz transport overhead clock, RTOHCLK1-4, and the transport overhead frame position signal, RTOHFP1-4, allowing identification of the bit positions in the transport overhead stream.

Individual data channels are also generated on the RSLD1-4 output. RTOHFP1-4 can be used to identify the required byte alignment on the serial input. The extracted TOH bytes on the above port may also be forced to all-ones on declaration of LOS/LOF/LAIS/TIM alarms.

10.7 Ring Control Port

The transmit and receive Ring Control ports provide bit-serial access to the section and line layer alarm and the maintenance signal status and control. These ports are useful in ring-based Add/Drop multiplexer applications where alarm status and maintenance signal insertion control must be passed between separate SPECTRA 4x155s (possibly residing on separate cards). Each ring control port consists of three signals: clock, data, and frame position. It is intended that the clock, data, and frame position outputs of the receive ring control port are connected directly to the clock, data, and frame position inputs of the transmit ring control port of the mate SPECTRA 4x155. The alarm status and maintenance signal control information that is passed on the ring control ports consists of:

- Filtered APS (K1 and K2) byte values.
- Change of filtered APS byte value status.
- Protection switch byte failure alarm status.
- Change of protection switch byte-failure-alarm status.
- Line RDI maintenance signal insertion in the mate SPECTRA 4x155.
- Line AIS maintenance signal insertion in the mate SPECTRA 4x155.
- Line REI information insertion in the mate SPECTRA 4x155.

The same APS byte values must be seen for three consecutive frames before being shifted out on the receive ring control port. The change of filtered APS byte value status is high for one frame when a new, filtered APS value is shifted out.

The protection switch byte failure alarm bit position is high when, after 12 consecutive frames since the last frame containing a previously consistent byte, no three consecutive frames containing identical K1 bytes have been received. The bit position is set low when three consecutive frames containing identical K1 bytes have been received. The change of the protection switch byte-failure-alarm status bit position is set high for one frame when the alarm state changes.

The insert line RDI bit position is set high under register control, or when LOS, LOF, or line AIS alarms are declared. The insert line AIS bit position is set high under register control only.

The insert line REI bit positions are high for one bit position for each detected B2 bit error. Up to 24 line REIs may be indicated per frame for an STS-3 (STM-3c) stream.

10.8 Receive De-multiplexer (RX_DEMUX)

The receive de-multiplexer (RX_DEMUX) block within each channel de-multiplexes the STS-3 (STM-1) stream into three STS-1(STM-1/AU3) streams or three equivalent STS-1(STM1/AU3) streams for an STS-3c(ATM1(AU4). In the case of an STS-3 (STM1/AU3) stream, the demultiplexed streams are fed into three master RPPSs. In the case of an STS-3c (STM1/AU4) stream, the demultiplexed streams are fed into one master RPPS and two slave RPPSs. The slave slices receiving the equivalent STS-1 #2 and #3.

The de-multiplexer also generates the low speed clock to accompany the streams into the slices.

10.9 Receive Path Processing Slice (RPPS)

The Receive Path Processing Slice (RPPS) of the RASE block provides path-processing termination for the four STS-3/3c (STM-1/AU-3/AU-4) streams received from the RLOP blocks. The path processing includes:

- Pointer interpretation.
- Path overhead and SPE (VC) extraction.
- Path level alarm and performance monitoring.
- Path trace identifier message (J1 bytes) extraction and processing.

Plesiochronous frequency offsets between the receive data stream and the Drop bus are accommodated by pointer adjustments. PRBS payload generation and monitoring is also supported on a per STS (AU) basis.

12 RPPSs (RPPS#1 to RPPS#12), arranged in four groups of three RPPSs each, are required to process the four STS-3 (STM-1) receive streams from the RLOP blocks. Each channel can be independently configured to process STS-3 (STM-1/AU-3) or STS-3c (STM-1/AU-4) streams. An STS-3 (STM-1/AU-3) stream is processed as three independent STS-1 (STM-0/AU-3) streams by the individual RPPSs in the group.

In processing an STS-3c (STM-1/AU-4), the first STS-1 (STM-0/AU-3) equivalent stream will be processed by an RPPS (for example, RPPS#1) configured as the master. The master RPPS controls two slave RPPSs (for example, RPPS#2, RPPS#3) that process the second and third STS-1 (STM-0/AU-3) equivalent streams respectively. The processing of a concatenated stream is coordinated by the control signals originating from the master RPPS and status information fed back from the slave RPPSs.

The path overhead bytes extracted by the RPPSs from all the receive STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) streams are extracted and serialized on an output RPOH, which is a multiplexed output signal. The path overhead bytes of all four channels are multiplexed onto RPOH. Output RPOHFP is provided to identify the most significant bit of the path trace byte (J1) of channel #1 first STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) on RPOH.

Note: The path overhead bytes are provided on RPOH at close to twice the rate in which they are received to facilitate the multiplexing of the extracted data from the various RPPSs on to a single serial output. Output RPOHEN is provided to mark the valid (fresh) path overhead bytes on RPOH. The path overhead clock, RPOHCLK, is nominally a 12.96 MHz clock. RPOH, RPOHEN, and RPOHFP are updated with timing aligned to RPOHCLK.

Received path BIP errors and receive path alarms for all the receive STS-1 (STM-0/AU-3) or STS-3c (STM-1/AU-4) streams of a SPECTRA 4x155 channel are communicated to the corresponding transmit path processing slices (TPPSs) in a mate SPECTRA 4x155 via the receive alarm port. The port carries the count of received path BIP errors. Detected receive alarms are reported in the alarm port and will trigger the corresponding remote TPOP to signal path RDI in the transmit stream.

Under a no transmit AIS-L condition, the receive alarm port also reports the APS bytes (K1, K2) that are placed on the transmit stream of the SPECTRA 4x155. In conjunction with the transmit alarm port of a mate SPECTRA 4x155, the working SPECTRA 4x155 can control the APS bytes of the protection SPECTRA 4x155. Under AIS-L generation on the transmit stream, the K1 and K2 bytes extracted are those that would have been transmitted if it were not for the forcing of AIS-L.

The PRBS generator of an RPPS can be enabled to generate the Drop bus transport frame in addition to the payload. For an STS-3c (STM-1/AU-4) stream, the PRBS generator in each of the three RPPSs required to process the concatenated stream will generate one third (one in three) of the PRBS payload sequence. A complete PRBS payload sequence is produced when these three partial sequences are byte interleaved. The PRBS generator in the master RPPS co-ordinates the PRBS generation by itself and by its counterparts in the two slave RPPSs.

When enabled, the PRBS monitor of an RPPS will synchronize itself to the receive payload sequence in an STS-1 (STM-0/AU-3) or equivalent stream. If it is successful in finding the pseudo-random sequence, then pattern errors detected will be accumulated in the corresponding error counter. For an STS-3c (STM-1/AU-4) stream, the PRBS monitor, in each of the three RPPSs required to process the concatenated stream, will independently validate one third (one in three) of the PRBS payload sequence.

10.9.1 Receive Path Overhead Processor (RPOP)

The Receive Path Overhead Processor (RPOP) of RPPS provides pointer interpretation, extraction of path overhead, extraction of the SPE (VC), and path level alarm and performance monitoring.

Pointer Interpreter

The Pointer Interpreter interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in an STS-1 (STM-0/AU-3) or equivalent stream. A finite state machine can model the algorithm. Within the pointer interpretation algorithm three states are defined as shown below:

- NORM_state (NORM).
- AIS_state (AIS).
- LOP_state (LOP).

The transition between states will be consecutive events (indications). Refer to Figure 6. An example is when three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. Note: Since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 6 Pointer Interpretation State Diagram

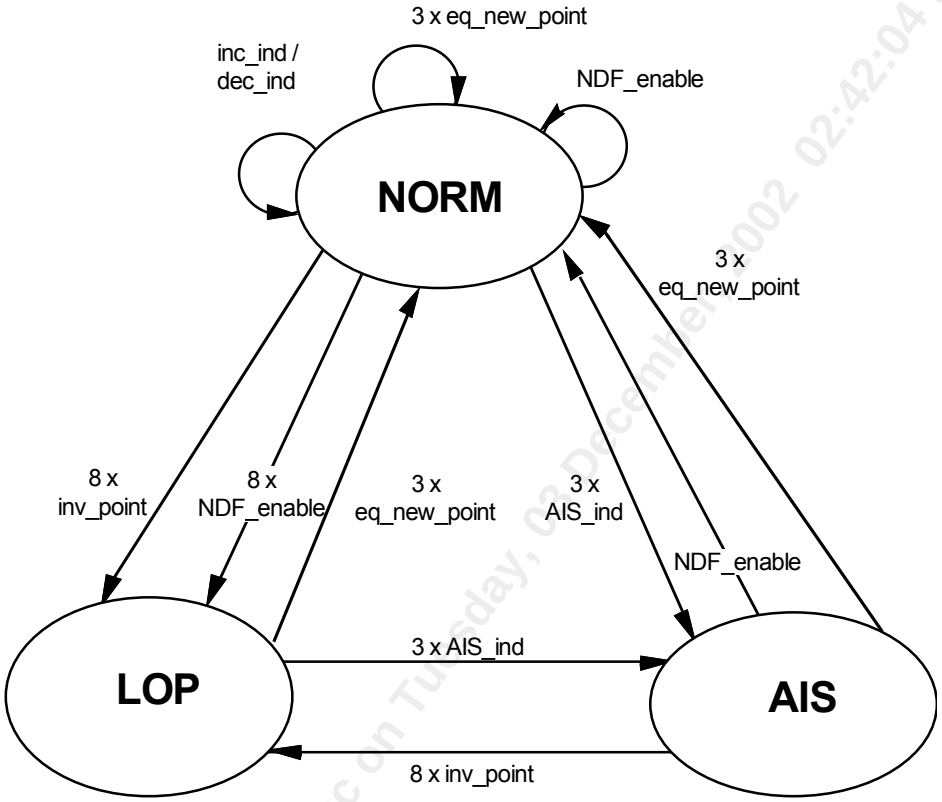


Table 1 defines the events (indications) shown in the state diagram.

Table 1 Pointer Interpreter Event (Indications) Description

Event (Indication)	Description
norm_point	Disabled NDF + ss + offset value equal to active offset.
NDF_enable	Enabled NDF + ss + offset value in range of 0 to 782. Or Enabled NDF + ss, if NDFPOR bit is set (Note that the current pointer is not updated by an enabled NDF if the pointer is out of range).
AIS_ind	H1 = 'hFF, H2 = 'hFF.
inc_ind	Disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago.
dec_ind	Disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago.
inv_point	Not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind).
new_point	Disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset.
inc_req	Majority of I bits inverted + no majority of D bits inverted.

Event (Indication)	Description
dec_req	Majority of D bits inverted + no majority of I bits inverted.

Notes

1. Active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.
2. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, and 1000.
3. Disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, and 0111.
4. The remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_ndf indication.
5. The ss bits are unspecified in SONET and has bit pattern 10 in SDH.
6. The use of ss bits in definition of indications may be optionally disabled.
7. The requirement for previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.
8. new_point is also an inv_point.
9. LOP is not declared if all the following conditions exist:

- The received pointer is out of range (>782),
- The received pointer is static,
- The received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication,
- After making the requested justification, the received pointer continues to be interpretable as a pointer justification.
- When the received pointer returns to an in-range value, the SPECTRA 4x155 will interpret it correctly.

10. LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.
11. For the purposes of 8xNDF_enable only, the requirement of the pointer to be within the range of 0 to 782 may be optionally disabled.

Table 2 defines the transitions indicated in the state diagram.

Table 2 Pointer Interpreter Transition Description

Transition	Description
inc_ind/dec_ind	Offset adjustment (increment or decrement indication).
3 x eq_new_point	Three consecutive equal new_point indications.
NDF_enable	Single NDF_enable indication.
3 x AIS_ind	Three consecutive AIS indications.
8 x inv_point	Eight consecutive inv_point indications.
8 x NDF_enable	Eight consecutive NDF_enable indications.

Notes

1. The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.
2. 3 x new_point takes precedence over other events and if the IINVCNT bit is set resets the inv_point count.
3. All three offset values received in 3 x eq_new_point must be identical.

4. "Consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

In an STS-1 (STM-0/AU-3) stream, the Pointer Interpreter detects:

- Loss of Pointer (LOP).
- Path AIS (PAIS).
- LOP-concatenated (LOPCON), when RPOP is operating as in a slave RPPS.
- Path AIS-concatenated (PAISCON), when RPOP is operating as in a slave RPPS.

The Pointer Interpreter declares LOP on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF-enabled indications. Path AIS is optionally inserted in the Drop bus when LOP is declared. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA 4x155 to insert a path RDI indication.

The Pointer Interpreter declares PAIS on entry to the AIS_state after three consecutive AIS indications. Path AIS is inserted in the Drop bus when AIS is declared. The alarm condition reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA 4x155 to insert a path RDI indication.

In an equivalent STS-1 (STM-0/AU-3) stream when RPOP is operating in a slave RPPS, the Pointer Interpreter declares LOPCON on entry to the LOPCON_state as a result of eight consecutive pointers with values other than concatenation indications (‘b1001 xx 1111111111). Path AIS is optionally inserted in the Drop bus when LOPCON is declared. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA 4x155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in Drop bus G1 byte is set to indicate the LOP alarm to the TPOP in a remote SPECTRA 4x155.

In an equivalent STS-1 (STM-0/AU-3) stream when RPOP is operating in a slave RPPS, the Pointer Interpreter declares PAISCON on entry to the AISC_state after three consecutive AIS indications. Path AIS is optionally inserted in the Drop bus when AISC is declared. The alarm condition reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SPECTRA 4x155 to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in Drop bus G1 byte is set to indicate the PAIS alarm to the TPOP in a remote SPECTRA 4x155.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF-enabled or NDF-disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset is updated with the receive pointer value. An illegal pointer change is defined as a inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The active offset value is used to extract the path overhead from the incoming stream and can be read from an internal register.

Multi-frame Framer

The multi-frame alignment sequence in the path overhead H4 byte is monitored for the bit patterns of 00, 01, 10, and 11 in the two least significant bits. If an unexpected value is detected, the primary multi-frame will be kept, and a second multi-frame process will, in parallel, check for a phase shift. The primary process will enter an out-of-multi-frame state (OOM). A new multi-frame alignment is chosen, and OOM state is exited when four consecutive correct multi-frame patterns are detected. Loss-of-multi-frame (LOM) is declared after residing in the OOM state for eight frames without re-alignment. A new multi-frame alignment is chosen, and LOM state is exited when four consecutive correct multi-frame patterns are detected.

Error Monitoring

Three 16-bit counters are provided to accumulate path BIP-8 errors (B3) and path remote error indications (REI). The contents of the counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame with the path BIP-8 computed for the previous frame. BIP-8 errors are selectable to be counted as bit errors or as block errors via register bits. When processing a concatenated stream, the RPOP in a master RPPS will include the BIP-8 values computed by its slave RPPSs in the generation of the actual BIP-8 for the stream. When in-band error reporting is enabled, the error count is inserted into the path status byte (G1) of the Drop bus.

Path REIs are detected by extracting the 4-bit path REI field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path RDI alarm is detected by extracting bit 5 of the path status byte. The PRDI signal is set high when bit 5 is set high for five/ten consecutive frames. PRDI is set low when bit 5 is low for five/ten consecutive frames.

The Enhanced RDI alarm is detected when the enhanced RDI code in bits 5, 6, 7 of the path status byte indicates the same error codepoint for five/ten consecutive frames. The Enhanced RDI alarm is removed when the enhanced RDI code in bits 5, 6, 7 of the path status byte indicates the same non-error codepoint for five/ten consecutive frames.

The SPECTRA 4x155 receive section does not support in-band error reporting of RDI codes.

Path Overhead Extract

Path overhead bytes are extracted from an STS-1 (STM-0/AU-3) or equivalent stream that is being processed by the RPOP. When processing a concatenated stream, only the RPOP in a master RPPS will provide valid path overhead bytes. The extracted path overhead bytes will be serialized and multiplexed on to RPOH by higher-level logic.

Receive Alarm Port

Path BIP errors and path RDIs for an STS-1 (STM-0/AU-3) or equivalent stream that are being processed by the RPOP are provided to the higher level logic for communicating via the Receive Alarm Port to the corresponding transmit path overhead processor (TPOP) in a mate SPECTRA 4x155. There is an independent Receive Alarm Port stream for each four channels of the SPECTRA-4X155. When processing a concatenated stream, only the RPOP in the master RPPS will provide the valid path BIP error count and path RDI code for the stream.

10.9.2 Receive Path Trace Buffer (SPTB)

In mode 1 operation, the receive portion of the SONET/SDH Path Trace Buffer (SPTB) of RPPS captures the received path trace identifier message (J1 bytes) into microprocessor readable registers. It contains four pages of trace message memory. They are:

- The transmit message page.
- The capture page.
- The accepted page.
- The expected page.

Path trace identifier data bytes from the receive stream are written into the capture page. The expected identifier message is downloaded by the microprocessor into the expected page. On receipt of a trace identifier byte, it is written into next location in the capture page. The received byte is compared with the data from the previous message in the capture page. The identifier message is accepted if it is received unchanged three times, or optionally, five times. The accepted message is then compared with the expected message.

If enabled, an interrupt is generated when the accepted message changes from “matching” the expected message to “mismatching” vice versa. If the current message differs from the previous message the unstable counter is incremented by one. When the unstable count reaches eight, the received message is declared unstable. The received message is declared stable and the unstable counter reset, when the received message passes the persistency criterion (three or five identical receptions) for being accepted. An interrupt may be optionally generated on entry to and exit from the unstable state. Optionally, path AIS may be inserted in the Drop bus when the receive message is in the mismatched or unstable state.

The length of the path trace identifier message is selectable between 16-bytes and 64-bytes. When programmed for 16-byte messages, the SPTB synchronizes to the byte with the most significant bit set to high and places the byte at the first location in the capture page. When programmed for 64-byte messages, the SPTB synchronizes to the trailing carriage return (CR = 0DH), line feed (LF = 0AH) sequence and places the next byte at the head of the capture page. This enables the path trace message to be appropriately aligned for interpretation by the microprocessor. Synchronization may be disabled, in which case, the memory acts as a circular buffer.

Mode 2 path trace identifier operation is supported. For mode 2 support, a stable message is declared when forty eight of the same section trace identifier message (J1) bytes are received. Once in the stable state, an unstable state is declared when one or more errors are detected in three consecutive sixteen byte windows.

The path signal label (PSL) found in the path overhead byte (C2) is processed. An incoming PSL is accepted when it is received unchanged for five consecutive frames. The accepted PSL is compared with the provisioned value. The PSL match/mismatch state is determined as follows:

Table 3 Path Signal Label Match/Mismatch State Table.

Expected PSL	Accepted PSL	PSLM State
00	00	Match
00	01	Mismatch
00	X ≠ 00	Mismatch
01	00	Mismatch
01	01	Match
01	X ≠ 01	Match
X ≠ 00, 01	00	Mismatch
X ≠ 00, 01	01	Match
X ≠ 00, 01	X	Match
X ≠ 00, 01	Y	Mismatch

Each time an incoming PSL differs from the one in the previous frame, the PSL unstable counter is incremented. Thus, a single bit error in the PSL in a sequence of constant PSL values will cause the counter to increment twice, once on the errored PSL and again on the first error-free PSL. The incoming PSL is considered unstable, when the counter reaches five. The counter is cleared when the same PSL is received for five consecutive frames.

In normal operation, only the status of the SPTB in a master RPPS should be monitored.

10.9.3 Receive TelecomBus Aligner (RTAL)

The Receive TelecomBus Aligner (RTAL) block of RPPS takes the payload data from an STS-1 (STM-0/AU-3) or equivalent stream from the RPOP and inserts it in a TelecomBus Drop bus. It aligns the frame of the received STS-1 (STM-0/AU-3) or equivalent stream to the frame of the Drop bus. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the receive stream and that of the Drop bus. When processing a concatenated stream, only the RTAL in the master RPPS will be performing the pointer adjustment calculation. The RTALs in the slave RPPSs will follow the new alignment of the RTAL in the master RPPS.

Frequency offsets from plesiochronous network boundaries, or the loss of a primary reference timing source and phase differences from normal network operation between the receive data stream and the Drop bus are accommodated by pointer adjustments in the Drop bus. Drop bus pointer justification events are indicated and are accumulated in the Performance Monitor (PMON) block. Large differences between the number and type of received pointer justification events as indicated by the RPOP block, and pointer justification events generated by the RTAL block may indicate network synchronization failure.

When the RPOP block detects a loss of multi-frame, the RTAL may optionally insert all-ones in the tributary portion of the SPE. The path overhead column and the fixed stuff columns are unaffected.

The RTAL may optionally insert the tributary multi-frame sequence and clear the fixed stuff columns. The tributary multi-frame sequence is a 4-byte pattern ('hFC, 'hFD, 'hFE, 'hFF) applied to the H4 byte. The H4 byte of the frame containing the tributary V1 bytes is set to 'hFD. The fixed stuff columns of a SPE (VC) may optionally be over-written all-zeros in the fixed stuff bytes.

Elastic Store

The Elastic Store perform rate adaptation between the receive data stream and the Drop bus. The entire received payload, including path overhead bytes, is written into in a first-in-first-out (FIFO) buffer at the receive byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. Receive pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the Drop bus rate by the Pointer Generator. Analogously, pointer justifications on the Drop bus are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

The FIFO read and write Addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the Addresses relative to programmable thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the Drop bus for three frames to alert downstream elements of data corruption.

Pointer Generator

The Pointer Generator generates the Drop bus pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the Drop bus STS-1 (STM-0/AU-3) stream. The algorithm can be modeled by a finite state machine. Within the pointer generator algorithm, five states are defined as shown below:

- NORM_state (NORM).
- AIS_state (AIS).
- NDF_state (NDF).
- INC_state (INC).
- DEC_state (DEC).

The transition from the NORM to the INC, DEC, and NDF states is initiated by events in the Elastic Store (ES) block. The transition to/from the AIS state are controlled by the pointer interpreter (PI) in the Receive Path Overhead Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 7 Pointer Generation State Diagram

The events indicated in the state diagram are defined in Table 4.

Table 4 Pointer Generator Event (Indications) Description

Event (Indication)	Description
ES_lowerT	ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.
ES_upperT	ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.
FO_discont	Frame offset discontinuity.

Event (Indication)	Description
PI_AIS	PI in AIS state.
PI_LOP	PI in LOP state.
PI_NORM	PI in NORM state.

Note

1. A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined in Table 5.

Table 5 Pointer Generator Transition Description

Transition	Description
inc_ind	Transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.
dec_ind	Transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.
NDF_enable	Accept new offset as active offset, transmit the pointer with NDF enabled and new offset.
norm_point	Transmit the pointer with NDF disabled and active offset.
AIS_ind	Active offset is undefined, transmit an all-1's pointer and payload.

Notes

1. Active offset is defined as the phase of the SPE (VC).
2. The ss bits are undefined in SONET, and has bit pattern 10 in SDH
3. Enabled NDF is defined as the bit pattern 1001.
4. Disabled NDF is defined as the bit pattern 0110.

When operating in a slave RPPS, the concatenation indications (‘b1001 xx 1111111111) will be generated in the pointer bytes (H1 and H2).

A piece of tandem connection originating equipment should signal incoming signal failure by setting the IEC field and the payload bytes to all-ones. A piece of tandem connection terminating equipment should detect ISF by only examining the IEC field for all-ones. If the upstream tandem connection originating equipment inserts a malformed, non-compliant ISF condition where the payload bytes are not all-ones, the SPECTRA-4X155 toggles in and out of the ISF state. However, in real systems, this behavior should not be observed because the upstream tandem connection originating equipment inserts a standards compliant ISF condition.

10.9.4 Drop Bus PRBS Generator and Monitor (DPGM)

The Drop bus Pseudo-random bit sequence Generator and Monitor (DPGM) block of RPPS generates and monitors an unframed 2^{23}-1 payload test sequence in an STS-1 (STM-0/AU-3) or equivalent stream on the Drop bus.

The PRBS generator of the DPGM can be configured to overwrite the payload bytes on the Drop bus as well as autonomously generate both the payload bytes and the framing on the Drop bus. The path overhead column and, optionally, the fixed stuff columns in an STS-1 (STM-0/AU-3) stream are not overwritten with PRBS payload bytes.

When processing a concatenated stream, the DPGM in a master RPPS co-ordinate the distributed PRBS generation by itself and its counterparts in the slave RPPSs. Each DPGM will generate one third (1 in 3) of the complete PRBS sequence for an STS-3c (STM-1/AU-4) stream. The master DPGM will be generating the partial sequence for the 1^{st} (after the transport overhead columns) and subsequent SPE bytes occurring at a 3-byte interval. The next partial sequence for the 2^{nd} and every third bytes thereafter will be generated by the first (in the order of payload generation) slave DPGM and so on. This corresponds to each DPGM processing an equivalent STS-1 (STM-0/AU-3) stream in the concatenated stream.

To ensure that the DPGM blocks in the slave RPPSs are synchronized with the DPGM in the master RPPS, a signature derived from its current state is continuously broadcasted by the master DPGM to allow the slave DPGM blocks to check their relative states. A DPGM operating in a slave RPPS continuously generates a matching signature based on its own state. A signature mismatch is flagged as an out-of-signature state by the slave DPGM. A re-synchronization of the PRBS generation is initiated by the master DPGM (under software control) when one or more slave DPGMs report an out-of-signature state in relation to that of the master DPGM. This involves a re-starting of PRBS generation in each DPGM from a pre-determined state according to the order of generation (transmission or reception) assigned to a particular DPGM.

When a path overhead byte position is encountered by the master DPGM in an STS-3c (STM-1/AU-4) stream, the master DPGM will not generate the next PRBS data byte, this task is left to the (first) slave DPGM that is next in line to generate a PRBS data byte. The second slave DPGM (in the order of generation) will now generate the PRBS data byte that is supposed to be generated by the first slave DPGM and so on. This means that the current states of the slave DPGM blocks will be re-aligned relative to the new state of the master DPGM to collectively skip over the path overhead byte position encountered by the master DPGM.

The PRBS monitor of the DPGM block monitors the recovered payload data for the presence of an unframed 2^{23}-1 test sequence and accumulates pattern errors detected based on this pseudo-random pattern. The DPGM declares synchronization when a sequence of 32 correct pseudo-random patterns (bytes) are detected consecutively. Pattern errors are only counted when the DPGM is in synchronization with the input sequence. When 16 consecutive pattern errors are detected, the DPGM will fall out of synchronization and it will continuously attempt to re-synchronize to the input sequence until it is successful.

When processing a concatenated stream, individual DPGM blocks, including the master DPGM, independently monitor their corresponding one third (1 in 3) of the complete PRBS payload sequence according to the SONET/SDH concatenated mode of the stream. The master DPGM will be monitoring the partial sequence contained in the 1st (after the transport overhead columns) and subsequent SPE bytes occurring at a 3-byte interval. The next partial sequence contained in the 2nd and every third bytes thereafter will be validated by the first (in the order of payload reception) slave DPGM and so on. Individual DPGM synchronization status and error count accumulation are provided. Optionally, an interrupt can be generated by the DPGM whenever a loss of synchronization or re-synchronization occurs.

Path overhead bytes and fixed stuff columns in the receive concatenated stream will be collectively skipped over as described for the PRBS generator of the DPGM. To ensure that all payload bytes (all STS-1 (STM-0/AU-3) or equivalent streams) in a concatenated stream together contain a single PRBS sequence, the signature generation by the master DPGM and signature matching by the slave DPGM monitors will be performed as described for the PRBS generation. Individual DPGM can only declared that has synchronized to the receive PRBS sequence when it has synchronized to its corresponding partial sequence and its has detected no signature mismatch.

10.9.5 Pointer Justification Monitor

The Pointer Justification Monitor (PMON) of RPPS accumulates pointer justification events (PJE) events in counters over intervals that are defined by the supplied transfer clock signal. The counters saturate at 255. Four counters are provided in order to accumulate four types of events; increment and decrement of receive or transmit pointers. The receive pointer events can be those of the receive stream before the FIFO or can be those of the Drop bus after rate adaption in the RTAL FIFO.

When the transfer signal is applied by writing to the TIP register bit, the PMON transfers the counter values into holding registers and resets the counters to begin accumulating error events for the next interval. The counters are reset in such a manner that error events occurring during the reset period are not missed. Writing to internal registers can also trigger this transfer.

10.10 Transmit Path Processing Slice (TPPS)

The Transmit Path Processing Slice (TPPS) generates transport frame alignment, inserts path overhead and the SPE as well as path level alarm signals and path BIP-8 (B3) for an STS-1 (STM-0/AU-3) SPE (VC-3) or equivalent data stream from the Add bus. Path trace identifier message (J1 bytes) can also be inserted. Plesiochronous frequency offsets and phase differences, from normal network operation, between the Add bus and the line are accommodated by pointer adjustments in the transmit stream. The TPPS can optionally interpret the pointer (H1, H2) and detect alarm conditions (for example, PAIS) in the STS-1 (STM-0/AU-3) SPE (VC-3) or equivalent data stream from the Add bus. PRBS payload generation and monitoring is also supported on a per STS (AU) basis.

12 TPPSs (TPPS#1 to TPPS#12), arranged in four groups of three TPPSs, are required to process the four STS-3/3c (STM-1/AU-3/AU-4) stream from the Add bus. Each channel can be independently configured to process STS-3 (STM-1/AU-3) or STS-3c (STM-1/AU-4) streams. An STS-3 (STM-1/AU-3) stream is processed as three independent STS-1 (STM-0/AU-3) streams by the individual TPPSs in the group.

In processing an STS-3c (STM-1/AU-4), the first STS-1 (STM-0/AU-3) equivalent stream will be processed by a TPPS (for example, TPPS#1) configured as the master. The master TPPS controls two slave TPPSs (for example, TPPS#2, TPPS#3) which process the second and third STS-1 (STM-0/AU-3) equivalent streams respectively. Processing of a concatenated stream is coordinated by the control signals originating from the master TPPS and status information feedback from the slave TPPSs.

Received path BIP errors (REI) and path RDIs for all the receive STS-1 (STM-0/AU-3) streams or STS-3c (STM-1/AU-4) streams from the RPPSs in a remote SPECTRA 4x155 are communicated to the corresponding TPPSs in the local SPECTRA 4x155 via the transmit alarm port. The transmit alarm port also contains the transmit APS bytes (K1, K2) of the (remote) working SPECTRA 4x155. In the protection (local) SPECTRA 4x155, the APS bytes in the transmit stream may be optionally sourced from the transmit alarm port.

The PRBS generator of a TPPS can be enabled to overwrite the transmit stream framing in addition to the payload. For an STS-3c (STM-1/AU-4) stream, the PRBS generator in each of the three TPPSs required to process the concatenated stream will generate one third (1 in 3) of the PRBS payload sequence. A complete PRBS payload sequence is produced when these three partial sequences are byte interleaved downstream. The PRBS generator in the master TPPS co-ordinates the PRBS generation by itself and its counterparts in the two slave TPPSs.

When enabled, the PRBS monitor of a TPPS will attempt to synchronize to the payload sequence in the STS-1 (STM-0/AU-3) SPE (VC-3) or equivalent data stream from the Add bus. If it is successful in finding the supported pseudo-random sequence then pattern errors detected will be accumulated in the corresponding error counter. For an STS-3c (STM-1/AU-4) stream, the PRBS monitor in each of the three TPPSs required to process the concatenated stream will independently validate one third (1 in 3) of the PRBS payload sequence.

10.10.1 Add Bus PRBS Generator and Monitor (APGM)

The Add bus Pseudo-random bit sequence Generator and Monitor (APGM) block of TPPS generates and monitors an unframed 2^{23}-1 payload test sequence in an STS-1 (STM-0/AU-3) SPE (VC-3) or equivalent data stream from the Add bus.

The PRBS generator of the APGM can be configured to overwrite the payload bytes of the Add bus STS-1 (STM-0/AU-3) SPE (VC3) data stream with an unframed 2^{23}-1 sequence as well as autonomously generate both the payload bytes and the SPE (VC3) frames. The PRBS monitor of the APGM block monitors the payload data from the Add bus for the presence of an unframed 2^{23}-1 sequence and accumulates pattern errors detected based on this pseudo-random pattern.

The operation of the APGM block is identical to that of the DPGM block of RPPS. Refer to section 10.9.4.

10.10.2 Transmit Pointer Interpreter Processor (TPIP)

The Transmit Pointer Interpreter Processor (TPIP) block of TPPS takes STS-1 (STM-0/AU-3) SPE (VC-3) or equivalent data stream from the Add bus, interprets the pointer (H1, H2), indicates the J1 byte location and detects alarm conditions (for example, PAIS).The indicated J1 byte position will be used only when the APFEN bit in the Add Bus Configuration register is set high or the DISJ1V1 bit is set high in the TPPS Path Configuration register of a specific TPPS. When supplying a valid telecom Add interface with valid J1 pulse, the TPIP pointer alarms may still be used.

Pointer Interpreter

The TPIP block allows the SPECTRA 4x155 to operate with TelecomBus-like back plane systems that do not indicate the J1 byte position. The TPIP block can be enabled using the DISJ1V1 bit in the SPECTRA 4x155 Path Configuration register. When enabled, the TPIP takes a STS-1 (STM-0/AU-3) SONET/SDH stream from the System Side Interface block, processes the stream, identifies the J1 byte location and provides the stream to the corresponding Transmit TelecomBus Aligner block. The block will interpret the Add Bus pointer to determine the J1 byte location. Refer to section 10.9.1 for details of the interpreter state machine.

The same pointer interpreter will be used to determine the J1 byte location when the APFEN control bit is set high. In this mode the Add bus will only a frame pulse identifying the 1st SPE byte of the Add bus.

When supplying a valid J1 pulse which is to be used from the Add Bus (DISJ1V1 and AFP set low), the pointer interpreter will still run and all declared alarms are still valid provided there are valid H1, H2 pointers on the Add bus. These alarms can also be used to force consequential actions.

Slave TPIP blocks are also able to verify for a valid concatenation indicator in the H1 and H2 bytes.

The LOP, LOPCON or PAISCON alarms declared by the pointer interpreter block can be used to force transmit path AIS.

Error Monitoring

Three 16-bit counters are provided to accumulate path BIP-8 errors (B3) and path REI. The contents of the counters may be transferred to holding registers, and the counters reset under microprocessor control. Refer to section 10.9.1 for details on error monitoring.

Multi-frame Framer

The multi-frame alignment sequence in the path overhead H4 byte is monitored for the bit patterns of 00, 01, 10, and 11 in the two least significant bits. If an unexpected value is detected, the primary multi-frame will be kept, and a second multi-frame process will, in parallel, check for a phase shift. The primary process will enter OOM. A new multi-frame alignment is chosen, and OOM state is exited when four consecutive correct multi-frame patterns are detected. LOM is declared after residing in the OOM state for eight frames without re-alignment. A new multi-frame alignment is chosen, and LOM state is exited when four consecutive correct multi-frame patterns are detected.

The LOM alarm declared by block can be used to force transmit tributary AIS.

10.10.3 Transmit TelecomBus Aligner (TTAL)

The Transmit TelecomBus Aligner (TTAL) block of TPPS takes the STS-1 (STM-0/AU-3) SPE (VC-3) or equivalent data stream from the Add bus and aligns it to the frame of the transmit stream. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the Add bus and the transmit stream. In processing a concatenated stream, the TTAL in the master TPPS will perform the pointer offset recalculation and the TTAL's in the slave TPPSs will follow the new pointer offset.

Frequency offsets from plesiochronous network boundaries, or the loss of a primary reference timing source and phase differences, from normal network operation, between the Add bus and the transmit stream are accommodated by pointer adjustments in the transmit stream. For a concatenated stream, the master TTAL will compute and perform the appropriate pointer adjustment to which the slave TTALs will follow.

The TTAL may optionally insert the tributary multi-frame sequence and clear the fixed stuff columns. The tributary multi-frame sequence is a four byte pattern ('hFC, 'hFD, 'hFE, 'hFF) applied to the H4 byte. The H4 byte of the frame containing the tributary V1 bytes is set to 'hFD. The fixed stuff columns of an SPE (VC) may optionally be over-written with all-zeros in the fixed stuff bytes.

Elastic Store

The Elastic Store block performs rate adaptation between the Add bus and the transmit stream. The entire Add bus payload, including path overhead bytes, is written into in a FIFO buffer at the Add bus byte rate. Each FIFO word stores a payload data byte and a one-bit tag labeling the J1 byte. Add bus pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the transmit stream rate by the Pointer Generator block. Analogously, pointer justifications on the transmit stream are accommodated by reading from the FIFO during the negative stuff-opportunity-byte or by not reading during the positive stuff-opportunity-byte.

The FIFO read and write addresses are monitored. Pointer justification requests are made to the Pointer Generator block based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator block schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is inserted in the transmit stream for three frames to alert downstream elements of data corruption.

Pointer Generator

The Pointer Generator Block generates the transmit stream pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the transmit STS-1 (STM-0/AU-3) or equivalent stream. The algorithm is identical to that described in the Receive TelecomBus Aligner (RTAL) block. Refer to section 10.9.3.

When operating in a slave TPPS, the concatenation indications (‘b1001 xx 1111111111) will be generated in the pointer bytes (H1 and H2) when enabled in the TPOP block.

A piece of tandem connection originating equipment should signal incoming signal failure by setting the IEC field and the payload bytes to all-ones. Likewise, the equipment should detect ISF by only examining the IEC field for all-ones. If the upstream tandem connection originating equipment inserts a malformed, non-compliant ISF condition where the payload bytes are not all-ones, the SPECTRA-4X155 toggles in and out of the ISF state. However, in real systems, this behavior should not be observed because the upstream tandem connection originating equipment inserts a standards compliant ISF condition.

10.10.4 Transmit Path Trace Buffer (SPTB)

The transmit portion of the SONET/SDH Path Trace Buffer (SPTB) sources the path trace identifier message (J1) for the Transmit Path Overhead Processor (TPOP) block. The length of the trace message is selectable between 16 bytes and 64 bytes. The SPTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and delivered serially to the TPOP block for insertion in the transmit stream. When the microprocessor is updating the transmit page buffer, SPTB may be programmed to transmit null characters to prevent transmission of partial messages.

10.10.5 Transmit Path Overhead Processor (TPOP)

The Transmit Path Overhead Processor (TPOP) of TPPS provides transport frame alignment generation, path overhead insertion, insertion of the SPE, insertion of path level alarm signals and path BIP-8 (B3) insertion.

BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE (VC) of the outgoing STS-1 (STM-0/AU-3) or equivalent stream. The fixed stuff columns in the VC-3 format may be optionally excluded from BIP calculations. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

In processing a concatenated stream, the BIP-8 Calculate Block of the TPOP in the master TPPS will include calculated BIP-8 values from the slave TPPSs in the final computation of the path BIP-8 (B3) value of the stream.

Path REI Calculate

The Path REI Calculate Block accumulates path REIs on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the path REI bit positions of the path status (G1) byte. The path REI information is derived from path BIP-8 errors detected by the corresponding RPOP. The asynchronous nature of these signals implies that more than eight path REI events may be accumulated between transmit G1 bytes. If more than eight receive Path BIP-8 errors are accumulated between transmit G1 bytes, the accumulation counter is decremented by eight, and the remaining path REIs are transmitted at the next opportunity. Alternatively, path REI can be accumulated from path REI counts reported on the transmit alarm port when the local SPECTRA 4x155 is paired with a receive section of a remote SPECTRA 4x155. FEBE errors may be inserted under register control for diagnostic purposes. Optionally, path REI insertion may be disabled and the incoming G1 byte passes through unchanged to support applications where the received path processing does not reside in the local SPECTRA 4x155.

Path RDI Insert

Path RDI may be inserted via the TPOP block. The RDI codes to be inserted into the transmit stream may be supplied externally via the transmit Alarm Data Port (TAD) or may be automatically inserted via the receive side of the device and the detected receive alarms. The RXSEL register bits define the source of the RDI.

Transmit Alarm Port

Received path BIP errors (REI) and RDIs from the RPOPs in a remote SPECTRA 4x155 are communicated to the corresponding TPOP's in the local SPECTRA 4x155 via the transmit alarm port. When the port is enabled, the path BIP error count and the remote defect indication for each TPOP are sampled from the transmit alarm port and inserted in the path REI and path RDI positions of the path status byte (G1) in the transmit stream. The APS bytes K1/K2 received on the TAD port are inserted by the appropriate channel's TTOC.

The TAD port can accumulate up to 15 BIP errors. Given the timings of the RAD port, a mate SPECTRA 4x155 could output 16 errors within one frame period. If eight errors are detected in two consecutive frames and the timing makes them appear within one frame period, the 16th count could be lost.

SPE Multiplexer

The SPE Multiplexer Block multiplexes the payload pointer bytes, the SPE stream, and the path overhead bytes into the transmit stream. When in-band error reporting is enabled, the path REI and path RDI bits of the path status (G1) byte has already been formed by the corresponding Receive Path Overhead Processor and is transmitted unchanged.

10.11 Transmit Multiplexer (TX_REMUX)

The transmit multiplexer (TX_REMUX) block within each channel multiplexes the three STS-1(STM-1/AU3) streams or three equivalent STS-1(STM1/AU3) streams into an STS-3(STM-1/AU3) or STS-3c(STM1/AU4) stream. In the case of an STS-3(STM1/AU3) stream, the STS-1(STM1/AU3) streams are fed in from three master TPPSs. In the case of an STS-3c(STM1/AU4) stream, the equivalent STS-1(STM1/AU3) streams are fed in from one master TPPS and two slave TPPSs. The slave slices feed in the equivalent STS-1 #2 and #3.

The multiplexer also generates the low speed clock used to time the data stream out of the slices.

10.12 Transmit Transport Overhead Controller (TTOC)

The Transmit Transport Overhead Controller block (TTOC) allows the transmit transport overhead bytes (manually), the section or line BIP errors, or payload pointer byte errors to be inserted.

The complete transport overhead to be inserted at once per channel using TTOH1-4, along with the nominal 5.184 MHz transport overhead clock, TTOHCLK1-4, and the transport overhead frame position, TTOHFP1-4. The transport overhead enable signal, TTOHEN1-4, controls the insertion of transport overhead from TTOH1-4.

The APS bytes K1/K2 received via the TAD port may be optionally inserted via the TTOC logic. The received K1/K2 on TAD match the transmitted K1/K2 that a mate SPECTRA transmitted.

Individual data channels can be sourced from TSLD1-4. TTOHFP1-4 can be used to identify the required byte alignment on the serial inputs.

The TTOC block also allows the Unused and National Use bytes in the SONET/SDH TOH to be set. Refer to Figure 8. Specific registers exist to program fixed values in the Z0 bytes and the S1 byte of the TOH. The REI in the M1 byte may also be manually set by the TTOH1-4 input.

Figure 8 Unused and National Use Bytes

		1	2	3	1	2	3	1	2	3
Section	1	A1	A1	A1	A2	A2	A2	J0	Z0	Z0
	2	B1			E1			F1		
	3	D1			D2			D3		
Line	4	H1	H1	H1	H2	H2	H2	H3	H3	H3
	5	B2	B2	B2	K1			K2		
	6	D4			D5			D6		
	7	D7			D8			D9		
	8	D10			D11			D12		
	9	S1	Z1	Z1	Z2	Z2	M1	E2		

National Bytes
Unused Bytes

The National overhead bytes are defined:

- Z0 bytes of STS-1 #2 and #3.
- F1 byte positions of STS-1 #2 and #3.
- E2 byte positions of STS-1 #2 and #3.

The Unused overhead bytes are defined:

- B1 byte positions of STS-1 #2 and #3.
- E1 byte positions of STS-1 #2 and #3.
- D1 to D3 byte positions of STS-1 #2 and #3.
- K1 and K2 byte positions of STS-1 #2 and #3.
- D4 to D12 byte positions of STS-1 #2 and #3.
- Z1 bytes of STS-1 #2 and #3.
- Z2 bytes of STS-1 #1 and #2.

10.13 Transmit Line Overhead Processor (TLOP)

The Transmit Line Overhead Processor block (TLOP) processes the line overhead of a transmit STS-3 (STM-1) stream.

10.13.1 APS Insert

The APS Insert Block of TLOP inserts the two APS channel bytes of the Line Overhead (K1 and K2) into the transmit stream when enabled by an internal register. The inserted K1 and K2 may also be overwritten via insertion by the TTOC block.

10.13.2 Line BIP Calculate

The Line BIP Calculate Block of TLOP calculates the line BIP-24 error detection code (B2) based on the line overhead and SPE of the transmit stream. The line BIP-24 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-24 code is inserted into the B2 byte positions of the following frame. BIP-24 errors may be continuously inserted under register control for diagnostic purposes. Errors may be inserted in the B2 code for diagnostic purposes.

10.13.3 Line RDI Insert

The Line RDI Insert Block of TLOP controls the insertion of RDI. Line RDI may be inserted in the transmit stream under the control of an external input (TLRDI1-4), or a writeable register. The bits in the SPECTRA 4x155 Line RDI Control Register control the immediate insertion of Line RDI upon detection of various errors in the received SONET/SDH stream. Line RDI may also be inserted when enabling the Transmit Ring Control port (TRCP) and by setting high the SENDLRDI bit position. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in the transmit stream.

10.13.4 Line REI Insert

The Line REI Insert Block of TLOP accumulates line BIP-24 errors (B2) detected by the Receive Line Overhead Processor and encodes remote error indications in the transmit M1 byte. Line REI may be inserted automatically in the SONET/SDH stream under the control of the AUTOLREI bit in the SPECTRA 4x155 Ring Control Register. Receive B2 errors are accumulated and optionally inserted automatically in bits 2 to 8 of the third Z2/M1 byte of the transmit STS-3 (STM-1) stream. Up to 24 errors may be inserted per frame.

Line REI may also be inserted when enabling the Transmit Ring Control port (TRCP) and by setting high the REI bit positions.

10.14 Transmit Section Overhead Processor (TSOP)

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion. The TSOP block operates with a downstream serializer (the PISO block) that accepts the transmit stream in byte serial format and serializes it at the line rate.

10.14.1 Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame being set to “one” before scrambling except for the section overhead. The Line AIS Insert Block of TSOP substitutes all-ones as described when enabled through an internal register or he AIS may optionally be inserted into the data stream under the control of an external input (TLAIS). Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

10.14.2 BIP-8 Insert

The BIP-8 Insert Block of TSOP calculates and inserts the BIP-8 error detection code (B1) into the transmit stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-3 (STM-1) frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

10.14.3 Framing and Identity Insert

The Framing and Identity Insert Block of TSOP inserts the framing bytes (A1, A2) and trace/growth bytes (J0/Z0) into the STS-3 (STM-1) frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

10.14.4 Scrambler

The Scrambler Block of TSOP uses a frame synchronous scrambler to process the transmit stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $x^7 + x^6 + 1$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

10.15 Transmit Section Trace Buffer (SSTB)

The transmit portion of the SONET/SDH Section Trace Buffer (SSTB) sources the section trace identifier message (J0) for the Transmit Transport Overhead Access block. The length of the trace message is selectable between 16-bytes and 64-bytes. The section trace buffer contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and delivered serially to the Transport Overhead Access block for insertion in the transmit stream. When the microprocessor is updating the transmit page buffer, the buffer may be programmed to transmit null characters to prevent transmission of partial messages.

10.16 Transmit Line Interface

The Transmit Line Interface allows to directly interface the SPECTRA 4x155 with optical modules (ODLs) or other medium interfaces. This block performs clock synthesis and parallel-to-serial conversion on the outgoing 155.52 Mbit/s data stream.

10.16.1 Clock Synthesis

The transmit clock of the SSTB block may be synthesized from a 19.44 MHz reference. The PLL filter transfer function is optimized to enable the PLL to track the reference, yet attenuate high frequency jitter on the reference signal. This transfer function yields a typical low pass corner of ~~TBD~~ 2 MHz, above which reference jitter is attenuated at ~~TBD~~ 12 dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free reference, the intrinsic jitter is less than ~~TBD~~ 0.01 UI RMS when measured using a band pass filter with a low cutoff frequency of 12 KHz and a high cutoff frequency of 1.3 MHz.

10.16.2 Parallel-to-Serial Converter (PISO)

The Parallel to Serial Converter (PISO) of SSTB converts the transmit byte serial stream to a bit serial stream. The transmit bit serial stream appears on the TXD1-4+/- PECL output.

10.17 Add/Drop Bus Time-Slot Interchange (TSI)

The Time-Slot Interchange (TSI) logic at the Telecom Add and Drop buses supports the grooming of the corresponding receive and transmit SONET/SDH streams by performing column (time-slot) switching in those streams. The Add or Drop bus TSI logic treats the four channels STS-3 (STM-1) SONET/SDH streams as consecutive blocks consisting of 12 independent time-division multiplexed columns (time-slots) of data. The 12 columns correspond to the 12 constituent STS-1 (STM-0/AU-3) or equivalent payload streams. The relationship between the columns and the payload streams is summarized in the columns and STS-1 (STM-0/AU-3) streams association table Table 6. The columns are numbered in the order of transmission (reception) and the corresponding payload streams are labeled according to their STS-3 (STM-1) channel and STS-1 (STM-0/AU-3) sub-group.

Table 6 Columns and STS-1 (STM-0/AU-3) Streams Association.

Column # (Tx/Rx Order)	STS-1 (STM-0/AU-3) Streams
1	Channel/STS-3 (STM-1) #1, STS-1 (STM-0/AU-3) #1
2	Channel/STS-3 (STM-1) #2, STS-1 (STM-0/AU-3) #1
3	Channel/STS-3 (STM-1) #3, STS-1 (STM-0/AU-3) #1
4	Channel/STS-3 (STM-1) #4, STS-1 (STM-0/AU-3) #1
5	Channel/STS-3 (STM-1) #1, STS-1 (STM-0/AU-3) #2
6	Channel/STS-3 (STM-1) #2, STS-1 (STM-0/AU-3) #2
7	Channel/STS-3 (STM-1) #3, STS-1 (STM-0/AU-3) #2
8	Channel/STS-3 (STM-1) #4, STS-1 (STM-0/AU-3) #2
9	Channel/STS-3 (STM-1) #1, STS-1 (STM-0/AU-3) #3
10	Channel/STS-3 (STM-1) #2, STS-1 (STM-0/AU-3) #3
11	Channel/STS-3 (STM-1) #3, STS-1 (STM-0/AU-3) #3
12	Channel/STS-3 (STM-1) #4, STS-1 (STM-0/AU-3) #3

Switching of columns (time-slots) is arbitrary, thus any column can be switched to any of the time-slots. Concatenated streams should be switched as a group to keep the constituent STS-1 (STM-0/AU-3) streams in the correct transmit or receive order within the group.

The software configuration of the Add or Drop bus TSI logic to perform grooming at the respective Add or Drop buses is described in the Operations section.

10.17.1 Drop TSI

On the Drop side, the Drop bus TSI logic grooms the four STS-3/3c (STM-1/AU-3/AU-4) receive streams provided by the 12 RPPSs into the corresponding column of a Drop bus stream. The Drop TSI also generates the STS-1 rate clocks into the RPPS from the Drop DCK clock. 12 staggered clocks are generated sequencing the order of data out of the 12 slices. The staggered clocks and clock divider are slave to the Drop bus frame alignment and DFP. A frame realignment caused by moving the DFP pulse position will reset the staggered clock generator and briefly corrupt the data sequencing out of the RPPSs. The Drop TSI also sets the frame alignment of the STS-1 or STS-1 equivalent frames out of the slices. It does so by forcing the alignment on the output of the RTAL FIFO.

10.17.2 Add TSI

Similarly, on the Add side, the Add bus TSI logic grooms the 12 columns of the Add bus stream provided by the TelecomBus Interface into the corresponding channel's STS-3/3c (STM-1/AU-3/AU-4) transmit stream to be processed by the 12 TPPSs. Similarly to the Drop TSI, the Add TSI generates the STS-1 rate clocks into the TPPSs from the Add ACK clock. 12 staggered clocks are generated sequencing the order of data into the 12 slices. The staggered clocks and clock divider are slave to the Add BUS #1 frame alignment (AC1J1V1_AFP[1]). A frame realignment caused by moving the C1/FP pulse position will reset the staggered clock generator and briefly corrupt the data sequencing into the TPPSs.

The dependence of the staggered clock generator on the C1/FP pulse position of the Add Bus #1 may be disabled via the ATSI_ISOLATE register bit. This bit is present to allow the generation of Autonomous mode PRBS on the transmit line without the need for a valid Add Bus.

10.18 System Side Interfaces

10.18.1 TelecomBus Interface

The TelecomBus Interface supports a single 77.76 MHz byte Telecom bus or four 19.44 MHz byte Telecom bus modes. It performs multiplexing and demultiplexing to support four STS-3/3c (STM-1/AU-3/AU-4) channels.

For the four STS-3/3c (STM-4/AU-3/AU-4) receive streams, the TelecomBus interface multiplexes the Drop side data streams from the Drop bus TSI logic at the STS-1 (STM-0/AU-3) rate and provides the combined data stream (the groomed receive stream) to the Drop bus configured as a single 77.76 MHz byte Telecom bus (referred as the STM-4 Telecom bus mode) or four 19.44 MHz byte Telecom buses (referred as the STM-1 Telecom bus mode). For the STM-4 Telecom bus mode, all four constituent STM-1 channels (Channel #1 - #4) are presented at the single 77.76 MHz Drop bus (DD[7:0]). For the STM-1 byte Telecom bus mode, the Drop bus Channel#1, Channel#2, Channel#3 and Channel#4 streams are presented at the DD[7:0], DD[15:8], DD[23:16], and DD[31:24] buses, respectively.

For the four STS-3/3c (STM-4/AU-3/AU-4) transmit streams, the Telecom bus interface accepts a byte stream from the single 77.76 MHz (STM-4) Telecom Add bus or four byte streams from the four 19.44 MHz (STM-1) byte Telecom Add buses. The byte streams are de-multiplexed into 12 STS-1 (STM-0/AU-3) equivalent streams and presented to the Add bus TSI logic for grooming. The four groomed Add buses STS-3 (STM-1) streams are then processed and transmitted. For the STM-4 Telecom bus mode, all four constituent STM-1 channels (Channel#1 - 4) are sourced from the single 77.76 MHz Add bus (AD[7:0]). For the STM-1 byte Telecom bus modes, the Add bus Channel #1, Channel #2, Channel #3 and Channel #4 streams are sourced from the AD[7:0], AD[15:8], AD[23:16], and AD[31:24] buses, respectively.

The transport frames of the STM-1 Drop buses can be aligned by the DFP frame pulse. On the Add side, the transport frames of the STM-1 Add buses in the group must be aligned (coincident C1/AFP pulses on the associated AC1J1V1/AFP signals).

The TelecomBus is very flexible and can support a wide range of system backplane architectures Table 7 shows the system side Add bus options:

Table 7 System Side Add Bus Configuration Options

AFPEN Bit	DISJ1V1 Bit	APL[4:1] Input Pin	AC1J1V1[4:1]/ AFP[4:1] Input Pin	Comments
0	0	APL marks payload bytes	AC1J1V1 marks C1, J1 and V1 positions	TPIP block is bypassed.
0	1	Tied to ground	AC1J1V1 marks C1 position only	TPIP block interprets pointers for J1/V1
0	1	APL marks payload bytes	AC1J1V1 marks C1 position only	TPIP block interprets pointers for J1/V1
0	1	APL marks payload bytes	AC1J1V1 marks C1, J1 and V1 positions	TPIP block interprets pointers for J1/V1. Ignores J1/V1 indications on AC1J1V1
1	X	Tied to ground	AFP marks first SPE byte position only	TPIP block interprets pointers for J1/V1

Table 8 shows the system side Drop bus options:

Table 8 System Side Drop Bus Configuration Options

ENDV1	DPL[4:1]	DC1J1V1[4:1]
0	DPL marks payload bytes	DC1J1V1 marks C1, J1 and V1 positions
1	DPL marks payload bytes	DC1J1V1 marks C1 and J1 positions only

10.19 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The SPECTRA 4x155 identification code is 053130CD hexadecimal.

10.20 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the generic microprocessor bus with the normal mode and test mode registers within the SPECTRA 4x155. The normal mode registers are used during normal operation to configure and monitor the SPECTRA 4x155. The test mode registers are used to enhance the testability of the SPECTRA 4x155. The register set is accessed as shown in the Table 9. In the following section every register is documented and identified using the register numbers in Table 9. The corresponding memory map address is identified by the “address” column of Table 9.

Address mapping for the control and status registers and the registers of the Transport Overhead processing blocks (RSOP, RLOP, SSTB, RASE, TSOP, TLOP) is equivalent for each of the four channels of the device. The address space for the registers of the Transport Overhead processing blocks spans the addresses A[13:11]=0 and A[10:8]=**m** for 1≤**m**≤4. The variable **m** represents the channel number or index.

Similarly the address mapping is identical within each Receive and Transmit Path Processing Slices (RPPS & TPPS). The Address space of the 12 RPPS and TPPS slices span the addresses where A[13:12]=1 and A[11:8]=**n** where 1≤**n**≤12 (1H≤**n**≤CH). The variable **n** represents the slice number or index.

Table 9 Register Memory Map

REG #	AddressA[13:0]	Register Description
0000H	0000H	SPECTRA 4x155 Reset, Identity and Accumulation Trigger.
0001H	0001H	Master Clock Activity Monitor
0002H	0002H	Master Clock Control
0003H	0003H	Master Interrupt Status
0004H	0004H	Path Processing Slice Interrupt Status #1
0005H	0005H	Path Processing Slice Interrupt Status #2
0006H	0006H	Path Processing Slice Interrupt Status #3
0007H	0007H	Path Reset
000AH	000AH	Free

REG #	AddressA[13:0]	Register Description
0010H	0010H	CSPI Control and Status
0011H	0011H	CSPI Reserved
0012H-00FFH	0012H-00FFH	Reserved
0100H	0**m**00H	Channel Identity, Reset & Accumulation Trigger
0101H	0**m**01H	Line Configuration #1
0102H	0**m**02H	Line Configuration #2
0103H	0**m**03H	Receive Line AIS Control
0104H	0**m**04H	Ring Control
0105H	0**m**05H	Transmit Line RDI Control
0106H	0**m**06H	Section Alarm Output Control #1
0107H	0**m**07H	Section Alarm Output Control #2
0108H	0**m**08H	Section/Line Block Interrupt Status
0109H	0**m**09H	Auxiliary Section/Line Interrupt Enable
010AH	0**m**0AH	Auxiliary Section/Line Interrupt Status
010BH	0**m**0BH	Auxiliary Signal Interrupt Enable
010CH	0**m**0CH	Auxiliary Signal Status/Interrupt Status
0110H	0**m**10H	CRSI Configuration and Interrupt Status
0111H	0**m**11H	CRSI reserved
0112H-0113H	0**m**12H-0**m**13H	Reserved
0114H	0**m**14H	RSOP Control and Interrupt Enable
0115H	0**m**15H	RSOP Status and Interrupt
0116H	0**m**16H	RSOP Section BIP (B1) Error Count #1
0117H	0**m**17H	RSOP Section BIP (B1) Error Count #2
0118H	0**m**18H	RLOP Control and Status
0119H	0**m**19H	RLOP Interrupt Enable and Status
011AH	0**m**1AH	RLOP Line BIP (B2) Error Count #1
011BH	0**m**1BH	RLOP Line BIP (B2) Error Count #2
011CH	0**m**1CH	RLOP Line BIP (B2) Error Count #3
011DH	0**m**1DH	RLOP Line REI Error Count #1
011EH	0**m**1EH	RLOP Line REI Error Count #2
011FH	0**m**1FH	RLOP Line REI Error Count #3
0120H	0**m**20H	SSTB Section Trace Control
0121H	0**m**21H	SSTB Section Trace Status
0122H	0**m**22H	SSTB Section Trace Indirect Address
0123H	0**m**23H	SSTB Section Trace Indirect Data
0124H	0**m**24H	SSTB Reserved
0125H	0**m**25H	SSTB Reserved
0126H	0**m**26H	SSTB Section Trace Operation

REG #	AddressA[13:0]	Register Description
0127H-012FH	0**m**27H-0**m**2FH	SSTB Reserved
0130H	0**m**30H	RTOC Overhead Control
0131H	0**m**31H	RTOC AIS Control
0132H-0137H	0**m**32H-0**m**37H	RTOC Reserved
0138H-013FH	0**m**38H-0**m**3FH	Reserved
0140H	0**m**40H	RASE Interrupt Enable
0141H	0**m**41H	RASE Interrupt Status
0142H	0**m**42H	RASE Configuration/Control
0143H	0**m**43H	RASE SF Accumulation Period
0144H	0**m**44H	RASE SF Accumulation Period
0145H	0**m**45H	RASE SF Accumulation Period
0146H	0**m**46H	RASE SF Saturation Threshold
0147H	0**m**47H	RASE SF Saturation Threshold
0148H	0**m**48H	RASE SF Declaring Threshold
0149H	0**m**49H	RASE SF Declaring Threshold
014AH	0**m**4AH	RASE SF Clearing Threshold
014BH	0**m**4BH	RASE SF Clearing Threshold
014CH	0**m**4CH	RASE SD Accumulation Period
014DH	0**m**4DH	RASE SD Accumulation Period
014EH	0**m**4EH	RASE SD Accumulation Period
014FH	0**m**4FH	RASE SD Saturation Threshold
0150H	0**m**40H	RASE SD Saturation Threshold
0151H	0**m**51H	RASE SD Declaring Threshold
0152H	0**m**52H	RASE SD Declaring Threshold
0153H	0**m**53H	RASE SD Clearing Threshold
0154H	0**m**54H	RASE SD Clearing Threshold
0155H	0**m**55H	RASE Receive K1
0156H	0**m**56H	RASE Receive K2
0157H	0**m**57H	RASE Receive Z1/S1
0158H-017FH	0**m**58H-0**m**7FH	Reserved
0180H	0**m**80H	TSOP Control
0181H	0**m**81H	TSOP Diagnostic
0182H-0183H	0**m**82H-0**m**83H	TSOP Reserved
0184H	0**m**84H	TLOP Control
0185H	0**m**85H	TLOP Diagnostic
0186H	0**m**86H	TLOP Transmit K1

REG #	AddressA[13:0]	Register Description
0187H	0**m**87H	TLOP Transmit K2
0188H	0**m**88H	TTOC Transmit Overhead Output Control
0189H	0**m**89H	TTOC Transmit Overhead Byte Control
018AH	0**m**8AH	TTOC Transmit Z0
018BH	0**m**8BH	TTOC Transmit S1
018CH-018FH	0**m**8CH-0**m**8FH	TTOC Reserved
0190H-019FH	0**m**90H-0**m**9FH	Reserved
01A0H-01BFH	0**m**A0H-0**m**BFH	Reserved
01C0H-01DFH	0**m**C0H-0**m**DFH	Reserved
01E0H-01FFH	0**m**E0H-0**m**FFH	Reserved
0200H-04FFH	0200H-04FFH	Reserved
0500H-051FH	0500H-051FH	Reserved
0520H-053FH	0520H-053FH	Reserved
0540H -055FH	0540H -055FH	Reserved
0560H-1000H	0560H-1000H	Reserved
1001H	1001H	Drop Bus STM-1 #1 AU-3 #1 Select
1002H	1002H	Drop Bus STM-1 #2 AU-3 #1 Select
1003H	1003H	Drop Bus STM-1 #3 AU-3 #1 Select
1004H	1004H	Drop Bus STM-1 #4 AU-3 #1 Select
1005H	1005H	Drop Bus STM-1 #1 AU-3 #2 Select
1006H	1006H	Drop Bus STM-1 #2 AU-3 #2 Select
1007H	1007H	Drop Bus STM-1 #3 AU-3 #2 Select
1008H	1008H	Drop Bus STM-1 #4 AU-3 #2 Select
1009H	1009H	Drop Bus STM-1 #1 AU-3 #3 Select
100AH	100AH	Drop Bus STM-1 #2 AU-3 #3 Select
100BH	100BH	Drop Bus STM-1 #3 AU-3 #3 Select
100CH	100CH	Drop Bus STM-1 #4 AU-3 #3 Select
100DH-101FH	100DH-101FH	Drop Bus Reserved
1020H	1020H	Drop DLL
1021	1021H	Reserved
1022	1022H	Reserved
1023H	1023H	Drop DLL

REG #	AddressA[13:0]	Register Description
1024H-102FH	1024H-102FH	Reserved
1030H	1030H	Drop Bus Configuration
1031H-1080H	1031H-1080H	Reserved
1081H	1081H	Add Bus STM-1 #1 AU-3 #1 Select
1082H	1082H	Add Bus STM-1 #2 AU-3 #1 Select
1083H	1083H	Add Bus STM-1 #3 AU-3 #1 Select
1084H	1084H	Add Bus STM-1 #4 AU-3 #1 Select
1085H	1085H	Add Bus STM-1 #1 AU-3 #2 Select
1086H	1086H	Add Bus STM-1 #2 AU-3 #2 Select
1087H	1087H	Add Bus STM-1 #3 AU-3 #2 Select
1088H	1088H	Add Bus STM-1 #4 AU-3 #2 Select
1089H	1089H	Add Bus STM-1 #1 AU-3 #3 Select
108AH	108AH	Add Bus STM-1 #2 AU-3 #3 Select
108BH	108BH	Add Bus STM-1 #3 AU-3 #3 Select
108CH	108CH	Add Bus STM-1 #4 AU-3 #3 Select
108DH-10AFH	108DH-10AFH	Add Bus Reserved
10B0H	10B0H	Add Bus Configuration #1
10B1H	10B1H	Add Bus Configuration #2
10B2H	10B2H	Add Bus Parity Interrupt Enable
10B3H	10B3H	Reserved
10B4H	10B4H	Add Bus Parity Interrupt Status
10B5H	10B5H	Reserved
10B6H	10B6H	System Side Clock Activity
10B7H	10B7H	Add Bus Signal Activity Monitor
10B8H-10FFH	10B8H-10FFH	Reserved
1100H	1**n**00H	RPPS Configuration & Slice ID
1101H	1**n**01H	RPPS Reserved
1102H	1**n**02H	RPPS Path Configuration
1103H-110FH	1**n**03H-1**n**0FH	RPPS Reserved
1110H	1**n**10H	RPPS Path AIS Control #1
1111H	1**n**11H	RPPS Path AIS Control #2
1112H-1113H	1**n**12H-1**n**13H	RPPS Reserved
1114H	1**n**14H	RPPS Path REI/RDI Control #1
1115H	1**n**15H	RPPS Path REI/RDI Control #2
1116H-1117H	1**n**16H-1**n**17H	RPPS Reserved

REG #	AddressA[13:0]	Register Description
1118H	1**n**18H	RPPS Path Enhanced RDI Control #1
1119H	1**n**19H	RPPS Path Enhanced RDI Control #2
111AH-111BH	1**n**1AH-1**n**1BH	RPPS Reserved
111CH	1**n**1CH	RPPS RALM Output Control #1
111DH	1**n**1DH	RPPS RALM Output Control #2
111EH-1127H	1**n**1EH-1**n**27H	RPPS Reserved
1128H	1**n**28H	RPPS Path Interrupt Status
1129H-112BH	1**n**29H-1**n**2BH	RPPS Reserved
112CH	1**n**2CH	RPPS Auxiliary Path Interrupt Enable #1
112DH	1**n**2DH	RPPS Auxiliary Path Interrupt Enable #2
112EH-112FH	1**n**2EH-1**n**2FH	RPPS Reserved
1130H	1**n**30H	RPPS Auxiliary Path Interrupt Status #1
1131H	1**n**31H	RPPS Auxiliary Path Interrupt Status #2
1132H-1133H	1**n**32H-1**n**33H	RPPS Reserved
1134H	1**n**34H	RPPS Auxiliary Path Status
1135H-113FH	1**n**35H-1**n**3FH	RPPS Reserved
1140H	1**n**40H	RPOP Status and Control (EXTD=0)
		RPOP Status and Control (EXTD=1)
1141H	1**n**41H	RPOP Alarm Interrupt Status (EXTD=0)
		RPOP Alarm Interrupt Status (EXTD=1)
1142H	1**n**42H	RPOP Pointer Interrupt Status
1143H	1**n**43H	RPOP Alarm Interrupt Enable (EXTD=0)
		RPOP Alarm Interrupt Enable (EXTD=1)
1144H	1**n**44H	RPOP Pointer Interrupt Enable
1145H	1**n**45H	RPOP Pointer LSB
1146H	1**n**46H	RPOP Pointer MSB
1147H	1**n**47H	RPOP Path Signal Label
1148H	1**n**48H	RPOP Path BIP-8 Count LSB
1149H	1**n**49H	RPOP Path BIP-8 Count MSB
114AH	1**n**4AH	RPOP Path REI Count LSB
114BH	1**n**4BH	RPOP Path REI Count MSB
114CH	1**n**4CH	RPOP Tributary Multi-frame Status and Control
114DH	1**n**4DH	RPOP Ring Control
114EH	1**n**4EH	Reserved
114FH	1**n**4FH	Reserved

REG #	AddressA[13:0]	Register Description
1150H-1153H	1**n**50H-1**n**53H	PMON Reserved
1154H	1**n**54H	PMON Receive Positive Pointer Justification Count
1155H	1**n**55H	PMON Receive Negative Pointer Justification Count
1156H	1**n**56H	PMON Transmit Positive Pointer Justification Count
1157H	1**n**57H	PMON Transmit Negative Pointer Justification Count
1158H	1**n**58H	RTAL Control
1159H	1**n**59H	RTAL Interrupt Status and Control
115AH	1**n**5AH	RTAL Alarm and Diagnostic Control
115BH	1**n**5BH	RTAL Reserved
115CH-115FH	1**n**5CH-1**n**5FH	Reserved
1160H	1**n**60H	SPTB Control
1161H	1**n**61H	SPTB Path Trace Identifier Status
1162H	1**n**62H	SPTB Indirect Address
1163H	1**n**63H	SPTB Indirect Data
1164H	1**n**64H	SPTB Expected Path Signal Label
1165H	1**n**65H	SPTB Path Signal Label Status
1166H	1**n**66H	SPTB Path Trace Indirect Access Trigger
1167H	1**n**67H	SPTB Reserved
1168H-116FH	1**n**68H-1**n**6FH	Reserved
1170H	1**n**70H	DPGM Generator Control #1
1171H	1**n**71H	DPGM Generator Control #2
1172H	1**n**72H	DPGM Generator Concatenate Control
1173H	1**n**73H	DPGM Generator Status
1174H-1177h	1**n**74H-1177H	DPGM Reserved
1178H	1**n**78H	DPGM Monitor Control #1
1179H	1**n**79H	Reserved
117AH	1**n**7AH	DPGM Monitor Concatenate Control
117BH	1**n**7BH	DPGM Monitor Status
117CH	1**n**7CH	DPGM Monitor Error Count #1
117DH	1**n**7DH	DPGM Monitor Error Count #2
117BH-117FH	1**n**7BH-1**n**7FH	DPGM Reserved
1180H	1**n**80H	TPPS Configuration
1181H	1**n**81H	TPPS Reserved
1182H	1**n**82H	TPPS Path Configuration
1183H-1185H	1**n**83H-1**n**85H	TPPS Reserved
1186H	1**n**86H	TPPS Path Transmit Control

REG #	AddressA[13:0]	Register Description
1187H-118FH	1**n**87H-1**n**8FH	TPPS Reserved
1190H	1**n**90H	TPPS Path AIS Control
1191H-11A7H	1**n**91H-1**n**A7H	TPPS Reserved
11A8H	1**n**A8H	TPPS Path Interrupt Status
11A9H-11ABH	1**n**A9H-1**n**ABH	TPPS Reserved
11ACH	1**n**ACH	TPPS Auxiliary Path Interrupt Enable
11ADH-11AFH	1**n**ADH-1**n**AFH	TPPS Reserved
11B0H	1**n**B0H	TPPS Auxiliary Path Interrupt Status
11B1H-11BFH	1**n**B1H-1**n**BFH	TPPS Reserved
11C0H	1**n**C0H	TPOP Control
11C1H	1**n**C1H	TPOP Pointer Control
11C2H	1**n**C2H	TPOP Reserved
11C3H	1**n**C3H	TPOP Current Pointer LSB
11C4H	1**n**C4H	TPOP Current Pointer MSB
11C5H	1**n**C5H	TPOP Payload Pointer LSB
11C6H	1**n**C6H	TPOP Payload Pointer MSB
11C7H	1**n**C7H	TPOP Path Trace
11C8H	1**n**C8H	TPOP Path Signal Label
11C9H	1**n**C9H	TPOP Path Status
11CAH	1**n**CAH	TPOP Path User Channel
11CBH	1**n**CBH	TPOP Path Growth #1
11CCH	1**n**CCH	TPOP Path Growth #2
11CDH	1**n**CDH	Reserved
11CEH-11CFH	1**n**CEH-1**n**CFH	TPOP Reserved
11D0H	1**n**D0H	TTAL Control
11D1H	1**n**D1H	TTAL Interrupt Status and Control
11D2H	1**n**D2H	TTAL Alarm and Diagnostic Control
11D3H	1**n**D3H	TTAL Reserved
11D4H-11DFH	1**n**D4H-1**n**DFH	TPPS Reserved
11E0H	1**n**E0H	TPIP Status and Control (EXTD=0)
		TPIP Status and Control (EXTD=1)
11E1H	1**n**E1H	TPIP Alarm Interrupt Status
11E2H	1**n**E2H	TPIP Pointer Interrupt Status
11E3H	1**n**E3H	TPIP Alarm Interrupt Enable (EXTD=0)

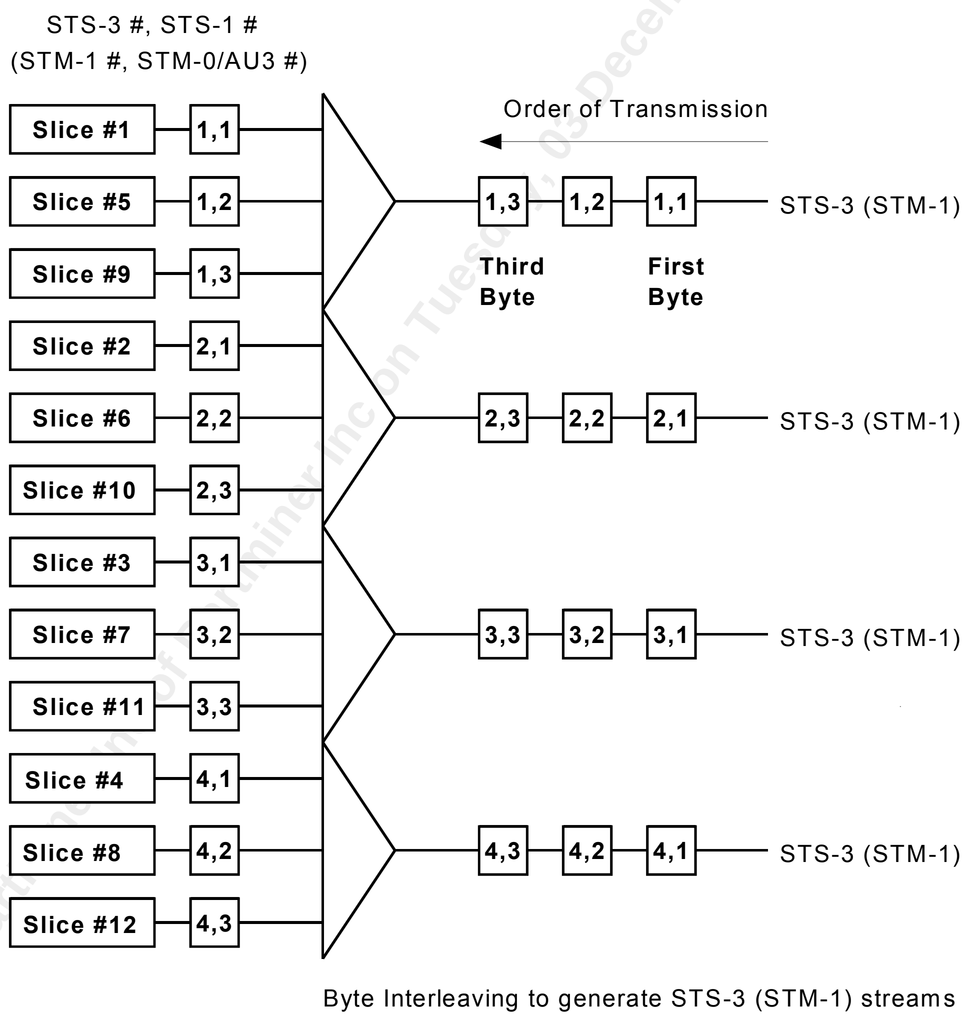
REG #	AddressA[13:0]	Register Description
		TPIP Alarm Interrupt Enable (EXTD=1)
11E4H	1**n**E4H	TPIP Pointer Interrupt Enable
11E5H	1**n**E5H	TPIP Pointer LSB
11E6H	1**n**E6H	TPIP Pointer MSB
11E7H	1**n**E7H	TPIP Reserved
11E8H	1**n**E8H	TPIP Path BIP-8 Count LSB
11E9H	1**n**E9H	TPIP Path BIP-8 Count MSB
11EAH-11EBH	1**n**EAH-1**n**EBH	TPIP Reserved
11ECH	1**n**ECH	TPIP Tributary Multi-frame Status and Control
11EDH	1**n**EDH	TPIP BIP Control
11EEH-11EFH	1**n**EEH-1**n**EFH	TPIP Reserved
11F0H	1**n**F0H	APGM Generator Control #1
11F1H	1**n**F1H	APGM Generator Control #2
11F2H	1**n**F2H	APGM Generator Concatenate Control
11F3H	1**n**F3H	APGM Generator Status
11F4H-11F7H	1**n**F4H-1**n**F7H	APGM Reserved
11F8H	1**n**F8H	APGM Monitor Control #1
11F9H	1**n**F9H	APGM Monitor Control #2
11FAH	1**n**FAH	APGM Monitor Concatenate Control
11FBH	1**n**FBH	APGM Monitor Status
11FCH	1**n**FCH	APGM Monitor Error Count #1
11FDH	1**n**FDH	APGM Monitor Error Count #2
11FEH-11FFH	1**n**FEH-1**n**FFH	APGM Reserved
1D00H	1D00H	Reserved
1FFFH	1FFFH	Reserved
2000H	2000H	Master Test
2001H	2001H	Master Test Slice Select
2002H	2002H	Reserved
2FFFH	2FFFH	Reserved

Notes

1. For all register accesses, CSB must be low.
2. Addresses that are not shown must be treated as Reserved.
3. A[13] is the test resister select (TRS) and should be set to logic zero for normal mode register access.

The Path Processing Slices and Order of Transmission diagram, illustrated in Figure 9, shows the relationship between the TPPSs and RPPSs and the corresponding SPE (VC) columns or bytes that they process. The SPE (VC) columns or bytes are labeled using an STS-3 (STM-1) group and STS-1 (STM-0/AU-3) sub-group numbering scheme, as they would appear in a STS-12 (STM-4) stream. The STS-3 (STM-1) number corresponds to the device channel. For example, to control the path processing of transmit STS-1 (STM-0/AU-3) #1 of the STS-3 (STM-1) #3 stream (channel #3), the register set of TPPS #7 in the address range of 1700H–17FFH must be used. Similarly, to access the path processing status of the same STS-1 (STM-0/AU-3) stream on the receive side, the register set of RPPS #7 in the address range of 0700H–07FFH must be accessed.

Figure 9 Path Processing Slices and Order of Transmission



11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the SPECTRA 4x155. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[13]) is low.

Notes on Normal Mode Register Descriptions

1. Writing to unused bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused register bits should be masked off by software when read.

2. All configuration bits that can be “written into” can also be “read back”. This allows the processor controlling the SPECTRA 4x155 to determine the programming state of the device.

3. Writeable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit-locations does not affect SPECTRA 4x155 operation unless otherwise noted.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the SPECTRA 4x155 operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

Register 0000H: SPECTRA 4x155 Reset, Identity and Accumulation Trigger

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R/W	Reserved	0
Bit 5	R	TIP	X
Bit 4	R	ID[4]	X
Bit 3	R	ID[3]	X
Bit 2	R	ID[2]	X
Bit 1	R	ID[1]	X
Bit 0	R	ID[0]	X

This register allows the revision number of the SPECTRA 4x155 to be read by software thereby allowing easy migration to newer, feature-enhanced versions of the SPECTRA 4x155.

A write to this register initiates the transfer of all PMON counter values in the RSOP, RLOP, PMON, RPOP, TPIP, DPGM, and APGM blocks to holding registers.

ID[4:0]

The version identification bits ID[4:0], are set to the value 00H, representing the version number of the SPECTRA 4x155.

TIP

The Transfer in Progress (TIP) bit is set to a logic one when the performance meter registers are being loaded. Writing to this register will initiate an accumulation interval transfer and loads all of the performance meter registers in the RSOP, RLOP, PMON, RPOP, TPIP, DPGM, and APGM blocks.

TIP remains high while the transfer is in progress and is set to logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

RESET

The RESET bit allows the SPECTRA 4x155 to be asynchronously reset under software control. If the reset bit is logic one, the entire SPECTRA–4x155 is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the SPECTRA 4x155 out of reset. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Register 0001H: Master Clock Activity Monitor

Bit	Type	Function	Default
Bit 7	R	REFCLKA	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register provides activity monitoring on SPECTRA 4x155 parallel line inputs. When a monitored input makes a low-to-high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register will be cleared. A lack of transition is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck-at conditions.

REFCLKA

The REFCLK active (REFCLKA) bit monitors for low-to-high transitions on the REFCLK reference clock input. REFCLKA is set high on a rising edge of REFCLK and is set low when this register is read.

Register 0002H: Master Clock Control

Bit	Type	Function	Default
Bit 7	R/W	PGMRCHSEL[1]	0
Bit 6	R/W	PGMRCHSEL[0]	1
Bit 5	R/W	RCLKEN	0
Bit 4	R/W	TCLKEN	0
Bit 3	R/W	PGMRCLKEN	0
Bit 2	R/W	PGMRCLKSEL	0
Bit 1	R/W	PGMTCLKEN	0
Bit 0	R/W	PGMTCLKSEL	0

This register controls the various line side output clocks generated for the SPECTRA 4x155.

PGMTCLKSEL

The PGMTCLKSEL bit selects the clock frequency of the PGMTCLK output. When PGMTCLKSEL is set low, PGMTCLK is a nominally 19.44 MHz clock. When PGMTCLKSEL is set high, PGMTCLK is a nominally 8 KHz clock.

PGMTCLKEN

The PGMTCLK enable (PGMTCLKEN) bit controls the gating of the PGMTCLK output. When PGMTCLKEN is set low, the PGMTCLK output is held low. When PGMTCLKEN is set high, the PGMTCLK output is allowed to operate normally.

PGMRCLKSEL

The PGMRCLKSEL bit selects the clock frequency of the PGMRCLK output. When PGMRCLKSEL is set low, PGMRCLK is a nominally 19.44 MHz clock. When PGMRCLKSEL is set high, PGMRCLK is a nominally 8 KHz clock.

PGMRCLKEN

The PGMRCLK enable (PGMRCLKEN) bit controls the gating of the PGMRCLK output. When PGMRCLKEN is set low, the PGMRCLK output is held low. When PGMRCLKEN is set high, the PGMRCLK output is allowed to operate normally.

TCLKEN

The TCLK enable (TCLKEN) bit controls the gating of the TCLK output. When TCLKEN is set low, the TCLK output is held low. When TCLKEN is set high, the TCLK output is allowed to operate normally.

RCLKEN

The RCLK enable (RCLKEN) bit controls the gating of the RCLK output. When RCLKEN is set low, the RCLK output is held low. When RCLKEN is set high, the RCLK output is allowed to operate normally.

PGMRCHSEL[1:0]

The PGMRCHSEL[1:0] bits select the timing source of the PGMRCLK output.

PGMRCHSEL[1:0]	PGMRCLK Source
01	Channel #1
10	Channel #2
11	Channel #3
00	Channel #4

Register 0003H: Master Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	MINTE	1
Bit 6	R	Reserved	X
Bit 5	R	PPSI	X
Bit 4	R	CHNL4I	X
Bit 3	R	CHNL3I	X
Bit 2	R	CHNL2I	X
Bit 1	R	CHNL1I	X
Bit 0	R	CSPII	X

When the interrupt output INTB goes low, this register allows the source of an active interrupt to be identified. Further register accesses are required for the channel in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

CSPII

The CSPII bit is set high when one or more of the maskable interrupt sources in the Clock Synthesis or the PISO block have been activated. This register bit remains high until the interrupt is acknowledged by reading the CSPI Clock Synthesis Control, Status and Interrupt register.

CHNL1I

The CHNL1I bit is high when an interrupt request is active from the transport overhead processing blocks of Channel #1. The Section/Line Block Interrupt Status register, Auxiliary Section/Line Interrupt Status register, and the Auxiliary Signal Status/Interrupt Status register of Channel #1 should be read to identify the source of the interrupt.

CHNL2I

The CHNL2I bit is high when an interrupt request is active from the transport overhead processing blocks of Channel #2. The Section/Line Block Interrupt Status register, Auxiliary Section/Line Interrupt Status register, and the Auxiliary Signal Status/Interrupt Status register of Channel #1 should be read to identify the source of the interrupt.

CHNL3I

The CHNL3I bit is high when an interrupt request is active from the transport overhead processing blocks of Channel #3. The Section/Line Block Interrupt Status register, Auxiliary Section/Line Interrupt Status register, and the Auxiliary Signal Status/Interrupt Status register of Channel #3 should be read to identify the source of the interrupt.

CHNL4I

The CHNL4I bit is high when an interrupt request is active from the transport overhead processing blocks of Channel #4. The Section/Line Block Interrupt Status register, Auxiliary Section/Line Interrupt Status register, and the Auxiliary Signal Status/Interrupt Status register of Channel #4 should be read to identify the source of the interrupt.

PPSI

The PPSI bit is high when an interrupt request is active from at least one of the RPPS or TPPS. The Path Processing Slice Interrupt Status #1-2-3 registers should be read to identify the source of the interrupt.

MINTE

The Master Interrupt Enable allows internal interrupt statuses to be propagated to the interrupt output. If MINTE is logic one, INTB will be asserted low upon the assertion of an interrupt status bit whose individual enable is set. If MINTE is logic zero, INTB is unconditionally high-impedance.

Register 0004H: Path Processing Slice Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R	RPPSI[8] (4,2)	X
Bit 6	R	RPPSI[7] (3,2)	X
Bit5	R	RPPSI[6] (2,2)	X
Bit 4	R	RPPSI[5] (1,2)	X
Bit 3	R	RPPSI[4] (4,1)	X
Bit 2	R	RPPSI[3] (3,1)	X
Bit 1	R	RPPSI[2] (2,1)	X
Bit 0	R	RPPSI[1] (1,1)	X

Register 0005H: Path Processing Slice Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R	RPPSI[12] (4,3)	X
Bit 6	R	RPPSI[11] (3,3)	X
Bit5	R	RPPSI[10] (2,3)	X
Bit 4	R	RPPSI[9] (1,3)	X
Bit 3	R	TPPSI[12] (4,3)	X
Bit 2	R	TPPSI[11] (3,3)	X
Bit 1	R	TPPSI[10] (2,3)	X
Bit 0	R	TPPSI[9] (1,3)	X

Register 0006H: Path Processing Slice Interrupt Status #3

Bit	Type	Function	Default
Bit 7	R	TPPSI[8] (4,2)	X
Bit 6	R	TPPSI[7] (3,2)	X
Bit5	R	TPPSI[6] (2,2)	X
Bit 4	R	TPPSI[5] (1,2)	X
Bit 3	R	TPPSI[4] (4,1)	X
Bit 2	R	TPPSI[3] (3,1)	X
Bit 1	R	TPPSI[2] (2,1)	X
Bit 0	R	TPPSI[1] (1,1)	X

The SPECTRA 4x155 Path Processing Slice Interrupt Status registers (#1, 2 and 3) are used to indicate the interrupt status of the 12 receive and 12 transmit path processing slices. A subsequent read of the RPPS Path Interrupt Status or TPPS Path Interrupt Status of the slice in interrupt reveals the source of the interrupt. The index numbers refer to the follow receive and transmit STS-1 (STM-0/AU-3)

Index	(STS-3, STS1) (STM-1, AU-3)	Index	(STS-3, STS1) (STM-1, AU-3)	Index	(STS-3, STS1) (STM-1, AU-3)
1	(1,1)	5	(1,2)	9	(1,3)

Index	(STS-3, STS1) (STM-1, AU-3)	Index	(STS-3, STS1) (STM-1, AU-3)	Index	(STS-3, STS1) (STM-1, AU-3)
2	(2,1)	6	(2,2)	10	(2,3)
3	(3,1)	7	(3,2)	11	(3,3)
4	(4,1)	8	(4,2)	12	(4,3)

RPPSI[12:1]

The Receive Path Processing Slice Interrupts (RPPSI[12:1]) are high when an interrupt request is active from the index number receive slice.

TPPSI[12:1]

The Transmit Path Processing Slice Interrupts (TPPSI[12:1]) are high when an interrupt request is active from the indexed number transmit slice.

Register 0007H: Path Reset

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RESET_PATH	0

RESET_PATH

The RESET_PATH bit allows the path processing blocks of the SPECTRA 4x155 to be asynchronously reset under software control. If the RESET_PATH bit is set to logic one, all Transmit Path Processing Slices (TPPS #1 to #12) and all Receive Path Processing Slices (RPPS #1 to #12) are held in reset. This is independent of all other processing blocks. This bit is not self-clearing. Therefore, a logic zero must be written to bring the slices out of reset. A hardware reset clears the RESET_PATH bit, thus negating the software reset.

Register 000AH: FREE

Bit	Type	Function	Default
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

FREE[7:0]

The FREE[7:0] register bits do not perform any function. They are free for user defined read/write operations.

Register 0010H: CSPI Control and Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R	TROOLI	X
Bit 4	—	Unused	X
Bit 3	R	TROOLV	X
Bit 2	—	Unused	X
Bit 1	R/W	TROOLE	0
Bit 0	R/W	Reserved	0

This register controls the clock synthesis and reports the state of the transmit PLL.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

TROOLE

The TROOLE bit is an interrupt enable for the transmit reference out of lock status. When TROOLE is set to logic one, an interrupt is generated when the TROOLV bit changes state.

TROOLV

The transmit reference out of lock status indicates the clock synthesis PLL is unable to lock to the reference on REFCLK. TROOLV is a logic one if the divided down synthesized clock frequency is not within 488 ppm of the REFCLK frequency. This bit will only be set to one just prior to affirming the out of locked state. The TROOLI interrupt bit should be used for a gross declaration of the clock's validity.

TROOLI

The TROOLI bit is the "transmit reference out of lock" interrupt status bit. TROOLI is set high when the TROOLV bit of the SPECTRA 4x155 Clock Synthesis Control and Status register changes state. TROOLV indicates the clock synthesis PLL is unable to lock to the reference on REFCLK and is a logic one if the divided down synthesized clock frequency is not within approximately 488 ppm of the REFCLK frequency. TROOLI is cleared when this register is read.

Register 0011H: CSPI Reserved

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

Register 0100H, 0200H, 0300H, and 0400H: Channel Reset, Identity and Accumulation Trigger

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	CHAN_TIP	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	CHAN_ID[1]	X
Bit 0	R	CHAN_ID[0]	X

Writing to this register initiates a transfer of all PMON counter values in the RSOP, RLOP, PMON, RPOP, DPGM, and APGM blocks on the indexed channel into holding registers.

CHAN_ID[1:0]

The CHAN_ID[1:0] bits indicate the channel number. These register bits exist for test purposes only. Reading register 0100h will return ‘00’, reading register 0200h will return ‘01’, reading register 0300h will return ‘10’ and reading register 0400h will return ‘11’.

CHAN_TIP

The Channel Transfer in Progress (TIP) bit is set to a logic one when the performance meter registers are being loaded. Writing to this register will initiate an accumulation interval transfer and loads all the performance meter registers in the RSOP, RLOP, PMON, RPOP, TPIP, DPGM and APGM blocks of the indexed channel.

CHAN_TIP remains high while the transfer is in progress, and is set to logic zero when the transfer is complete. CHAN_TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

Register 0101H, 0201H, 0301H, and 0401H: Line Configuration #1

Bit	Type	Function	Default
Bit 7	R/W	SLLE	0
Bit 6	R/W	SDLE	0
Bit 5	R/W	LOOPT	0
Bit 4	R/W	PDLE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	RESET_PATH	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register is used to configure the receive and transmit line side interfaces. Some of the following bits must not be programmed simultaneously.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

RESET_PATH

The RESET_PATH bit allows the path processing blocks of the indexed channel to be asynchronously reset under software control. If the RESET_PATH bit is set to logic one, all TPPSs and all RPPSs of the indexed channel are held in reset. Table 10 gives the correspondence between the channel number and the path processing slice number.

Table 10 Correspondence between Channel and Path Processing Slice Number

Channel ID	Path Slice ID
1	STS-1 (STM-0/AU-3) #1, #5 and #9
2	STS-1 (STM-0/AU-3) #2, #6 and #10 (0AH)
3	STS-1 (STM-0/AU-3) #3, #7 and #11 (0BH)
4	STS-1 (STM-0/AU-3) #4, #8 and #12 (0CH)

This is independent of all other processing blocks. This bit is not self-clearing. Therefore, a logic zero must be written to bring the slices out of reset. A hardware reset clears the RESET_PATH bit, thus negating the software reset.

PDLE

The PDLE bit enables the parallel diagnostic loop back. When PDLE is a logic one, the transmit parallel stream is connected to the receive stream on the indexed channel. The loop back point is between the TSOP and the RSOP of the indexed channel. Blocks upstream of the loop back point continue to operate normally. For example line AIS may be inserted in the transmit stream upstream of the loop back point using the TSOP.

LOOPT

The LOOPT bit selects the source of timing for the transmit section of the indexed channel. When LOOPT is a logic zero, the transmitter timing is derived from input REFCLK. When LOOPT is a logic one, the transmitter timing is derived from the recovered clock.

SDLE

The SDLE bit enables the serial diagnostic loop back of the indexed channel. When SDLE is a logic one, the transmit serial stream on the channel TXDm+/- differential outputs is internally connected to the received serial RXDm+/- differential inputs. The transmit serial stream is still output on TXDm+/-. The SDLE and the SLLE bits should not be set high simultaneously.

SLLE

The SLLE bit enables the line loop back of the indexed channel. When SLLE is a logic one, the recovered data from the receive serial RXDm+/- differential inputs is mapped to the TXDm+/- differential outputs. Blocks downstream of the loop back point continue to operate normally. The SDLE and the SLLE bits should not be set high simultaneously.

Register 0102H, 0202H, 0302H, and 0402H: Line Configuration #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Unused	0
Bit 5	R/W	Unused	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TXDINV	0
Bit 0	R/W	RXDINV	0

This register is used to configure the receive and transmit line side interfaces.

RXDINV

The receive inversion (RXDINV) controls the polarity of the receive data. When RXDINV is set high, the polarity of the RXDm+/- is inverted. When RXDINV is set low, the RXDm+/- inputs operate normally.

TXDINV

The transmit inversion TXDINV controls the polarity of the transmit data. When TXDINV is set high, the polarity of the TXDm+/- is inverted. When TXDINV is set low, the TXDm+/- outputs operate normally.

Register 0103H, 0203H, 0303H, and 0403H: Receive Line AIS Control

Bit	Type	Function	Default
Bit 7	R/W	SDAIS	0
Bit 6	R/W	SFAIS	0
Bit 5	R/W	LOFAIS	1
Bit 4	R/W	LOSAIS	1
Bit 3	R/W	RTIMAIS	0
Bit 2	R/W	RTIUAIS	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register enables various section and line alarms to control the insertion of line AIS just before or just after the RLOP block. This will result in the insertion of path AIS on the SPECTRA 4x155 Drop bus and the same downstream block alarms as when receiving line AIS from the fiber.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

RTIUAIS

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The RTIUAIS bit enables the insertion of path AIS in the Drop direction upon the declaration of section trace identifier (mode 1 or 2) “unstable”. If RTIUAIS is a logic one, path AIS is inserted into the indexed channel SONET/SDH frame when the SSTB declares a RTIU. Path AIS is terminated when the RTIU is removed

RTIMAIS

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The RTIMAIS bit enables the insertion of path AIS in the Drop direction upon the declaration of section trace identifier (mode 1) “mismatch”. If RTIMAIS is a logic one, path AIS is inserted into the indexed channel SONET/SDH frame when the accepted identifier message differs from the expected message. Path AIS is terminated when the accepted message matches the expected message.

LOSAIS

The LOSAIS bit enables the insertion of path AIS in the Drop direction upon the declaration of LOS. If LOSAIS is logic one, path AIS is inserted into the indexed channel SONET/SDH frame when LOS is declared. Path AIS is terminated when LOS is removed.

LOFAIS

The LOFAIS bit enables the insertion of path AIS in the Drop direction upon the declaration of LOF. If LOFAIS is a logic one, path AIS is inserted into the indexed channel SONET/SDH frame when LOF is declared. Path AIS is terminated when LOF is removed.

SFAIS

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The SFAIS bit enables the insertion of path AIS in the Drop direction upon the declaration of signal fail (SF). If SFAIS is a logic one, path AIS is inserted into the indexed SONET/SDH frame when SF is declared. Path AIS is terminated when SF is removed.

SDAIS

This bit is active only when the ALLONES bit in the RLOP Control/Status register is set high; it is ignored if the ALLONES bit is set low. The SDAIS bit enables the insertion of path AIS in the Drop direction upon the declaration of signal degrade (SD). If SDAIS is a logic one, path AIS is inserted into the indexed channel SONET/SDH frame when SD is declared. Path AIS is terminated when SD is removed.

Register 0104H, 0204H, 0304H, and 0404H: Ring Control

Bit	Type	Function	Default
Bit 7	R	INSLRDI	X
Bit 6	R	INSLAIS	X
Bit 5	R/W	RINGEN	0
Bit 4	R/W	AUTOLREI	0
Bit 3	R/W	RCPEN	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	SLRDI	0
Bit 0	R/W	SLAIS	0

SLAIS

The SLAIS bit controls the value of the SENDLAIS bit position in the receive ring control port stream of the indexed channel. The SLAIS bit is used to cause a mate SPECTRA 4x155 to send the line AIS maintenance signal under software control.

SLRDI

The SLRDI bit controls the value of the SENDLRDI bit position in the receive ring control port stream of the indexed channel. The SENDLRDI bit value is determined by the logical OR of this register bit along with the line RDI insertion events programmed in the Line RDI Control register. The SLRDI bit is used to cause a mate SPECTRA 4x155 to send the line RDI maintenance signal under software control.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

RCPEN

The RCPEN bit controls the enabling of the receive and transmit ring control ports of the indexed channel. When RCPEN is a logic zero, the ring control ports are disabled, and the LOS, LAIS and LRDI outputs and the RLAIS, TLAIS, and TLRDI inputs are used to monitor alarm status and control maintenance signal insertion. When RCPEN is a logic one, the ring control ports are enabled, and alarm status and maintenance signal insertion control is provided by the RRCPCLKm, RRCPFPm, and RRCPDATm outputs and the TRCPCLKm, TRCPFPm, and TRCPDATm inputs.

AUTOLREI

The AUTOLREI bit enables the automatic insertion/indication of line REI events to the mate transmitter (local or remote). When AUTOLREI is a logic one and the local ring control port of the indexed channel is disabled, receive B2 errors detected by the SPECTRA 4x155 are automatically inserted in the Z2/M1 byte of the transmit stream of the indexed channel. When AUTOLREI is a logic one and the remote ring control port is enabled, received B2 errors are output on the ring control port of the indexed channel for insertion in the Z2/M1 byte of the remote transmit stream.

When AUTOLREI is a logic zero, line REI events are not automatically inserted in the transmit stream nor indicated on the ring control port of the indexed channel. A Z2/M1 byte inserted from the transmit transport overhead port (using the TTOHEN input) takes precedence over the automatic insertion of line REI events.

RINGEN

The RINGEN bit controls the operation of the transmit ring control port of the indexed channel when the ring control ports are enabled by the RCPEN bit. When RINGEN is a logic one, the automatic insertion of line RDI, line AIS, and line REI is controlled by bit positions in the transmit ring control port input stream of the indexed channel.

When RINGEN is a logic zero, the insertion of line RDI is done automatically based on alarms detected by the receive portion of the SPECTRA 4x155 indexed channel. Also, line REI is inserted based on B2 errors detected by the receive portion of the SPECTRA 4x155 indexed channel.

INSLAIS

The INSLAIS bit reports the value of the SENDLAIS bit position in the transmit ring control port of the indexed channel. When the ring control ports are enabled, a logic one in this bit position indicates that the SPECTRA 4x155 is inserting the line AIS maintenance signal.

INSLRDI

The INSLRDI bit reports the value of the SENDLRDI bit position in the transmit ring control port of the indexed channel. When the ring control ports are enabled, a logic one in this bit position indicates that the SPECTRA 4x155 is inserting the line RDI maintenance signal.

Register 0105H, 0205H, 0305H, and 0405H: Transmit Line RDI Control

Bit	Type	Function	Default
Bit 7	R/W	SDLRDI	0
Bit 6	R/W	SFLRDI	0
Bit 5	R/W	LOFLRDI	1
Bit 4	R/W	LOSLRDI	1
Bit 3	R/W	RTIMLRDI	0
Bit 2	R/W	RTIULRDI	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAISLRDI	1

This register controls the alarms enabled to generate Line RDI in the transmit stream via the ring control port on a mate device or, automatically, in the same device.

LAISLRDI

The LAISLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port of the indexed channel upon the declaration of line AIS. When LAISLRDI is a logic one, the detection of line AIS results in the insertion of line RDI in the transmit stream, when the ring control ports are disabled, or in the insertion of a logic one in the SENDLRDI bit position in the receive ring control port, when the ring control ports are enabled.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

RTIULRDI

The RTIULRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port of the indexed channel upon the declaration of section trace identifier (mode 1 or 2) unstable. When RTIULRDI is a logic one, the detection of section trace identifier (mode 1) unstable results in the insertion of line RDI in the transmit stream, when the ring control ports are disabled, or in the insertion of a logic one in the SENDLRDI bit position in the receive ring control port, when the ring control ports are enabled.

RTIMLRDI

The RTIMLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port of the indexed channel upon the declaration of section trace identifier (mode 1) mismatch. When RTIMLRDI is a logic one, the detection of section trace identifier (mode 1) mismatch results in the insertion of line RDI in the transmit stream of the indexed channel, when the ring control ports are disabled, or in the insertion of a logic one in the SENDLRDI bit position in the receive ring control port, when the ring control ports are enabled.

LOSLRDI

The LOSLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port of the indexed channel upon the declaration of LOS. When LOSLRDI is a logic one, the detection of LOS results in the insertion of line RDI in the transmit stream, when the ring control ports are disabled, or in the insertion of a logic one in the SENDLRDI bit position in the receive ring control port, when the ring control ports are enabled.

LOFLRDI

The LOFLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port of the indexed channel upon the declaration of LOF. When LOFLRDI is a logic one, the detection of LOF results in the insertion of line RDI in the transmit stream, when the ring control ports are disabled, or in the insertion of a logic one in the SENDLRDI bit position in the receive ring control port, when the ring control ports are enabled.

SFLRDI

The SFLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port of the indexed channel upon the declaration of signal failure. When SFLRDI is a logic one, the detection of SF results in the insertion of line RDI in the transmit stream, when the ring control ports are disabled, or in the insertion of a logic one in the SENDLRDI bit position in the receive ring control port, when the ring control ports are enabled.

SDLRDI

The SDLRDI bit enables the insertion of line RDI in the transmit stream or the receive ring control port of the indexed channel upon the declaration of signal degrade. When SDLRDI is a logic one, the detection of SD results in the insertion of line RDI in the transmit stream, when the ring control ports are disabled, or in the insertion of a logic one in the SENDLRDI bit position in the receive ring control port, when the ring control ports are enabled.

Register 0106H, 0206H, 0306H, and 0406H: Section Alarm Output Control #1

Bit	Type	Function	Default
Bit 7	R/W	SDSALM	0
Bit 6	R/W	SFSALM	0
Bit 5	R/W	LOFSALM	0
Bit 4	R/W	LOSSALM	0
Bit 3	R/W	RTIMSALM	0
Bit 2	R/W	RTIUSALM	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAISSALM	0

This register and the Section Alarm Output Control #2 register control the alarms enabled to "set high" the SALM pin of the device

LAISSALM

The LAISSALM bit allows the AIS (LAIS) of the indexed channel to be ORed into the SALMm output. When the LAISSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications of the indexed channel and output on SALMm. When the LAISSALM bit is set low, the corresponding alarm indication does not affect the SALMm output.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

RTIUSALM

The RTIUSALM bit allows the section trace identifier (mode 1 or 2) unstable (RTIU) alarm indication of the indexed channel to be ORed into the SALMm output. When the RTIUSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications of the indexed channel and output on SALMm. When the RTIUSALM bit is set low, the corresponding alarm indication does not affect the SALMm output.

RTIMSALM

The RTIMSALM bit allows the section trace identifier (mode 1) mismatch (RTIM) alarm indication of the indexed channel to be ORed into the SALMm output. When the RTIMSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications of the indexed channel and output on SALMm. When the RTIMSALM bit is set low, the corresponding alarm indication does not affect the SALMm output.

LOSSALM

The LOSSALM bit allows the LOS alarm indication of the indexed channel to be ORed into the SALMm output. When the LOSSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications of the indexed channel and output on SALMm. When the LOSSALM bit is set low, the corresponding alarm indication does not affect the SALMm output.

LOFSALM

The LOFSALM bit allows the LOF alarm indication of the indexed channel to be ORed into the SALMm output. When the LOFSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications of the indexed channel and output on SALMm. When the LOFSALM bit is set low, the corresponding alarm indication does not affect the SALMm output.

SFSALM

The SFSALM bit allows the signal fail (SF) alarm indication of the indexed channel to be ORed into the SALMm output. When the SFSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications of the indexed channel and output on SALMm. When the SFSALM bit is set low, the corresponding alarm indication does not affect the SALMm output.

SDSALM

The SDSALM bit allows the signal degrade (SD) alarm indication of the indexed channel to be ORed into the SALMm output. When the SDSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications of the indexed channel and output on SALMm. When the SDSALM bit is set low, the corresponding alarm indication does not affect the SALMm output.

Register 0107H, 0207H, 0307H, and 0407H: Section Alarm Output Control #2

Bit	Type	Function	Default
Bit 7	R/W	LRDISALM	0
Bit 6	R/W	OOFSALM	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register and the Section Alarm Output Control #1 register control the alarms enabled to "set high" the SALM pin of the device

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

OOFSALM

The OOFSALM bit allows the OOF alarm indication of the indexed channel to be ORed into the SALMm output. When the OOFSALM bit is set high, the corresponding alarm indication is ORed with other alarm indications of the indexed channel and output on SALMm. When the OOFSALM bit is set low, the corresponding alarm indication does not affect the SALMm output.

LRDISALM

The LRDISALM bit allows the LRDI of the indexed channel to be ORed into the SALMm output. When the LRDISALM bit is set high, the corresponding alarm indication is ORed with other alarm indications of the indexed channel and output on SALMm. When the LRDISALM bit is set low, the corresponding alarm indication does not affect the SALMm output.

Register 0108H, 0208H, 0308H, and 0408H: Section/Line Block Interrupt Status

Bit	Type	Function	Default
Bit 7	—	Reserved	X
Bit 6	—	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	CRSII	X
Bit 3	R	RASEI	X
Bit 2	R	RSOPI	X
Bit 1	R	SSTBI	X
Bit 0	R	RLOPI	X

This register allows the source of an active interrupt from a section or line processing block of the indexed channel to be identified. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source.

RLOPI

The RLOPI bit is set high when one or more of the maskable interrupt sources in the receive line overhead processor of the indexed channel have been activated. This register bit remains high until the interrupt is acknowledged by reading the RLOP Interrupt Enable and Status Register of the indexed channel.

SSTBI

The SSTBI bit is set high when one or more of the maskable interrupt sources in the section trace buffer of the indexed channel have been activated. This register bit remains high until the interrupt is acknowledged by reading the SSTB Section Trace Status Register of the indexed channel.

RSOPI

The RSOPI bit is set high when one or more of the maskable interrupt sources in the receive section overhead processor of the indexed channel have been activated. This register bit remains high until the interrupt is acknowledged by reading the RSOP Interrupt Status Register of the indexed channel.

RASEI

The RASEI bit is set high when one or more of the maskable interrupt sources in the receive APS and synchronization extractor of the indexed channel have been activated. This register bit remains high until the interrupt is acknowledged by reading the RASE Interrupt Status Register of the indexed channel.

CRSII

The CRSII bit is set high when one or more of the maskable interrupt sources in the CRSI's of the indexed channel have been activated. This register bit remains high until the interrupt is acknowledged by reading the CRSI Interrupt Status Register of the indexed channel.

Register 0109H, 0209H, 0309H, and 0409H: Auxiliary Section/Line Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	RDOOLE	0
Bit 4	R/W	OOFE	0
Bit 3	R/W	LRDIE	0
Bit 2	R/W	LAISE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	LOSE	0

The Auxiliary Section/Line Interrupt Enable register is used to enable the generation of an external interrupt on the INTB pin of the device. When an associated auxiliary interrupt bit is set high and the enable is set high, an external interrupt will be generated on the INTB pin. Note: These interrupt enable bits do not affect the actual interrupt bits found in the Auxiliary Section/Line Interrupt Status register.

LOSE

The LOS interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the Auxiliary Section/Line Interrupt Status register of the indexed channel.

LOFE

The LOF interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the Auxiliary Section/Line Interrupt Status register of the indexed channel.

LAISE

The LAIS interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the Auxiliary Section/Line Interrupt Status register of the indexed channel.

LRDIE

The LRDI interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the Auxiliary Section/Line Interrupt Status register of the indexed channel.

OOFE

The OOF interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the Auxiliary Section/Line Interrupt Status register of the indexed channel.

RDOOLE

The receive data out of lock (RDOOL) interrupt enable bit controls interrupt generation on output INTB by the corresponding interrupt status bit in the Auxiliary Section/Line Interrupt Status register of the indexed channel.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

Register 010AH, 020AH, 030AH, and 040AH: Auxiliary Section/Line Interrupt Status

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	RDOOLI	X
Bit 4	R	OOFI	X
Bit 3	R	LRDII	X
Bit 2	R	LAISI	X
Bit 1	R	LOFI	X
Bit 0	R	LOSI	X

The Auxiliary Section/Line Interrupt Status register replicates section and line interrupts that can be found in the CRU, RSOP and RLOP registers of the indexed channel. However, unlike the above interrupt register bits that clear-on-reads, the Auxiliary Section/Line Interrupt Status register bits do not clear when read. To clear these register bits, logic one must be written to the register bit.

LOSI

The LOSI bit is set high when LOS is declared or removed.

LOFI

The LOFI bit is set high when LOF is declared or removed.

LAISI

The LAISI bit is set high when line LAIS is declared or removed.

LRDII

The LRDII bit is set high when line RDI is declared or removed.

OOFI

The OOFI bit is set high when OOF is declared or removed.

RDOOLI

The RDOOLI bit is the receive data out of lock interrupt status bit. RDOOLI is set high when the RDOOLV bit of the CRSI Clock Recovery Control, Status and Interrupt register changes state. RDOOLV is a logic one if the divided down recovered clock frequency is not within approximately 488 ppm of the REFCLK frequency or if no transitions have occurred on the RXDm+/- inputs for more than 80 bit periods.

Register 010BH, 020BH, 030BH, and 040BH: Auxiliary Signal Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	SDE	0
Bit 0	R/W	SFE	0

The Auxiliary Signal Interrupt Enable register is used to enable the generation of an external interrupt on the INTB pin of the device. When an associated auxiliary interrupt bit is set high and the enable is set high, an external interrupt will be generated on the INTB pin. Note that these interrupt enable bits do not affect the actual interrupt bits found in the Auxiliary Signal Interrupt Status register.

SFE

The signal fail (SF) interrupt enable bit controls interrupt generation on output INTB by the corresponding SFI in the Auxiliary Signal Status/Interrupt register of the indexed channel.

SDE

The signal degrade (SD) interrupt enable bit controls interrupt generation on output INTB by the corresponding SDI bit in the Auxiliary Signal Status/Interrupt register of the indexed channel.

Note: These enable bits do not affect the actual interrupt bits.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

Register 010CH, 020CH, 030CH, and 040CH: Auxiliary Signal Status/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	X
Bit 6	R/W	Reserved	X
Bit5	R/W	Reserved	X
Bit 4	R/W	Reserved	X
Bit 3	R/W	Reserved	X
Bit 2	R/W	Reserved	X
Bit 1	R/W	SDI	X
Bit 0	R/W	SFI	X

This register replicates the receive signal status and interrupts that can be found in the registers of the RASE block of the indexed channel. However, unlike the RASE interrupt register bits that clear-on-read, the interrupt bits in this register do not clear when read. To clear these register bits, a logic one must be written to the register bit.

SFI

The signal fail interrupt (SFI) status bit indicate when the signal fail threshold has been crossed as controlled using RASE registers of the indexed channel. This register bit is the same as the SFBERI bit found in the RASE Interrupt Status register of the indexed channel with the exception that it does not clear when read. To clear the register bit, a logic one must be written to it.

SDI

The signal degrade interrupt (SDI) status bit indicate when the signal degrade threshold has been crossed as controlled using RASE registers of the indexed channel. This register bit is the same as the SDBERI bit found in the RASE Interrupt Status register of the indexed channel with the exception that it does not clear when read. To clear the register bit, a logic one must be written to it.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

Registers 0110H, 0210H, 0310H, and 0410H: CRSI Configuration and Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	RROOLI	X
Bit5	R	RDOOLI	X
Bit 4	R	RROOLV	X
Bit 3	R	RDOOLV	X
Bit 2	R/W	RROOLE	0
Bit 1	R/W	RDOOLE	0
Bit 0	R/W	Reserved	0

This register controls the clock recovery and reports the state of the receive PLL of the indexed channel.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

RDOOLE

The RDOOLE bit is an interrupt enable for the receive data out of lock status. When RDOOLE is set to logic one, an interrupt is generated when the RDOOLV bit changes state.

RROOLE

The RROOLE bit is an interrupt enable for the reference out of lock status. When RROOLE is set to logic one, an interrupt is generated when the RROOLV bit changes state.

RDOOLV

The receive data out of lock status indicates the clock recovery PLL is unable to lock to the incoming data stream of the indexed channel. RDOOLV is a logic one if the divided down recovered clock frequency is not within 488 ppm of the REFCLK frequency or if no transitions have occurred on the RXDm+/- inputs for more than 80 bit periods. This bit will only be set to one just prior to affirming the out of locked state. The RDOOLI interrupt bit should be used for a gross declaration of the clock's validity.

RROOLV

The receive reference out of lock status indicates the clock recovery PLL is unable to lock to the receive reference (REFCLK). RROOLV should be polled after a power up reset to determine when the CRU PLL is operational. When RROOLV is a logic one, the CRU of the indexed channel is unable to lock to the receive reference. When RROOLV is a logic zero, the CRU is locked to the receive reference. The RROOLV bit may remain set at logic one for several hundred milliseconds after the removal of the power on reset as the CRU PLL locks to the receive reference clock.

RDOOLI

The RDOOLI bit is the receive data out of lock interrupt status bit. RDOOLI is set high when the RDOOLV bit of this register changes state. RDOOLI is cleared when this register is read.

RROOLI

The RROOLI bit is the receive reference out of lock interrupt status bit. RROOLI is set high when the RROOLV bit of this register changes state. RROOLI is cleared when this register is read.

Registers 0111H, 0211H, 0311H, and 0411H: CRSI Reserved

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	\R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The reserved bits must be programmed to logic zero for proper operation.

Registers 0114H, 0214H, 0314H, and 0414H: RSOP Control and Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	BLKBIP	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE

The OOFE bit is an interrupt enable for the OOF alarm of the indexed channel. When OOFE is a logic one, a section interrupt is generated when the OOF alarm is declared or removed.

LOFE

The LOFE bit is an interrupt enable for the LOF alarm of the indexed channel. When LOFE is a logic one, a section interrupt is generated when the LOF alarm is declared or removed.

LOSE

The LOSE bit is an interrupt enable for the LOS alarm of the indexed channel. When LOSE is a logic one, a section interrupt is generated when the LOS alarm is declared or removed.

BIPEE

The BIPEE bit is an interrupt enable for the section BIP-8 (B1) errors of the indexed channel. When BIPEE is a logic one, a section interrupt is generated when a section BIP-8 error is detected.

ALGO2

The ALGO2 bit selects the framing algorithm used to confirm and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first four bits of the last A2 framing byte (12 bits total) are examined. This algorithm examines only 12 bits of the framing pattern; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is enabled to use the first of the framing algorithms where all the A1 framing bytes and all the A2 framing bytes are examined.

FOOF

The FOOF bit is used to force the RSOP of the indexed channel OOF. When a logic one is written to the FOOF bit location, the RSOP is forced OOF at the next frame boundary, for only one frame. The OOF event results in the assertion of the OOFV register bit. The FOOF bit is defined as write only and the reading of this bit is undefined.

DDS

The DDS bit is used to disable the descrambling of the received stream of the indexed channel. When a logic one is written to the DDS bit position, the descrambler is disabled. When a logic zero is written to the DDS bit position, the descrambler is enabled.

BLKBIP

The BLKBIP bit enables the accumulating of section block BIP errors of the indexed channel. When set to logic one, one or more errors in the section BIP-8 byte (B1) results in a single error accumulated in the B1 error counter. When a logic zero is written to the BLKBIP bit position, all errors in the B1 byte are accumulated in the B1 error counter.

Registers 0115H, 0215H, 0315H, and 0415H: RSOP Status and Interrupt

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV

The OOFV bit is set high when OOF is declared. OOFV is set high and out-of frame declared while the SPECTRA 4x155 is unable to find a valid framing pattern (A1, A2) in the incoming stream of the indexed channel. OOF is removed when a valid framing pattern is detected. This alarm indication is also available on SPECTRA 4x155 OOF and RALM outputs.

LOFV

The LOFV bit is set high when LOF is declared. LOFV is set high and LOF declared when an OOF state persists for 3 ms on the indexed channel. LOF is removed when an in frame state persists for 3 ms. This alarm indication may also be available on the SPECTRA 4x155 RALMm output.

LOSV

The LOSV bit is set high when LOS is declared. LOSV is set high and LOS declared when 20 ± 2.5 µs of consecutive all zeros patterns is detected in the incoming stream of the indexed channel. LOS is removed when two valid framing words (A1, A2) are detected, and during the intervening time (125 µs), no violating period of all-zeros patterns is observed. This alarm indication may also be available on the SPECTRA 4x155 RALMm output.

OOFI

The OOFI bit is set high when OOF is declared or removed on the indexed channel. This bit is cleared when this register is read. A clear-on-write version of this register bit may be found in the Auxiliary Section/Line Interrupt Status Register.

LOFI

The LOFI bit is set high when LOF is declared or removed on the indexed channel. This bit is cleared when this register is read. A clear-on-write version of this register bit may be found in the Auxiliary Section/Line Interrupt Status Register.

LOSI

The LOSI bit is set high when LOS is declared or removed on the indexed channel. This bit is cleared when this register is read. A clear-on-write version of this register bit may be found in the Auxiliary Section/Line Interrupt Status Register.

BIPEI

The BIPEI bit is set high when a section BIP error is detected on the indexed channel. This bit is cleared when the RSOP Interrupt Status Register is read.

Registers 0116H, 0216H, 0316H, 0416H: RSOP Section BIP (B1) Error Count #1

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0117H, 0217H, 0317H, 0417H: RSOP Section BIP (B1) Error Count #2

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]

Bits SBE[15] through SBE[0] represent the number of section BIP-8 parity (B1) errors (individual or block) that have been detected on the indexed channel since the last accumulation interval. The error counters are polled by writing to either of the RSOP Section BIP Error count registers or by writing to the SPECTRA 4x155 Reset, Identity and Accumulation Trigger register. Such a write transfers the internally accumulated error count to the registers within 7 µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7 µs period has elapsed, the RSOP B1 Error Count Registers may be read.

Register 0118H, 0218H, 0318H, and 0418H: RLOP Control and Status

Bit	Type	Function	Default
Bit 7	R/W	BLKBIP	0
Bit 6	R/W	ALLONES	0
Bit 5	R/W	LAISDET	0
Bit 4	R/W	LRDIDET	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	BLKREI	0
Bit 1	R	LAISV	X
Bit 0	R	LRDIV	X

LRDIV

The LRDIV bit is set high when RDI (RDI) is detected on the indexed channel. Line RDI is detected when a 110 binary pattern is detected in bits 6, 7, and 8, of the K2 byte for three or five consecutive frames (as selected by the LRDIDET bit in this register). Line RDI is removed when any pattern other than 110 is detected for three or five consecutive frames. This alarm indication is also available on the SPECTRA 4x155 LRDI/RRCPCLK and RALM outputs.

LAISV

The LAISV bit is set high when AIS (AIS) is detected on the indexed channel. Line AIS is detected when a 111 binary pattern is detected in bits 6, 7, and 8, of the K2 byte for three or five consecutive frames (as selected by the LAISDET bit in this register). Line AIS is removed when any pattern other than 111 is detected for three or five consecutive frames. This alarm indication is also available on the SPECTRA 4x155 LAIS/RRCPDAT and RALM outputs.

BLKREI

The BLKREI (Block REI) bit controls the accumulation of REI's on the indexed channel. When BLKREI is logic one the REI event counter is incremented only once per frame whenever one or more REI bits occur during the frame. When BLKREI is logic zero, the REI event counter is incremented for each and every REI bit that occurs during that frame. The counter may be incremented up to 24 times.. The REI counter is not incremented for invalid REI code words.

BLKBIPO

The BLKBIPO (Block BIP Out) bit controls the indication of line BIP (B2) errors reported to the TLOP and receive ring control port blocks of the indexed channel for insertion as REI. When BLKBIPO is logic one, one BIP error is indicated per frame whenever one or more B2 bit errors occur during that frame. When BLKBIPO is logic zero, a BIP error is indicated for every B2 bit error that occurs during that frame. The accumulation of B2 error events functions independently and is controlled by the BLKBIP register bit.

LRDIDET

The LRDIDET bit determines the line RDI alarm detection algorithm of the indexed channel. When LRDIDET is set to logic one, line RDI is declared when a 110 binary pattern is detected in bits 6,7 and, 8 of the K2 byte for three consecutive frames and is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When LRDIDET is set to logic zero, line RDI is declared when a 110 binary pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames and is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

LAISDET

The LAISDET bit determines the line AIS alarm detection algorithm of the indexed channel. When LAISDET is set to logic one, line AIS is declared when a 111 binary pattern is detected in bits 6,7 and, 8 of the K2 byte for three consecutive frames and is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three consecutive frames. When LAISDET is set to logic zero, line AIS is declared when a 111 binary pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames and is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for five consecutive frames.

ALLONES

The ALLONES bit controls automatically overwriting the SONET/SDH frame with all-ones whenever line AIS is detected on the indexed channel. When ALLONES is set to logic one, the SONET/SDH frame is forced to logic one immediately when the line AIS alarm is declared. When line AIS is removed, the SONET/SDH frame is immediately returned to carrying the receive stream. When ALLONES is set to logic zero, the outputs carry the receive stream regardless of the state of the line AIS alarm.

BLKBIP

The BLKBIP (Block BIP) bit controls the accumulation of B2 errors on the indexed channel. When BLKBIP is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When BLKBIP is logic zero, the B2 error event counter is incremented for each B2 bit error that occurs during that frame (the counter can be incremented up to 96 times per frame).

Registers 0119H, 0219H, 0319H, and 0419H: RLOP Interrupt Enable and Status

Bit	Type	Function	Default
Bit 7	R/W	LREIE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	LRDIE	0
Bit 3	R	LREII	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	LRDII	X

LRDII

The LRDII bit is the RDI interrupt status bit. LRDII is set high when line RDI is declared or removed on the indexed channel. This bit is cleared when this register is read. A clear-on-write version of this register bit may be found in the Auxiliary Section/Line Interrupt Status Registers.

LAISI

The LAISI bit is the alarm indication signal interrupt status bit. LAISI is set high when line LAIS is declared or removed on the indexed channel. This bit is cleared when this register is read. A clear-on-write version of this register bit may be found in the Auxiliary Section/Line Interrupt Status Registers.

BIPEI

The BIPEI bit is the line BIP-24 interrupt status bit. BIPEI is set high when a line BIP error is detected on the indexed channel. This bit is cleared when this register is read.

LREII

The LREII bit is the remote error indication status bit. LREII is set high when a line REI error is detected on the indexed channel. This bit is cleared when this register is read.

LRDIE

The LRDIE bit is an interrupt enable for the RDI alarm. When LRDIE is a logic one, a line interrupt is generated when line RDI is declared or removed on the indexed channel.

LAISE

The LAIS bit is an interrupt enable for the AIS. When LAISE is a logic one, a line interrupt is generated when line AIS is declared or removed on the indexed channel.

BIPEE

The BIPEE bit is an interrupt enable for the line BIP-24 errors. When BIPEE is a logic one, a line interrupt is generated when a line BIP-24 error (B2) is detected on the indexed channel.

LREIE

The LREIE is an interrupt enable for the line remote error indications. When LREIE is a logic one, a line interrupt is generated when a line REI indication is detected on the indexed channel.

Registers 011AH, 021AH, 031AH, 041AH: RLOP Line BIP (B2) Error Count #1

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Registers 011BH, 021BH, 031BH, 041BH: RLOP Line BIP (B2) Error Count #2

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Registers 011CH, 021CH, 031CH, 041CH: RLOP Line BIP (B2) Error Count #3

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]

Bits LBE[19:0] represent the number of line BIP errors (individual or block) that have been detected on the indexed channel since the last accumulation interval. The error counters are polled by writing to any of the RLOP B2 Error Count or the RLOP REI Error Count registers along with writing to the SPECTRA 4x155 Reset, Identify and Accumulation Trigger Register. Such write accesses transfer the internally accumulated error count to these registers within 7 µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7 µs period has elapsed, the RLOP B2 Error Count Registers may be read.

Registers 011DH, 021DH, 031DH, and 041DH: RLOP REI Error Count #1

Bit	Type	Function	Default
Bit 7	R	LREI[7]	X
Bit 6	R	LREI[6]	X
Bit 5	R	LREI[5]	X
Bit 4	R	LREI[4]	X
Bit 3	R	LREI[3]	X
Bit 2	R	LREI[2]	X
Bit 1	R	LREI[1]	X
Bit 0	R	LREI[0]	X

Registers 011EH, 021EH, 031EH, and 041EH: RLOP REI Error Count #2

Bit	Type	Function	Default
Bit 7	R	LREI[15]	X
Bit 6	R	LREI[14]	X
Bit 5	R	LREI[13]	X
Bit 4	R	LREI[12]	X
Bit 3	R	LREI[11]	X
Bit 2	R	LREI[10]	X
Bit 1	R	LREI[9]	X
Bit 0	R	LREI[8]	X

Registers 011FH, 021FH, 031FH, and 041FH: RLOP REI Error Count #3

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R	LREI[19]	X
Bit 2	R	LREI[18]	X
Bit 1	R	LREI[17]	X
Bit 0	R	LREI[16]	X

LREI[19:0]

Bits LREI[19:0] represent the number of line REIs (individual or block) that have been detected on the indexed channel since the last accumulation interval. The error counters are polled by writing to any of the RLOP B2 Error Count or the RLOP REI Error Count registers along with writing to the SPECTRA 4x155 Reset, Identify and Accumulation Trigger Register. Such a write transfers the internally accumulated error count to the registers within 7 µs and simultaneously resets the internal counters to begin a new cycle of error accumulation. After the 7 µs period has elapsed, the RLOP REI Error Count Registers may be read.

Registers 0120H, 0220H, 0320H, and 0420H: SSTB Section Trace Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	TIMODE	0
Bit 5	R/W	RTIUE	0
Bit 4	R/W	RTIME	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

LEN16

The section trace message length bit (LEN16) selects the length of the section trace message to be 16 bytes or 64 bytes for the indexed channel. When LEN16 is set high, the section trace message length is 16 bytes. When LEN16 is set low, the section trace message length is 64 bytes.

NOSYNC

The section trace message synchronization disable bit (NOSYNC) disables the writing of the section trace message into the trace buffer synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive section trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the section trace message buffer behaves as a circular buffer.

TNULL

The transmit null bit (TNULL) controls the insertion of an all-zero section trace identifier message in the transmit stream of the indexed channel. When TNULL is set high, the contents of the transmit buffer are ignored and all-zeros bytes are optionally inserted into the J0 byte. When TNULL is set low the contents of the transmit section trace buffer is optionally inserted into the J0 byte. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5

The receive trace identifier persistence bit (PER5) controls the number of times a section trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively on the indexed channel. When PER5 is set low, the message is accepted after three identical repetitions.

RTIME

The receive section trace identifier (mode 1) mismatch interrupt enable bit (RTIME) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa on the indexed channel. When RTIME is set high, changes in match state activates the interrupt (INTB) output. When RTIME is set low, section trace identifier (mode 1) state changes will not affect INTB. This bit is should be disabled in Trace identifier Mode 2 since the RTIM is generate using the Mode 1 algorithm.

RTIUE

The receive section trace identifier (mode 1) unstable interrupt enable bit (RTIUE) controls the activation of the interrupt output when the receive identifier message state (RTIUV) changes from stable to unstable and vice versa on the indexed channel. State changes dependent on the Trace Identifier Mode When RTIUE is set high, changes in the receive section trace identifier unstable (RTIUV) state will activate the interrupt (INTB) output. When RTIUE is set low, section trace identifier unstable state changes will not affect INTB.

TIMODE

The Trace Identifier Mode is used to set the mode for the received section trace identifier of the indexed channel. Setting this bit to low sets the Trace Identifier Mode to Mode 1. In this mode the section trace identifier is defined as a regular 16 or 64-byte trace message and persistency is based on the whole message. Receive trace identifier mismatch (RTIM) and unstable (RTIU) alarms are declared on the trace message. Setting this bit to high sets the Trace Identifier Mode to Mode2. In this mode the section trace identifier is defined as a 16-byte message with a single repeating byte that is monitored for persistency and errors. A receive trace identifier unstable (RTIU) alarm is declared when one or more byte errors are detected in three consecutive 16-byte windows. RTIM is not defined in this mode.

ZEROEN

The zero enable bit (ZEROEN) is defined for Trace Identifier Mode 1 only and enables trace identifier mismatch (RTIM) assertion and removal on the indexed channel based on an all-zeros section trace message string. When ZEROEN is set high, all-zeros section trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all-zeros section trace message strings are ignored. Trace identifier unstable (RTIU) assertion and removal is not affected by setting this register bit.

Registers 0121H, 0221H, 0321H, and 0421H: SSTB Section Trace Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the section trace identifier status.

RTIMV

The receive section trace identifier mismatch status bit (RTIMV) is set high in Trace Identifier Mode 1 when the accepted message differs from the expected message on the indexed channel. The accepted message is the last message to have been received five times consecutively. RTIMV is set low when the accepted message is equal to the expected message. If the accepted section trace message string is all-ZEROs, the mismatch is not declared unless the ZEROEN register bit in the Control register is set. This bit is usually ignored in Trace Identifier Mode 2.

RTIMI

The receive trace identifier mismatch indication status bit (RTIMI) is set high in Trace Identifier Mode 1 when the match/mismatch status (RTIMV) of the trace identifier framer changes state on the indexed channel. This bit (and the interrupt) is cleared when this register is read. This bit is usually ignored in Trace Identifier Mode 2.

RTIUV

The receive section trace identifier unstable status bit (RTIUV) is dependent on the Trace Identifier Mode. In Mode 1, the bit is set high when eight trace messages mismatching against their immediate predecessor message have been received without a persistent message being detected on the indexed channel. The unstable counter is incremented on each message that mismatches its predecessor and is cleared on the reception of a persistent message (three or five consecutive matching messages). RTIUV is set high when the unstable counter reaches eight. RTIUV is set low and the unstable counter cleared once a persistent message has been received.

In Mode 2, RTIUV is set low during the stable state that is declared after having received the same 16-byte trace message three consecutive times on the indexed channel (stable trace byte for forty-eight consecutive frames). The stable byte is declared the accepted byte. RTIUV is set high when mismatches between the accepted byte and the received byte have been detected in three consecutive 16-byte windows. The 16-byte windows do not overlap and start immediately upon the first detected error.

RTIUI

The receive section trace identifier unstable interrupt status bit is set high when the path trace identifier unstable status (RTIUV) changes state on the indexed channel. The setting of this bit is dependent on the unstable status (RTIUV), which is dependent on the Trace Identifier Mode. This bit and the interrupt are cleared when this register is read.

Reserved

The Reserved read bits must be ignored when read in the SPECTRA 4x155.

Registers 0122H, 0222H, 0322H, and 0422H: SSTB Section Trace Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	A[7]	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into section trace identifier buffers. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. If RWB is set high, a read access is initiated. The data read can be found in the SSTB Indirect Data register. If RWB is set low, a write access is initiated. The data in the SSTB Indirect Data register will be written to the address specified.

A[7:0]

The indirect read address bits (A[7:0]) indexes into the path trace identifier buffers. Addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted into the J0 byte of the transmit stream. Addresses 64 to 127 reference the receive accepted message page. A receive message is accepted into this page when it is received unchanged three or five times consecutively as determined by the PER5 bit setting. Addresses 128 to 191 reference the receive capture page while addresses 192 to 255 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor.

A[7:0]	RAM Contents
0-63d	Transmit Trace Message
64-127d	Receive Accepted Trace Message
128-191d	Receive Captured Trace Message
192-255d	Receive Expected Trace Message

Registers 0123H, 0223H, 0323H, and 0423H: SSTB Section Trace Indirect Data

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the section trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Registers 0124H, 0224H, 0324H, and 0424H: SSTB Reserved

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

Registers 0125H, 0225H, 0325H, and 0425H: SSTB Reserved

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155. The Reserved read bits must be ignored when reading the SPECTRA-4x-155.

Registers 0126H, 0226H, 0326H, and 0426H: SSTB Section Trace Operation

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6	R/W	RWB	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

RWB

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer of the indexed channel. The access will be performed when the SSTB Indirect Address register is written to. If RWB is set high, a read access is initiated. The data read can be found in the SSTB Indirect Data register. If RWB is set low, a write access is initiated. The data in the SSTB Indirect Data register will be written to the address specified.

BUSY

The BUSY bit reports whether a previously initiated indirect read or write to the section trace RAM of the indexed channel has been completed. BUSY is set high upon writing to the SSTB Path Trace Indirect Address register, and stays high until the initiated access has completed. At this point, BUSY is set low. This register should be polled to determine when new data is available in the SSTB Indirect Data register. The maximum latency for the BUSY to return low is 10 µs.

Registers 0130H, 0230H, 0330H, and 0430H: RTOC Overhead Control

Bit	Type	Function	Default
Bit 7	R/W	Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	1
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	1
Bit 1	R/W	RSLD_TS	1
Bit 0	R/W	RSLDSEL	0

The RTOC Control Register is used to control the receive section and line overhead outputs of the SPECTRA 4x155.

RSLDSEL

The receive data line select (RSLDSEL) bit determines the contents of the outgoing RSLDm stream. When RSLDSEL is low, the RSLDm stream contains the section DCC (D1-D3) of the indexed channel. When RSLDSEL is high, the RSLD stream contains the line DCC (D4-D12).

RSLD_TS

The register bit can be used to control the tri-stating of the RSLDm and RSLDCLKm outputs. Setting RSLD_TS to logic one tri-states the outputs. Setting this bit to logic zero allows normal functioning. RSLD_TS defaults to logic one so that RSLDm and RSLDCLKm would be tri-stated after reset.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

Registers 0131H, 0231H, 0331H, and 0431H: RTOC AIS Control

Bit	Type	Function	Default
Bit 7	R/W	Unused	X
Bit 6	R/W	Unused	X
Bit 5	R/W	LINE_AISEN(2)	0
Bit 4	R/W	LINE_AISEN(1)	0
Bit 3	R/W	LINE_AISEN(0)	0
Bit 2	R/W	SECT_AISEN(2)	0
Bit 1	R/W	SECT_AISEN(1)	0
Bit 0	R/W	SECT_AISEN(0)	0

The RTOC AIS Control Register is provided to explicitly force the receive section and line overhead outputs of the indexed channel.

SECT_AISEN(2:0)

The SECT_AISEN(2:0) bits enable the explicit insertion of all-ones on RSLDm when carrying section DCC and the section overhead on RTOHm. Each bit enables a separate group of alarms to force the section overhead outputs to all-ones. Setting a bit to logic one enables a declared alarm in that bit's group to force the output section overhead to all-ones. Alarms in that group will not explicitly force the section overhead outputs to all-ones when the bit is set to logic low.

SECT_AIS_EN	Grouped Alarms
[0]	LOS & LOF
[1]	LAIS
[2]	RTIM

LINE_AISEN(2:0)

The LINE_AISEN(2:0) bits enable the explicit insertion of all-ones on RSLDm when carrying line overhead and the line overhead on RTOHm. Each bit enables a separate group of alarms to force the line overhead outputs to all-ones. Setting a bit to logic one enables a declared alarm in that bit's group to force the output line overhead to all-ones. Alarms in that group will not explicitly force the line overhead outputs to all-ones when the bit is set to logic low. Other SPECTRA 4x155 top level bits may control the insertion of LAIS on certain alarms and hence affect the line overhead outputs when all-ones insertion is disabled here.

LINE_AIS_EN	Grouped Alarms
[0]	LOS & LOF
[1]	LAIS
[2]	RTIM

Registers 0140H, 0240H, 0340H, 0440H: RASE Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	Z1/S1E	0
Bit 4	R/W	SFBERE	0
Bit 3	R/W	SDBERE	0
Bit 2	R/W	Unused	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

SDBERE

The SDBERE bit is the interrupt enable for the signal degrade threshold alarm. When SDBERE is a logic one, an interrupt is generated when the SD alarm is declared or removed on the indexed channel.

SFBERE

The SFBERE bit is the interrupt enable for the signal fail threshold alarm. When SFBERE is a logic one, an interrupt is generated when the SF alarm is declared or removed on the indexed channel.

Z1/S1E

The Z1/S1 interrupt enable is an interrupt mask for changes in the received synchronization status of the indexed channel. When Z1/S1E is a logic one, an interrupt is generated when a new synchronization status message is extracted into the Receive Z1/S1 register.

COAPSE

The COAPS interrupt enable is an interrupt mask for changes in the received APS code on the indexed channel. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value is extracted into the RASE Receive K1 and RASE Receive K2 registers.

PSBFE

The PSBF interrupt enable is an interrupt mask for protection switch byte failure alarms. When PSBFE is a logic one, an interrupt is generated when PSBF is declared or removed on the indexed channel.

Registers 0141H, 0241H, 0341H, 0441H: RASE Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSBFI	X
Bit 6	R	COAPSI	X
Bit 5	R	Z1/S1I	X
Bit 4	R	SFBERI	X
Bit 3	R	SDBERI	X
Bit 2	R	SFBERV	X
Bit 1	R	SDBERV	X
Bit 0	R	PSBFV	X

PSBFV

The PSBFV bit indicates the protection switching byte failure alarm state on the indexed channel. The alarm is declared (PSBFV is set high) when 12 successive frames, starting with the last frame containing a previously consistent byte, have been received without three consecutive frames containing identical K1 bytes. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received.

SDBERV

The SDBERV bit indicates the signal degrade threshold crossing alarm state on the indexed channel. The alarm is declared (SDBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SD Declaring Threshold registers. The alarm is removed (SDBERV is set low) when the bit error rate is below the threshold programmed in the RASE SD Clearing Threshold registers.

SFBERV

The SFBERV bit indicates the signal failure threshold crossing alarm state on the indexed channel. The alarm is declared (SFBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SF Declaring Threshold registers. The alarm is removed (SFBERV is set low) when the bit error rate is below the threshold programmed in the RASE SF Clearing Threshold registers.

SDBERI

The SDBERI bit is set high when the signal degrade threshold crossing alarm is declared or removed on the indexed channel. This bit is cleared when the RASE Interrupt Status register is read. A clear-on-write version of this register bit may be found in the SPECTRA 4x155 Auxiliary Section/Line Interrupt Status registers.

SFBERI

The SFBERI bit is set high when the signal failure threshold crossing alarm is declared or removed on the indexed channel. This bit is cleared when the RASE Interrupt Status register is read. A clear-on-write version of this register bit may be found in the SPECTRA 4x155 Auxiliary Section/Line Interrupt Status Registers.

Z1/S1I

The Z1/S1I bit is set high when a new synchronization status message has been extracted into the RASE Receive Z1/S1 register of the indexed channel. This bit is cleared when the RASE Interrupt Status register is read.

COAPSI

The COAPSI bit is set high when a new APS code value has been extracted into the RASE Receive K1 and RASE Receive K2 registers of the indexed channel. This bit is cleared when the RASE Interrupt Status register is read.

PSBFI

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed on the indexed channel. This bit is cleared when the RASE Interrupt Status register is read.

Registers 0142H, 0242H, 0342H, 0442H: RASE Configuration/Control

Bit	Type	Function	Default
Bit 7	R/W	Z1/S1_CAP	0
Bit 6	R/W	SFBERTEN	0
Bit 5	R/W	SFSMODE	0
Bit 4	R/W	SFCMODE	0
Bit 3	R/W	SDBERTEN	0
Bit 2	R/W	SDSMODE	0
Bit 1	R/W	SDCMODE	0
Bit 0	R/W	Unused	X

SDCMODE

The SDCMODE alarm bit selects the RASE window size to use for clearing the SD alarm. When SDCMODE is a logic zero the RASE clears the SD alarm using the same window size used for declaration. When SDCMODE is a logic one the RASE clears the SD alarm using a window size that is eight times longer than the alarm declaration window size. The declaration window size is determined by the RASE SD Accumulation Period registers.

SDSMODE

The SDSMODE bit selects the RASE saturation mode. When SDSMODE is a logic zero the RASE limits the number of B2 errors accumulated in one frame period to the RASE SD Saturation Threshold register value. When SDSMODE is a logic one the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SD Saturation Threshold register value. Note: The number of frames in a window subtotal accumulation period is determined by the RASE SD Accumulation Period register value.

SDBERTEN

The SDBERTEN bit selects automatic monitoring of line bit error rate threshold events by the RASE. When SDBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SDBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SDBERTEN is written.

SFCMODE

The SFCMODE alarm bit selects the RASE window size to use for clearing the SF alarm. When SFCMODE is a logic zero the RASE clears the SF alarm using the same window size used for declaration. When SFCMODE is a logic one the RASE clears the SF alarm using a window size that is eight times longer than the alarm declaration window size. The declaration window size is determined by the RASE SF Accumulation Period registers.

SFSMODE

The SFSMODE bit selects the RASE saturation mode. When SFSMODE is a logic zero the RASE limits the number of B2 errors accumulated in one frame period to the RASE SF Saturation Threshold register value. When SFSMODE is a logic one the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SF Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SF Accumulation Period register value.

SFBERTEN

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the RASE. When SFBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SFBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SFBERTEN is written.

Z1/S1_CAP

The Z1/S1_CAP bit enables the Z1/S1 Capture algorithm. When Z1/S1_CAP is a logic one, the Z1/S1 clock synchronization status message nibble must have the same value for eight consecutive frames before writing the new value into the RASE Receive Z1/S1 register. When Z1/S1_CAP is logic zero, the Z1/S1 nibble value is written directly into the RASE Receive Z1/S1 register.

Registers 0143H, 0243H, 0343H, and 0443H: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[7]	0
Bit 6	R/W	SFSAP[6]	0
Bit 5	R/W	SFSAP[5]	0
Bit 4	R/W	SFSAP[4]	0
Bit 3	R/W	SFSAP[3]	0
Bit 2	R/W	SFSAP[2]	0
Bit 1	R/W	SFSAP[1]	0
Bit 0	R/W	SFSAP[0]	0

Registers 0144H, 0244H, 0344H, and 0444H: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[15]	0
Bit 6	R/W	SFSAP[14]	0
Bit 5	R/W	SFSAP[13]	0
Bit 4	R/W	SFSAP[12]	0
Bit 3	R/W	SFSAP[11]	0
Bit 2	R/W	SFSAP[10]	0
Bit 1	R/W	SFSAP[9]	0
Bit 0	R/W	SFSAP[8]	0

Registers 0145H, 0245H, 0345H, and 0445H: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[23]	0
Bit 6	R/W	SFSAP[22]	0
Bit 5	R/W	SFSAP[21]	0
Bit 4	R/W	SFSAP[20]	0
Bit 3	R/W	SFSAP[19]	0
Bit 2	R/W	SFSAP[18]	0
Bit 1	R/W	SFSAP[17]	0
Bit 0	R/W	SFSAP[16]	0

SFSAP[23:0]

The SFSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SF alarm is broken into eight subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Registers 0146H, 0246H, 0346H, and 0446H: RASE SF Saturation Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFSTH[7]	0
Bit 6	R/W	SFSTH[6]	0
Bit 5	R/W	SFSTH[5]	0
Bit 4	R/W	SFSTH[4]	0
Bit 3	R/W	SFSTH[3]	0
Bit 2	R/W	SFSTH[2]	0
Bit 1	R/W	SFSTH[1]	0
Bit 0	R/W	SFSTH[0]	0

Registers 0147H, 0247H, 0347H, and 0447H: RASE SF Saturation Threshold

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SFSTH[11]	0
Bit 2	R/W	SFSTH[10]	0
Bit 1	R/W	SFSTH[9]	0
Bit 0	R/W	SFSTH[8]	0

SFSTH[11:0]

The SFSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SF threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Registers 0148H, 0248H, 0348H, and 0448H: RASE SF Declaring Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFDTH[7]	0
Bit 6	R/W	SFDTH[6]	0
Bit 5	R/W	SFDTH[5]	0
Bit 4	R/W	SFDTH[4]	0
Bit 3	R/W	SFDTH[3]	0
Bit 2	R/W	SFDTH[2]	0
Bit 1	R/W	SFDTH[1]	0
Bit 0	R/W	SFDTH[0]	0

Registers 0149H, 0249H, 0349H, and 0449H: RASE SF Declaring Threshold

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SFDTH[11]	0
Bit 2	R/W	SFDTH[10]	0
Bit 1	R/W	SFDTH[9]	0
Bit 0	R/W	SFDTH[8]	0

SFDTH[11:0]

The SFDTH[11:0] value determines the threshold for the declaration of the SF alarm. The SF alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SFDTH[11:0] value. Refer to the Operations section for the recommended settings.

Registers 014AH, 024AH, 034AH, and 044AH: RASE SF Clearing Threshold

Bit	Type	Function	Default
Bit 7	R/W	SFCTH[7]	0
Bit 6	R/W	SFCTH[6]	0
Bit 5	R/W	SFCTH[5]	0
Bit 4	R/W	SFCTH[4]	0
Bit 3	R/W	SFCTH[3]	0
Bit 2	R/W	SFCTH[2]	0
Bit 1	R/W	SFCTH[1]	0
Bit 0	R/W	SFCTH[0]	0

Registers 014BH, 024BH, 034BH, and 044BH: RASE SF Clearing Threshold

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SFCTH[11]	0
Bit 2	R/W	SFCTH[10]	0
Bit 1	R/W	SFCTH[9]	0
Bit 0	R/W	SFCTH[8]	0

SFCTH[11:0]

The SFCTH[11:0] value determines the threshold for the removal of the SF alarm. The SF alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SFCTH[11:0] value. Refer to the Operations section for the recommended settings.

Registers 014CH, 024CH, 034CH, and 044CH: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[7]	0
Bit 6	R/W	SDSAP[6]	0
Bit 5	R/W	SDSAP[5]	0
Bit 4	R/W	SDSAP[4]	0
Bit 3	R/W	SDSAP[3]	0
Bit 2	R/W	SDSAP[2]	0
Bit 1	R/W	SDSAP[1]	0
Bit 0	R/W	SDSAP[0]	0

Registers 014DH, 024DH, 034DH, and 044DH: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[15]	0
Bit 6	R/W	SDSAP[14]	0
Bit 5	R/W	SDSAP[13]	0
Bit 4	R/W	SDSAP[12]	0
Bit 3	R/W	SDSAP[11]	0
Bit 2	R/W	SDSAP[10]	0
Bit 1	R/W	SDSAP[9]	0
Bit 0	R/W	SDSAP[8]	0

Registers 014EH, 024EH, 034EH, and 044EH: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[23]	0
Bit 6	R/W	SDSAP[22]	0
Bit 5	R/W	SDSAP[21]	0
Bit 4	R/W	SDSAP[20]	0
Bit 3	R/W	SDSAP[19]	0
Bit 2	R/W	SDSAP[18]	0
Bit 1	R/W	SDSAP[17]	0
Bit 0	R/W	SDSAP[16]	0

SDSAP[23:0]

The SDSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SD alarm is broken into eight subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operations section for recommended settings.

Registers 014FH, 024FH, 034FH, and 044FH: RASE SD Saturation Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDSTH[7]	0
Bit 6	R/W	SDSTH[6]	0
Bit 5	R/W	SDSTH[5]	0
Bit 4	R/W	SDSTH[4]	0
Bit 3	R/W	SDSTH[3]	0
Bit 2	R/W	SDSTH[2]	0
Bit 1	R/W	SDSTH[1]	0
Bit 0	R/W	SDSTH[0]	0

Registers 0150H, 0250H, 0350H, and 0450H: RASE SD Saturation Threshold

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SDSTH[11]	0
Bit 2	R/W	SDSTH[10]	0
Bit 1	R/W	SDSTH[9]	0
Bit 0	R/W	SDSTH[8]	0

SDSTH[11:0]

The SDSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SD threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operations section for the recommended settings.

Registers 0151H, 0251H, 0351H, and 0451H: RASE SD Declaring Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDDTH[7]	0
Bit 6	R/W	SDDTH[6]	0
Bit 5	R/W	SDDTH[5]	0
Bit 4	R/W	SDDTH[4]	0
Bit 3	R/W	SDDTH[3]	0
Bit 2	R/W	SDDTH[2]	0
Bit 1	R/W	SDDTH[1]	0
Bit 0	R/W	SDDTH[0]	0

Registers 0152H, 0252H, 0352H, and 0452H: RASE SD Declaring Threshold

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SDDTH[11]	0
Bit 2	R/W	SDDTH[10]	0
Bit 1	R/W	SDDTH[9]	0
Bit 0	R/W	SDDTH[8]	0

SDDTH[11:0]

The SDDTH[11:0] value determines the threshold for the declaration of the SD alarm. The SD alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SDDTH[11:0] value. Refer to the Operations section for the recommended settings.

Registers 0153H, 0253H, 0353H, and 0453H: RASE SD Clearing Threshold

Bit	Type	Function	Default
Bit 7	R/W	SDCTH[7]	0
Bit 6	R/W	SDCTH[6]	0
Bit 5	R/W	SDCTH[5]	0
Bit 4	R/W	SDCTH[4]	0
Bit 3	R/W	SDCTH[3]	0
Bit 2	R/W	SDCTH[2]	0
Bit 1	R/W	SDCTH[1]	0
Bit 0	R/W	SDCTH[0]	0

Registers 0154H, 0254H, 0354H, and 0454H: RASE SD Clearing Threshold

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	SDCTH[11]	0
Bit 2	R/W	SDCTH[10]	0
Bit 1	R/W	SDCTH[9]	0
Bit 0	R/W	SDCTH[8]	0

SDCTH[11:0]

The SDCTH[11:0] value determines the threshold for the removal of the SD alarm. The SD alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SDCTH[11:0] value. Refer to the Operations section for the recommended settings.

Registers 0155H, 0255H, 0355H, 0455H: RASE Receive K1

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]

The K1[7:0] bits contain the current K1 code value. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Registers 0156H, 0256H, 0356H, 0456H: RASE Receive K2

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]

The K2[7:0] bits contain the current K2 code value. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Registers 0157H, 0257H, 0357H, 0457H: RASE Receive Z1/S1

Bit	Type	Function	Default
Bit 7	R	~~Z1/S1[7]~~Reserved	X
Bit 6	R	~~Z1/S1[6]~~Reserved	X
Bit 5	R	~~Z1/S1[5]~~Reserved	X
Bit 4	R	~~Z1/S1[4]~~Reserved	X
Bit 3	R	Z1/S1[3]	X
Bit 2	R	Z1/S1[2]	X
Bit 1	R	Z1/S1[1]	X
Bit 0	R	Z1/S1[0]	X

Z1/S1[3:0]

The lower nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. The Z1/S1 byte is used to carry synchronization status messages between line terminating network elements. Z1/S1[3] is the most significant bit corresponding to bit 5, the first bit received. Z1/S1[0] is the least significant bit, corresponding to bit 8, the last bit received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame (using the Z1/S1E bit in the RASE Interrupt Enable register).

Debouncing can be performed where the register is not loaded until eight of the same consecutive nibbles are received. Debouncing is controlled using the Z1/S1_CAP bit in the RASE Configuration/Control register.

~~Z1/S1[7:4]~~

~~The upper nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. No interrupt is asserted on the change of this nibble.~~

~~When the Z1/S1_CAP3 bit in the RASE Configuration/Control register selects debouncing, the upper nibble is only updated when three of the same consecutive lower nibbles are received.~~

Registers 0180H, 0280H, 0380H, and 0480H: TSOP Control

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	DC1	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS

The LAIS bit controls the insertion of AIS on the indexed channel. When LAIS is set high, the TSOP inserts line AIS into the transmit stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

DC1

The DC1 bit controls the overwriting of the identity bytes (J0/Z0) on the indexed channel. When DC1 is logic one, the values inserted by the TTOC during the J0/Z0 byte positions are passed through the transmit section overhead processor unaltered. Note: All three (STS-3/STM-1) identification bytes are passed through unaltered. When DC1 is logic zero, the identity bytes not inserted via the TTOC block are programmed as specified in the North American references: STS-1 (STM-0) #1 J0 = 01H, STS-1 (STM-0) #2 Z0 = 02H, and STS-1 (STM-0) #3 Z0 = 03H.

DS

The disable scrambling (DS) bit controls the scrambling of the transmit stream of the indexed channel. When a logic one is written to the DS bit position, the scrambler is disabled. When a logic zero is written to the DS bit position, the scrambler is enabled.

Registers 0181H, 0281H, 0381H, and 0481H: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DB1	0
Bit 0	R/W	DFP	0

DFP

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. If DFP is set high the A1 bytes are set to 76H instead of F6H.

DB1

The DB1 bit controls the insertion of bit errors continuously in the B1 section overhead byte. When DB1 is set high the B1 byte value is inverted.

DLOS

The DLOS bit controls the insertion of all-zeros in the transmit outgoing stream. When DLOS is set high the transmit stream is forced low.

Registers 0184H, 0284H, 0384H, and 0484H: TLOP Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LRDI	0

LRDI

The LRDI bit controls the insertion of transmit RDI (RDI) on the indexed channel. When LRDI is a logic one, line RDI is inserted into the transmit stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7, and 8 of the K2 byte. Line RDI may also be inserted using the TLRDI input, when the ring control ports are disabled, or using the transmit ring control port, when it is enabled. When LRDI is logic zero, bit 6, 7, and 8 of the K2 byte are not modified by the transmit line overhead processor.

Line RDI may also be inserted into the transmit stream, when receive line AIS is detected, by setting LAISINS bit to high in the Line RDI Control register. Setting of this register bit is also required for line RDI insertion via the transmit ring control port.

Reserved

The Reserved bits must be set low for proper operation of SPECTRA 4x155.

APSREG

The APSREG bit selects the source for the transmit APS channel on the indexed channel. When APSREG is a logic zero, the transmit APS channel is inserted by the TTOC block from the bit serial input TOH which is shifted in on the rising edge of TOHCLK. When APSREG is a logic one, the transmit APS channel is inserted from the TLOP Transmit K1 Register and the TLOP Transmit K2 Register.

Registers 0185H, 0285H, 0385H, and 0485H: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	R/W	DB2	0

DB2

The DB2 bit controls the insertion of bit errors continuously in each of the line BIP-8 bytes (B2 bytes) on the indexed channel. When DB2 is set high, each bit of every B2 byte is inverted.

Registers 0186H, 0286H, 0386H, and 0486H: TLOP Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control register of the indexed channel is logic one. K1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the TLOP Transmit K2 Register are inserted in the SONET/SDH stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Registers 0187H, 0287H, 0387H, and 0487H: TLOP Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register of the indexed channel is logic one. K2[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K2[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the TLOP Transmit K1 register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing to the TLOP Transmit K1 register.

Registers 0188H, 0288H, 0388H, and 0488H: TTOC Transmit Overhead Output Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	1
Bit 2	R/W	TSLD_TS	1
Bit 1	R/W	TSLD_VAL	0
Bit 0	R/W	TSLD_SEL	0

TSLD_SEL

The transmit data line select (TSLD_SEL) bit determines the content of the incoming TSLDm stream. When TSLD_SEL is low, the TSLDm stream contains the section DCC (D1–D3). When TSLD_SEL is high, the TSLDm stream contains the line DCC (D4–D12). When TSLD_SEL selects the line DCC on TSLDm, section DCC (D1–D3) can be controlled using the TTOHm input or can be forced to an all-ones or all-zeros pattern using the TSLD_VAL.

TSLD_VAL

The transmit section/line DCC value (TSDVAL) bit selects an all-ones or all-zeros value on the section DCC data (D1, D2, D3) of the indexed channel when TSLD_SEL register bit selects the TSLDm input to provide the line DCC. Setting TSDVAL to high will force the section data link (D1, D2, D3) to all-ones and setting the bit to low will force the data to all-zeros. In such a case, the section DCC still can be controlled using the TTOHm input.

TSLD_TS

The transmit section/line data link tri-state (TSLD_TS) bit controls the tri-stating of the TSLDCLKm output. TSLD_TS defaults to logic one so that TSLDCLKm will be tri-stated after a reset.

Reserved

The Reserved bits must be kept at their default value for proper operation of SPECTRA 4x155.

Registers 0189H, 0289H, 0389H, and 0489H: TTOC Transmit Overhead Byte Control

Bit	Type	Function	Default
Bit 7	R/W	TREN	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	TAPS_SEL	0
Bit 4	R/W	Z0INS	0
Bit 3	R/W	UNUSED_EN	0
Bit 2	R/W	UNUSED_V	0
Bit 1	R/W	NAT_EN	0
Bit 0	R/W	NAT_V	0

NAT_V

The NAT_V bit determines the value to insert into the national use transport overhead bytes of the indexed channel when the NAT_EN register bit is programmed to overwrite these bytes. When NAT_V is set high, the national use transport overhead bytes are set to FFH. When NAT_V is set low, the national use transport overhead bytes are set to 00H. This register bit has not effect when the NAT_EN register bit is set to logic zero.

NAT_EN

The NAT_EN bit enables overwriting the national use transport overhead bytes of the indexed channel with an all-ones or all-zeros pattern. The national use TOH bytes affected when NAT_EN is set high are the, Z0, F1 and E2 bytes of STS-1 (STM-0/AU-3) #2 and #3. When this bit is high, these bytes are overwritten with an all-ones pattern or all-zeros pattern as controlled by the NAT_V bit. When NAT_EN is set low, the national use TOH bytes are controlled by the TTOHEN input or Z0INS register bit. The Z0INS register bit has precedence over NAT_EN for the setting of Z0. NAT_EN has precedence over TTOHENm for all three bytes.

UNUSED_V

The UNUSED_V bit determines the value to insert into the unused transport overhead bytes of the indexed channel when the UNUSED_EN register bit is programmed to overwrite these bytes. When UNUSED_V is set high, the unused transport overhead bytes are set to FFH. When UNUSED_V is set low, the unused transport overhead bytes are set to 00H. This register bit has not effect when the UNUSED_EN register bit is set to logic zero.

UNUSED_EN

The UNUSED_EN bit enables overwriting the unused transport overhead bytes of the indexed channel with an all-ones or all-zeros pattern. When UNUSED_EN is set high, the unused transport overhead bytes are overwritten with an all-ones pattern or all-zeros pattern as controlled by the UNUSED_V bit. When UNUSED_EN is set low, the unused transport overhead bytes are controlled by the TTOHENm input. When UNUSED_EN and TTOHENm are both high, the UNUSED_EN has precedence.

The unused bytes are illustrated in Table 11.

Table 11 Transport overhead National and Unused bytes

A1	A1	A1	A2	A2	A2	J0	N*	N*
B1	U	U	E1	U	U	F1	N	N
D1	U	U	D2	U	U	D3	U	U
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2	K1	U	U	K2	U	U
D4	U	U	D5	U	U	D6	U	U
D7	U	U	D8	U	U	D9	U	U
D10	U	U	D11	U	U	D12	U	U
S1	U	U	U	U	M1	E2	N	N

Notes:

N - National use byte.

N* - National use byte, controlled by the Z0INS bit in this register.

U - Unused byte.

Z0INS

The Z0INS bit controls the values inserted in the transmit Z0 bytes on the indexed channel. When Z0INS is logic one, the value contained in the TTOC Transmit Z0 register is inserted in the Z0 bytes. ZOINS has precedence over the NAT_EN register bit, the TTOHENm input and the TSOP Control Register DC1 register bit. When Z0INS is logic zero, the Z0 bytes may be inserted via the NAT_EN register bit or TTOHENm. Leaving the Z0 bytes undefined and programming the DC1 bit in the TSOP Control register to logic zero will allow the values 02H and 03H to be inserted in the Z0 byte of 2nd and 3rd STS-1 (STM-0/AU-3) respectively. Note: Values inserted using the transmit transport overhead port take precedence.

TAPS_SEL

The transmit APS select (TAPS_SEL) bit selects the source of the transmit APS (K1/K2) bytes of the indexed channel. When TAPS_SEL is low, the TTOHENm is used as source for the APS bytes. When TAPS_SEL is high, the APS bytes are sourced from Transmit alarm port (TAD).

Reserved

The Reserved bits must be kept at their default value for proper operation of SPECTRA 4x155.

TREN

The transmit trace enable (TREN) bit enables the insertion of the section trace message programmed in the SSTB of the indexed channel. Setting this bit to logic one will enable the insertion of the SSTB stored message into the transmit stream. When setting this bit to logic zero, the section trace message may be inserted byte-by-byte using the TTOH and TTOHEN overhead inputs. When not asserting TTOHEN for the insertion of J0 or enabling TREN, the TSOP DC1 register bit in the TSOP Control Register may be used to insert the 01h value into the J0 byte position.

Registers 018AH, 028AH, 038AH, and 048AH: TTOC Transmit Z0

Bit	Type	Function	Default
Bit 7	R/W	Z0[7]	1
Bit 6	R/W	Z0[6]	1
Bit 5	R/W	Z0[5]	0
Bit 4	R/W	Z0[4]	0
Bit 3	R/W	Z0[3]	1
Bit 2	R/W	Z0[2]	1
Bit 1	R/W	Z0[1]	0
Bit 0	R/W	Z0[0]	0

Z0[7:0]

Z0[7:0] contains the value inserted in Z0 bytes of the indexed channel transmit stream when the Z0INS register bit is logic one. Z0[7] is the most significant bit corresponding to bit 1, the first bit transmitted. Z0[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The Z0 byte defaults to “11001100b”.

Registers 018BH, 028BH, 038BH, and 048BH: TTOC Transmit S1

Bit	Type	Function	Default
Bit 7	R/W	S1[7]	0
Bit 6	R/W	S1[6]	0
Bit 5	R/W	S1[5]	0
Bit 4	R/W	S1[4]	0
Bit 3	R/W	S1[3]	0
Bit 2	R/W	S1[2]	0
Bit 1	R/W	S1[1]	0
Bit 0	R/W	S1[0]	0

S1[7:0]

The value written into these register bits is inserted in the first S1/Z1 (S1) byte position of the indexed channel transmit stream. The S1 byte is used to carry synchronization status messages between line terminating network elements. S1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. S1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The TTOHEN input takes precedence over the contents of this register.

Register 1001H: Drop Bus STM-1 #1 AU-3 #1 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the Time-Slot Interchange (TSI) operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #1 AU-3 #1 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1002H: Drop Bus STM-1 #2 AU-3 #1 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #2 AU-3 #1 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1003H: Drop Bus STM-1 #3 AU-3 #1 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #3 AU-3 #1 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1004H: Drop Bus STM-1 #4 AU-3 #1 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #4 AU-3 #1 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1005H: Drop Bus STM-1 #1 AU-3 #2 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	1

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #1 AU-3 #2 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1006H: Drop Bus STM-1 #2 AU-3 #2 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	1

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #2 AU-3 #2 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1007H: Drop Bus STM-1 #3 AU-3 #2 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	1

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #3 AU-3 #2 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1008H: Drop Bus STM-1 #4 AU-3 #2 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	1

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #4 AU-3 #2 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1009H: Drop Bus STM-1 #1 AU-3 #3 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	1
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #1 AU-3 #3 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 100AH: Drop Bus STM-1 #2 AU-3 #3 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	1
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #2 AU-3 #3 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 100BH: Drop Bus STM-1 #3 AU-3 #3 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	1
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #3 AU-3 #3 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 100CH: Drop Bus STM-1 #4 AU-3 #3 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	1
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation at the Telecom Drop bus. This register selects an STS-1 (STM-0/AU-3) or equivalent of the receive stream for insertion in time-slot STM-1 #4 AU-3 #3 of the Drop bus. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 0D01H to 0D0CH enable a straight-through connection of the receive stream to the Drop bus.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams in the STS-3 (STM-1) receive stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register: Register 1020H: Drop Bus DLL Configuration

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	OVERRIDE	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

OVERRIDE

The override control (OVERRIDE) disables the DLL operation. When OVERRIDE is set low, the Drop bus clock (DCK) is processed by the DLL before clocking the Drop interface logic. The DLL must not be overridden (set low) in 77.76 MHz Drop interface mode if the specified propagation delays are to be met for the interface. When OVERRIDE is set high, the Drop bus clock (DCK) is not processed by the DLL before clocking the Drop interface logic. The DLL must be overridden (set high) in 19.44 MHz Drop interface mode if the specified propagation delays are to be met for the interface. The DLL does not function at 19.44 MHz.

Note: The default configuration of the Drop BUS (DTMODE) is 19.44 MHz. The default mode of the DLL is enabled (OVERRIDE low). These two default modes conflict each other and a configuration of the system bus mode or the DLL is necessary for proper functioning.

Register 1021H: Drop Bus DLL Reserved

Bit	Type	Function	Default
Bit 7	R/W	Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits must be kept at their default values for proper functioning of the SPECTRA 4x155

Register 1022H: Drop Bus DLL Reset Register

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a software reset of the DLL. A software reset should be applied after when setting the device in 77.76 MHz DROP interface mode and the DCK input is frequency stable.

Reserved

The Reserved register read bits must be ignored when reading the SPECTRA 4x155.

Register 1023H: Drop Bus DLL Control Status

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	CHANGEI	X
Bit 3	—	Unused	X
Bit 2	R	ERROR	X
Bit 1	R	CHANGE	0
Bit 0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit RUN indicates the DLL has found a delay line tap in which the Drop interface timings will be met at 77.76 Mhz interface mode. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic one. The RUN register bit is cleared only by a system reset or a software reset (writing to register 00A6H).

CHANGE

The delay line tap change register bit CHANGE indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight DCK cycles when the DLL moves to a new delay line tap. A fixed value of 1 indicates that the DLL has not locked to a frequency and should be reset.

ERRORI

The delay line error register bit (ERRORI) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERRORI is set high. ERROR is set low, when the DLL captures lock again. Writing to register 1022H if the ERROR condition persists, should reset the DLL.

CHANGEI

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one. The CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Reserved

The Reserved register read bits must be ignored when reading the SPECTRA 4x155.

Register 1030H: Drop Bus Configuration

Bit	Type	Function	Default
Bit 7	R/W	DTMODE	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ODDPD	0
Bit 1	R/W	INCDPL	0
Bit 0	R/W	INCDC1J1V1	0

This register allows the parity insertion in the Drop bus of the SPECTRA 4x155 to be configured.

INCDC1J1V1

The INCDC1J1V1 bit controls whether the composite timing signals, DC1J1V1[4:1], on the Drop buses are used to calculate the corresponding parity signals, DDP[4:1]. When INCDC1J1V1 is set high, the parity signal set includes the DC1J1V1[4:1] signals. When INCDC1J1V1 is set low, parity is calculated without regard to the state of the corresponding DC1J1V1 signal on the Drop bus.

INCDPL

The INCDPL bit controls whether the payload active signals, DPL[4:1], on the Drop buses are used to calculate the corresponding parity signals, DDP[4:1]. When INCDPL is set high, the parity signal set includes the DPL[4:1] signals. When INCDPL is set low, parity is calculated without regard to the state of the corresponding DPL signal on the Drop bus.

ODDPD

The ODDPD bit controls the parity placed on the Drop bus parity signals, DDP[4:1]. When set high, the ODDPD bit configures the bus parity to be odd. When set low, the ODDPD bit configures the bus parity to be even.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

DTMODE

The Drop Telecom bus mode select (DTMODE) bit is used to select the operation of the Drop Bus system side interface when Telecom mode is enabled. When the DTMODE bit is set low, the single (STM-4) 77.76 MHz byte Telecom Drop Bus Interface is supported and the Drop Bus DLL must be enabled for proper timing. When the DTMODE bit is set high, the four (STM-1) 19.44 MHz byte Telecom Drop Bus Interface is supported and Drop Bus DLL must be disabled (OVERRIDE high) for proper timing.

Note: The default configuration of the Drop BUS (DTMODE) is 19.44 MHz. The default mode of the DLL is enabled (OVERRIDE low). These two default modes conflict each other and a configuration of the system bus mode or the DLL is necessary for proper functioning.

Register 1081H: SPECTRA 4x155 Add Bus STM-1 #1 AU-3 #1 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #1 AU-3 #1 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) Add bus stream as summarized in the table below.

STM1SEL[1:0]	STM-1 Add bus stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1082H: SPECTRA 4x155 Add Bus STM-1 #2 AU-3 #1 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #2 AU-3 #1 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1083H: SPECTRA 4x155 Add Bus STM-1 #3 AU-3 #1 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #3 AU-3 #1 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1084H: SPECTRA 4x155 Add Bus STM-1 #4 AU-3 #1 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #4 AU-3 #1 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1085H: SPECTRA 4x155 Add Bus STM-1 #1 AU-3 #2 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	1

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #1 AU-3 #2 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1086H: SPECTRA 4x155 Add Bus STM-1 #2 AU-3 #2 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	1

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #2 AU-3 #2 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1087H: SPECTRA 4x155 Add Bus STM-1 #3 AU-3 #2 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	1

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #3 AU-3 #2 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1088H: SPECTRA 4x155 Add Bus STM-1 #4 AU-3 #2 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	0
Bit 0	R/W	AU-3SEL[0]	1

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #4 AU-3 #2 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 1089H: SPECTRA 4x155 Add Bus STM-1 #1 AU-3 #3 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	1
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #1 AU-3 #3 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 108AH: SPECTRA 4x155 Add Bus STM-1 #2 AU-3 #3 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	0
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	1
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #2 AU-3 #3 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 108BH: SPECTRA 4x155 Add Bus STM-1 #3 AU-3 #3 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	0
Bit 1	R/W	AU-3SEL[1]	1
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #3 AU-3 #3 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 108CH: SPECTRA 4x155 Add Bus STM-1 #4 AU-3 #3 Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	STM1SEL[1]	1
Bit 2	R/W	STM1SEL[0]	1
Bit 1	R/W	AU-3SEL[1]	1
Bit 0	R/W	AU-3SEL[0]	0

This is a configuration register for the TSI operation on the Telecom Add bus. This register selects an STS-1 (STM-0/AU-3) or equivalent on the Add bus for insertion in time-slot STM-1 #4 AU-3 #3 of the transmit stream. The default values of STM1SEL[1:0] and AU-3SEL[1:0] for registers 1061H to 106CH enable a straight-through connection of the Add bus to the transmit stream.

AU-3SEL[1:0]

The AU-3SEL[1:0] bits select one of three STS-1 (STM-0/AU-3) streams on the STS-3 (STM-1) Add bus stream selected by the STM1SEL[1:0] bits. The AU-3SEL[1:0] options are summarized in the table below.

AU-3SEL[1:0]	AU-3 Receive Stream #
00	STS-1 (STM-0/AU-3) #1
01	STS-1 (STM-0/AU-3) #2
10	STS-1 (STM-0/AU-3) #3
11	Reserved

STM1SEL[1:0]

The STM1SEL[1:0] bits select the STS-3 (STM-1) receive stream as summarized in the table below.

STM1SEL[1:0]	STM-1 receive stream #
00	STS-3 (STM-1) #1
01	STS-3 (STM-1) #2
10	STS-3 (STM-1) #3
11	STS-3 (STM-1) #4

Register 10B0H: SPECTRA 4x155 Add Bus Configuration #1

Bit	Type	Function	Default
Bit 7	R/W	AFPEN	0
Bit 6	R/W	ATMODE	1
Bit 5	R/W	Reserved	0
Bit 4	R/W	ATSICLK_RST	0
Bit 3	R/W	ATSICLK_ISOLATE	0
Bit 2	R/W	ODDPA	0
Bit 1	R/W	INCAPL	0
Bit 0	R/W	INCAC1J1V1	0

This register allows the Add bus of the SPECTRA 4x155 to be configured.

INCAC1J1V1

The INCAC1J1V1 bit controls whether the composite timing signals (AC1J1V1[4:1]) in the Add buses are used to calculate the corresponding parity signals (ADP[4:1]). When INCAC1J1V1 is set high, the parity signal set includes the AC1J1V1[4:1] signals. When INCAC1J1V1 is set low, parity is calculated without regard to the state of the corresponding AC1J1V1 signal.

INCAPL

The INCAPL bit controls whether the payload active signals (APL[4:1]) in the Add buses are used to calculate the corresponding parity signals (ADP[4:1]) and whether the payload active signals (APL[4:1]) in the Add buses are included in the condition to set high the ACA[4:1] activity monitors. When INCAPL is set high, the parity signal set includes the APL[4:1] signals and the condition to set the ACA[4:1] activity monitors bits includes these signals. When INCAPL is set low, parity is calculated without regard to the state of the corresponding APL signal and the activity monitor will be set high even when the APL signals do not toggle.

ODDPA

The ODDPA bit controls the parity expected on the Add bus parity signal (ADP[4:1]). When set high, the ODDPA bit configures the Add bus parity to be odd. When set low, the ODDPA bit configures the Add bus parity to be even.

ATSICLK_ISOLATE

The ATSI_ISOLATE bit is used to disable the realignment by AC1J1V1/AFP[1] Add BUS pin on the generated system side clocks of the 12 TPPS slices in the Add TSI. This bit should only be used when all 12 TPPS slices are placed in PRBS Autonomous mode and the AC1J1V1/AFP[1] (and/or APL) Add Bus interface cannot maintain a constant frame alignment (C1 or FP moving around). Programming this bit to logic one will mask low AC1J1V1/AFP[1] pin and the generated clocks will fly-wheel on the last C1 or FP received on AC1J1V1/AFP[1]. The data from the Add Bus cannot be analyzed or monitored. Programming this bit to logic zero has no affect. This bit is mainly for diagnostic purpose and to let the user isolate the 12 TPPS slices from the Add bus.

ATSICLK_RST

The ATSICLK_RST bit is used to force a constant realignment of the system side clocks generated in the TPPS's. This bit can be used in conjunction with ATSICLK_ISOLATE to force the alignment of the generated clocks. When programmed high the generated clocks are disabled and realign. Upon programming the bit to logic zero, the generated clocks will start again in a known sequence with slice #1 clocked first. The TPPS PRBS generators must be regenerated each time realignment is forced.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

ATMODE

The Add Telecom bus mode select (ATMODE) bit is used to select the operation of the Add Bus system side interface when Telecom mode is enabled. When the ATMODE bit is set low, the single (STM-4) 77.76 MHz byte Telecom Add Bus Interface is supported. When the AMTODE bit is set high, the four (STM-1) 19.44 MHz byte Telecom Add Bus Interface is supported.

AFPEN

The Add bus reference frame position input enable (AFPEN) bit controls the interpretation of the AC1J1V1[4:1]/AFP[4:1] input signals. When set high, the AC1J1V1[4:1]/AFP[4:1] signals provide the Add bus reference frame position (AFP) indications to the corresponding Add buses. When set low, the AC1J1V1[4:1]/AFP[4:1] signals provide the Add bus composite timing signals (AC1J1V1) to the corresponding Add buses.

Register 10B1H: SPECTRA 4x155 Add Bus Configuration #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	ADPACTDIS	0

This register allows the Add bus of the SPECTRA 4x155 to be configured.

ADPACTDIS

The ADPACTEN bit controls whether activity on the ADP1-4 inputs is monitored and included in the ACA[m] status bit of the SPECTRA 4x155 Add Bus Signal Activity Monitor register. When this bit is set low, activity on the ADP1-4 inputs is included in the corresponding ACA1-4 status bit. When this bit is set high, the ACA1-4 status bits are not affected by the activity on the ADP1-4 inputs.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

Register 10B2H: SPECTRA 4x155 Add Bus Parity Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	APE1	0
Bit 6	R/W	APE2	0
Bit 5	R/W	APE3	0
Bit 4	R/W	APE4	0
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

APE1-4

The Add bus parity interrupt enable (APIE1-4) bit controls the assertion of an interrupt when a parity error event is indicated by the corresponding parity interrupt status in the SPECTRA 4x155 Add Bus Parity Interrupt Status register. When APE1-4 is set high, an interrupt will be asserted (INTB set low) on a parity error event indication. When APEn is set low, parity error events will not affect the interrupt output (INTB).

Register 10B4H: SPECTRA 4x155 Add Bus Parity Interrupt Status

Bit	Type	Function	Default
Bit 7	R	API1	X
Bit 6	R	API2	X
Bit 5	R	API3	X
Bit 4	R	API4	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register reports the parity interrupt status of the SPECTRA 4x155 Telecom Add buses #1 (AD[7:0]), #2 (AD[15:8]), #3 (AD[23:16]) and #4 (AD[31:24]).

Reserved

The Reserved read bits must be ignored when reading then in the SPECTRA-4X155.

API1-4

The Add bus parity interrupt status (APIm) bit reports parity error events detected at the corresponding Add bus. APIm is set high on detection of a parity error event on the corresponding Add bus. This bit and the interrupt are cleared when this register is read. The occurrence of parity error events is an indication of mis-configured parity generation/detection or actual hardware problem at the Add bus input.

Register 10B6H: SPECTRA 4x155 System Side Clock Activity Monitor

Bit	Type	Function	Default
Bit 7	R	ACKA	X
Bit 6	R	DCKA	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

This register provides activity monitoring on SPECTRA 4x155 system-side clock inputs. When a monitored input makes a low-to-high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect stuck at conditions.

DCKA

The DCK active (DCKA) bit monitors for low-to-high transitions on the DCK input. DCKA is set high on a rising edge of DCK, and is set low when this register is read.

ACKA

The ACK active (ACKA) bit monitors for low-to-high transitions on the ACK input. ACKA is set high on a rising edge of ACK, and is set low when this register is read.

Register 10B7H: SPECTRA 4x155 Add Bus Signal Activity Monitor

Bit	Type	Function	Default
Bit 7	R	ADA1	X
Bit 6	R	ACA1	X
Bit 5	R	ADA2	X
Bit 4	R	ACA2	X
Bit 3	R	ADA3	X
Bit 2	R	ACA3	X
Bit 1	R	ADA4	X
Bit 0	R	ACA4	X

This register provides activity monitoring on SPECTRA 4x155 signal and data inputs for byte Add TelecomBus operation. When a monitored input makes a low-to-high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read periodically to detect "stuck at" conditions.

ACA1-4

The Add bus control active (ACAm) bit monitors for low-to-high transitions on the corresponding APL[m], AC1J1V1[m] and ADP[m] inputs. ACA1-4 is set high when rising edges have been observed on all these signals, and is set low when this register is read. In applications where APL may be tied low, APL may be excluded from the activity monitor status using the INCAPL register bit. If ADP is tied low or high, it may be excluded from the activity monitor status using the ADPACTDIS register bit.

ADA1-4

The Add bus data active (ADAm) bit monitors for low-to-high transitions on the corresponding AD[7:0] (#1), AD[15:8] (#2), AD[23:16] (#3) or AD[31:24] (#4) bus when configured for byte Telecom Add bus mode. ADAm is set high when rising edges have been observed on all the required signals in the corresponding Telecom Add bus, and is set low when this register is read.

Registers 1100H, 1200H, 1300H, 1400H, 1500H, 1600H, 1700H, 1800H, 1900H, 1A00H, 1B00H, and 1C00H: RPPS Configuration & Slice ID

Bit	Type	Function	Default
Bit 7	R/W	MASTER	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	STM1_CONCAT	0
Bit 3	R	RX_SLICE_ID[3]	X
Bit 2	R	RX_SLICE_ID[2]	X
Bit 1	R	RX_SLICE_ID[1]	X
Bit 0	R	RX_SLICE_ID[0]	X

This register allows the operational mode of the SPECTRA 4x155 Receive Path Processing Slice (RPPS) to be configured.

RX_SLICE_ID[3:0]

The RX_SLICE_ID[3:0] bits indicate the RX path processing slice numbers 1 to 12. These register bits exist for test purposes only. The read back values are from 0 to 11, 0 being slice 1 and eleven being slice 12.

STM1_CONCAT

The STM1_CONCAT bit is used to configure the RPPS to be processing TU2, TU11 or TU12 inside an STM-1(VC-4). When configured, TUAIS is properly asserted as defined by the ITUAIS in the RTAL. When set high, the RTAL fixed stuff columns are columns 1, 2 and 3. This supports TU2, TU11 and TU12 payloads in a VC-4. When set low, the RTAL fixed stuff columns are columns 30 and 59. When set low TUAIS cannot be inserted properly. This bit can otherwise be set low.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

MASTER

When set high, the MASTER bit enables the RPPS to control and co-ordinate the processing of an STS-1 (STM-0/AU-3) or an STS-3c (STM-1/AU-4) receive stream as the master. It also enables the RPPS to control and co-ordinate the distributed PRBS payload sequence generation and monitoring. When the MASTER bit is set low, the RPPS operates in a slave mode and its operation is co-ordinated by the associated master RPPS. Setting this bit low (slave mode) does not necessarily mask alarms or errors that only a master slice can declare. The alarms or errors must be disabled via the appropriate register bits.

Registers 1102H, 1202H, 1302H, 1402H, 1502H, 1602H, 1702H, 1802H, 1902H, 1A02H, 1B02H, and 1C02H: RPPS Path Configuration

Bit	Type	Function	Default
Bit 7	R/W	ENDV1	1
Bit 6	R/W	MONRS	0
Bit 5	R/W	ALMJ1V1	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register allows the operational mode of the SPECTRA 4x155 RPPS Path functions to be configured. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

ALMJ1V1

When set high, the ALMJ1V1 bit disables the realignment of the Drop TelecomBus J1 and V1 indication on DC1J1V1 when the RPOP block is in the LOP or PAIS state. Conditional on the rate adaption FIFO (RTAL) not overflowing or underflowing, the~~The~~ J1 and V1 pulses will flywheel at their previous position prior to entry to the LOP or PAIS state. When forcing consequential AIS-P on the DROP bus via the RPPS Path AIS Control #1 and #2 registers or via the IPAIS register bit in the RTAL, the RTAL FIFO stops adjusting the FIFO level via outgoing pointer justifications and may over/underflow. Setting this bit in slave slices has no effect. Setting this bit in the master slice will cause BIP errors for STS-3c(STM-1/AU4) payloads during the LOP or PAIS state, in the event that the received B3 is not already corrupted.

MONRS

When set high, the MONRS selects the receive side pointer justification events counters to monitor the receive stream directly. When MONRS is set low, the counters accumulate pointer justification events on the Drop bus.

ENDV1

When set high, the ENDV1 bit configures the DC1J1V1 output to mark the frame, SPE (VC) alignments and tributary multi-frame alignments (C1, J1 and V1 bytes). When ENDV1 is set low, DC1J1V1 marks only the frame and SPE alignments and does not indicate the tributary multi-frame alignment. It is recommended that ENDV1 be set low in normal operation to disable the V1 pulse on DC1J1V1. PMC-Sierra's tributary-processing devices (PM5362 TUPP+, PM5363 TUPP+622, PM5365 TEMAP, PM8315 TEMUX, PM8316 TEMUX-84, and PM5366 TEMAP) interpret the H4 byte in the path overhead to identify the tributary multi-frame alignment, so they do not require the V1 pulse. In applications that do not use tributaries, there is no definition for multi-frame and therefore no need for the V1 pulse on DC1J1V1.

Registers 1110H, 1210H, 1310H, 1410H, 1510H, 1610H, 1710H, 1810H, 1910H, 1A10H, 1B10H, and 1C10H: RPPS Path AIS Control #1

Bit	Type	Function	Default
Bit 7	R/W	LOMTUAIS	0
Bit 6	R/W	ALMAIS	0
Bit 5	R/W	DPAIS_EN	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LOPAIS	0
Bit 2	R/W	PAISAIS	0
Bit 1	R/W	LOPCONPAIS	0
Bit 0	R/W	PAISCONPAIS	0

This register along with the RPPS Receive Path AIS Control #2 register controls the auto assertion of path AIS on the Drop bus. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

PAISCONPAIS

When set high, the PAISCONPAIS bit enables path AIS insertion on the Drop bus when Path AIS concatenation (PAISCON) events are detected. When PAISCONPAIS is set low, Path AIS concatenation events have no effect on the Drop bus.

Note: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low. The register bit will also force the associated master and slave RPPSs to insert path AIS.

LOPCONPAIS

When set high, the LOPCONPAIS bit enables path AIS insertion on the Drop bus when loss of pointer concatenation (LOPCON) events are detected. When LOPCONPAIS is set low, loss of pointer concatenation events have no effect on the Drop bus.

Note: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low. The register bit will also force the associated master and slave RPPSs to insert path AIS.

PAISAIS

When set high, the PAISAIS bit enables path AIS insertion on the Drop bus when path AIS is detected in the receive stream. When PAISAIS is set low, path AIS events have no effect on the Drop bus.

Note: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slave RPPSs to insert path AIS.

When ALMJ1V1 and PAISAIS are set high together and the device is forcing AIS on the DROP Bus due to PAISAIS, the forcing will not stop immediately by disabling the PAISAIS register bit. The forcing of AIS will only stop when the receive line AIS-P is cleared. When ALMJ1V1 is set low, setting low the PAISAIS register bit during PAIS will stop the forcing of AIS on the DROP bus immediately.

LOPAIS

When set high, the LOPAIS bit enables path AIS insertion on the Drop bus when LOP events are detected in the receive stream. When LOPAIS is set low, LOPs have no effect on the Drop bus.

Note: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slave RPPSs to insert path AIS.

When ALMJ1V1 and LOPAIS are set high together and the device is forcing AIS on the DROP Bus due to LOPAIS, the forcing will not stop immediately by disabling the LOPAIS register bit. The forcing of AIS will only stop when the receive line AIS-P is cleared. When ALMJ1V1 is set low, setting low the LOPAIS register bit during PAIS will stop the forcing of AIS on the DROP bus immediately.

DPAIS_EN

When set high, the DPAIS_EN bit enables path AIS insertion into the Drop stream via the corresponding time-slot of the DPAIS input signal. When DPAIS_EN is set low, the DPAIS input signal has no effect on the Drop stream of that slice. Forcing DPAIS on master slice will also force the slave slices into PAIS when DPAIS_EN register bit of the master is set high.

ALMAIS

When set high, the ALMAIS bit enables path AIS assertion when LOS, LOF, or LAIS events are detected in the receive stream. When ALMAIS is set low, the above events have no effect on path AIS.

LOMTUAIS

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the Drop bus when LOM events are detected in the receive stream. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. The STM1_CONCAT bit must be set high for TU2, TU11 and TU12 payloads in a VC-4.When LOMTUAIS is set low, loss of multi-frame events have no effect on the Drop bus. LOMTUAIS must be set low when processing TU3 or payload not requiring tributary multi-frame alignment.

Note: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slave RPPSs to insert tributary AIS.

Registers 1111H, 1211H, 1311H, 1411H, 1511H, 1611H, 1711H, 1811H, 1911H, 1A11H, 1B11H, and 1C11H: RPPS Path AIS Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	UNEQAIS	0
Bit 5	R/W	PSLUAIS	0
Bit 4	R/W	PSLMAIS	0
Bit 3	R/W	Reserved	0
Bit 2	—	Unused	0
Bit 1	R/W	TIUAIS	0
Bit 0	R/W	TIMAIS	0

This register along with the RPPS Path AIS Control #1 register controls the auto assertion of path AIS on the Drop bus. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

TIMAIS

When set high, the TIMAIS bit enables path AIS insertion on the Drop bus when path trace identifier mismatch (TIM) events are detected in the receive stream. When TIMAIS is set low, trace identifier (mode 1) mismatch events have no effect on the Drop bus.

Note: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPSs to insert path AIS.

TIUAIS

When set high, the TIUAIS bit enables path AIS insertion on the Drop bus when path trace identifier (mode 1) unstable events are detected in the receive stream. When TIUAIS is set low, trace identifier (mode 1) unstable events have no effect on the Drop bus.

Note: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPSs to insert path AIS.

PSLMAIS

When set high, the PSLMAIS bit enables path AIS insertion on the Drop bus when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMAIS is set low, path signal label mismatch events have no effect on the Drop bus.

Note: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPSs to insert path AIS.

PSLUAIS

When set high, the PSLUAIS bit enables path AIS insertion on the Drop bus when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUAIS is set low, path signal label unstable events have no effect on the Drop bus.

Note: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPSs to insert path AIS.

UNEQAIS

When set high, the UNEQAIS bit enables path AIS insertion on the Drop bus when path signal label in the receive stream indicates unequipped status (UNEQ). When UNEQAIS is set low, the path signal label unequipped status has no effect on the Drop bus.

Note: This register bit should only be used when the RPPS is configured as a master. Otherwise, it should normally be set low. The register bit will also force the associated slaves RPPSs to insert path AIS.

Registers 1114H, 1214H, 1314H, 1414H, 1514H, 1614H, 1714H, 1814H, 1914H, 1A14H, 1B14H, and 1C14H: RPPS Path REI/RDI Control #1

Bit	Type	Function	Default
Bit 7	R/W	AUTOPREI	0
Bit 6	R/W	ALMPRDI	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LOPPRDI	0
Bit 2	R/W	PAISPRDI	0
Bit 1	R/W	LOPCONPRDI	0
Bit 0	R/W	PAISCONPRDI	0

This register along with the RPPS Path REI/RDI Control #2 register controls the auto assertion of path RDI (G1 bit 5) in the local TPOP or a mate TPOP (via the RAD PRDI5 bit position) of the corresponding TPPS. These register bits should normally be set low when the RPPS is configured as a slave.

PAISCONPRDI

When set high, the PAISCONPRDI bit enables path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. When PAISCONPRDI is set low, path AIS concatenation events have no effect on path RDI.

LOPCONPRDI

When set high, the LOPCONPRDI bit enables path RDI assertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. When LOPCONPRDI is set low, loss of pointer concatenation events

PAISPRDI

When set high, the PAISPRDI bit enables path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. When PAISPRDI is set low, PAIS states have no effect on path RDI.

LOPPRDI

When set high, the LOPPRDI bit enables path RDI assertion when LOP events are detected in the receive stream. When LOPPRDI is set low, LOP events have no effect on path RDI.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

ALMPRDI

When set high, the ALMPRDI bit enables path RDI assertion when LOS, LOF, or LAIS events are detected in the receive stream. When ALMPRDI is set low, the above events have no effect on path RDI.

AUTOPREI

The AUTOPREI bit enables the automatic insertion of path REI events in the local or mate transmitter. When AUTOPREI is a logic one, receive B3 errors detected by the SPECTRA 4x155 are automatically inserted in the G1 byte of the local transmit stream (as enabled using the RXSEL[1:0] bits in the SPECTRA 4x155 TPPS Path Configuration register). In Addition, REI events are indicated on the RAD output. When AUTOPREI is a logic zero, path REI events are not automatically inserted in the local transmit stream.

REI events are not indicated on the RAD output.

Registers 1115H, 1215H, 1315H, 1415H, 1515H, 1615H, 1715H, 1815H, 1915H, 1A15H, 1B15H, and 1C15H: RPPS Path REI/RDI Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	UNEQPRDI	0
Bit 5	R/W	PSLUPRDI	0
Bit 4	R/W	PSLMPRDI	0
Bit 3	R/W	Reserved	0
Bit 2	—	Unused	0
Bit 1	R/W	TIUPRDI	0
Bit 0	R/W	TIMPRDI	0

This register along with the RPPS Path REI/RDI Control #1 register controls the auto assertion of path RDI (G1 bit 5) in the local TPOP or a mate TPOP (via the RAD PRDI5 bit position) of the corresponding TPPS. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

TIMPRDI

When set high, the TIMPRDI bit enables path RDI assertion when path trace identifier (mode 1) mismatch (TIM) events are detected in the receive stream. When TIMPRDI is set low, trace identifier (mode 1) mismatch events have no effect on path RDI.

TIUPRDI

When set high, the TIUPRDI bit enables path RDI assertion when path trace identifier (mode 1) unstable (TIU) events are detected in the receive stream. When TIUPRDI is set low, trace identifier (mode 1) unstable events have no effect on path RDI.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

PSLMPRDI

When set high, the PSLMPRDI bit enables path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPRDI is set low, path signal label mismatch events have no effect on path RDI.

PSLUPRDI

When set high, the PSLUPRDI bit enables path RDI assertion when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUPRDI is set low, path signal label unstable events have no effect on path RDI.

UNEQPRDI

When set high, the UNEQPRDI bit enables path RDI assertion when the path signal label in the receive stream indicates unequipped status. When UNEQPRDI is set low, the path signal label unequipped status has no effect on path RDI.

Registers 1116H, 1216H, 1316H, 1416H, 1516H, 1616H, 1716H, 1816H, 1916H, 1A16H, 1B16H, and 1C16H: Reserved

Bit	Type	Function	Default
Bit 7	—	Reserved	X
Bit 6	—	Reserved	X
Bit 5	—	Reserved	X
Bit 4	—	Reserved	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved read/write bits should be set to logic zero for proper functioning of the SPECTRA 4x155.

Registers 1118H, 1218H, 1318H, 1418H, 1518H, 1618H, 1718H, 1818H, 1918H, 1A18H, 1B18H, and 1C18H: RPPS Path Enhanced RDI Control #1

Bit	Type	Function	Default
Bit 7	R/W	PERDI_EN	0
Bit 6	R/W	ALMPERDI	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LOPPERDI	0
Bit 2	R/W	PAISPERDI	0
Bit 1	R/W	LOPCONPERDI	0
Bit 0	R/W	PAISCONPERDI	0

This register along with Path Enhanced RDI Control #2 register controls the auto assertion of path enhanced RDI (G1 bits 5, 6, 7) in the local TPOP or a mate TPOP (via the RAD PRDI5, PRDI6 and PRDI7 bit positions) of the corresponding TPPS. These register bits should normally be set low when the RPPS is configured as a slave. To fully support enhanced RDI, the RPPS Path REI/RDI Control #1 and #2 register must also be programmed to properly get the Bit 5 for the G1 byte.

PAISCONPERDI

When set high, the PAISCONPERDI bit enables path enhanced RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. PAISCONPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI.

When PAISCONPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI and the associated alarm states.

LOPCONPERDI

When set high, the LOPCONPERDI bit enables path enhanced RDI assertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. LOPCONPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI.

When LOPCONPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI and the associated alarm states.

PAISPERDI

When set high, the PAISPERDI bit enables path enhanced RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. PAISPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI.

When PAISPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI and the associated alarm states.

LOPPERDI

When set high, the LOPPERDI bit enables path enhanced RDI assertion when loss of pointer (LOP) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. LOPPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI.

When LOPPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI and the associated alarm states.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

ALMPERDI

When set high, the ALMPERDI bit enables path enhanced RDI assertion when LOS , LOF (LOF) or AIS (LAIS) events are detected in the receive stream. If enabled, when these events occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set low while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set high. ALMPERDI has precedence over PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI.

When ALMPERDI is set low, reporting of enhanced RDI is according to PSLMPERDI, PSLUPERDI, TIUPERDI, TIMPERDI, and UNEQERDI and the associated alarm states.

PERDI_EN

The PERDI_EN bit enables the automatic insertion of enhanced RDI in the local transmitter or in a mate transmitter via the RAD output. When PERDI_EN is a logic one, auto insertion is enabled using the event enable bits in this register and in the SPECTRA 4x155 Path Enhanced RDI Control #2 register. When PERDI_EN is a logic zero, path enhanced RDI is not automatically inserted in the transmit stream.

Registers 1119H, 1219H, 1319H, 1419H, 1519H, 1619H, 1719H, 1819H, 1919H, 1A19H, 1B19H, and 1C19H: RPPS Path Enhanced RDI Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	UNEQPERDI	0
Bit 5	R/W	PSLUPERDI	0
Bit 4	R/W	PSLMPERDI	0
Bit 3	R/W	Unused	0
Bit 2	R/W	Unused	0
Bit 1	R/W	TIUPERDI	0
Bit 0	R/W	TIMPERDI	0

This register along with Path Enhanced RDI Control #1 register controls the auto assertion of path enhanced RDI (G1 bits 5, 6, 7) in the local TPOP or a mate TPOP (via the RAD PRDI5, PRDI6 and PRDI7 bit positions) of the corresponding TPPS. These register bits should normally be set low when the RPPS is configured as a slave. To fully support enhanced RDI, the RPPS Path REI/RDI Control #1 and #2 register must also be programmed to properly get the Bit 5 for the G1 byte.

TIMPERDI

When set high, the TIMPERDI bit enables path enhanced RDI assertion when path trace identifier (mode 1) mismatch (TIM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIMPERDI is set low, trace identifier (mode 1) mismatch events have no effect on path RDI.

This bit has no effect when PERDI_EN is set low.

TIUPERDI

When set high, the TIUPERDI bit enables path enhanced RDI assertion when path trace identifier (mode 1) unstable (TIU) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When TIUPERDI is set low, trace identifier (mode 1) unstable events have no effect on path RDI.

This bit has no effect when PERDI_EN is set low.

PSLMPERDI

When set high, the PSLMPERDI bit enables path enhanced RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When PSLMPERDI is set low, path signal label mismatch events have no effect on path RDI. This bit has no effect when PERDI_EN is set low.

PSLUPERDI

When set high, the PSLUPERDI bit enables path enhanced RDI assertion when path signal label unstable (PSLU) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When PSLUPERDI is set low, path signal label unstable events have no effect on path RDI. This bit has no effect when PERDI_EN is set low.

UNEQPERDI

When set high, the UNEQPERDI bit enables path enhanced RDI assertion when the path signal label in the receive stream indicates unequipped status. If enabled, when the event occurs, bit 6 of the G1 byte (or the RAD output PRDI6 bit position) is set high while bit 7 of the G1 byte (or the RAD output PRDI7 bit position) is set low.

When UNEQPERDI is set low, path signal label unequipped status has no effect on path enhanced RDI.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

Registers 111CH, 121CH, 131CH, 141CH, 151CH, 161CH, 171CH, 181CH, 191CH, 1A1CH, 1B1CH, and 1C1CH: RPPS RALM Output Control #1

Bit	Type	Function	Default
Bit 7	R/W	LOMRALM	0
Bit 6	R/W	PRDIRALM	0
Bit 5	R/W	PERDIRALM	0
Bit 4	R/W	ALMRALM	0
Bit 3	R/W	LOPRALM	0
Bit 2	R/W	PAISRALM	0
Bit 1	R/W	LOPCONRALM	0
Bit 0	R/W	PAISCONRALM	0

This register along with the RALM Output Control #2 register controls the receive path alarm output (RALM) signal. These register bits should normally be set low when the RPPS is configured as a slave, unless indicated otherwise.

PAISCONRALM

The Path AIS concatenation (PAISCON) RALM output enable has different definitions for master and slave slices.

For a slave slice, the bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

For a master slice, the bit allows the corresponding alarm for the payload to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indications from the slaves are ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication from the slaves does not affect the RALM output.

LOPCONRALM

The loss of pointer concatenation (LOPCON) RALM output enable has different definitions for master and slave slices.

For a slave slice, the bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

For a master slice, the bit allows the corresponding alarm for the payload to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indications from the slaves are ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication from the slaves does not affect the RALM output.

PAISRALM

The path alarm indication signal (PAIS) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

LOPRALM

The LOP RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

PERDIRALM

The path enhanced RDI (PERDI) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

PRDIRALM

The path RDI (PRDI) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

ALMRALM

The LOS, LOF, or LAIS RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

LOMRALM

The LOM RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

Registers 111DH, 121DH, 131DH, 141DH, 151DH, 161DH, 171DH, 181DH, 191DH, 1A1DH, 1B1DH, and 1C1DH: RPPS RALM Output Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	UNEQRALM	0
Bit 5	R/W	PSLURALM	0
Bit 4	R/W	PSLMRALM	0
Bit 3	R/W	Reserved	0
Bit 2	—	Unused	X
Bit 1	R/W	TIURALM	0
Bit 0	R/W	TIMRALM	0

This register along with RALM Output Control #1 register controls the receive path alarm output (RALM) signal. These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

TIMRALM

The path trace identifier mismatch (TIM) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

TIURALM

The path trace identifier (mode 1) unstable (TIU) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

PSLMRALM

The path signal label mismatch (PSLM) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

PSLURALM

The path signal label unstable (PSLU) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

UNEQRALM

The path unequipped (UNEQ) RALM output enable bit allows the corresponding alarm to be ORed into the RALM output. When the enable bit is set high, the corresponding alarm indication is ORed with other alarm indications and output on RALM. When the enable bit is set low, the corresponding alarm indication does not affect the RALM output.

Registers 111EH, 121EH, 131EH, 141EH, 151EH, 161EH, 171EH, 181EH, 191EH, 1A1EH, 1B1EH, and 1C1EH: RPPS Reserved

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved register bit must be set to logic 0 for proper functioning of the SPECTRA 4x155.

Registers 1128H, 1228H, 1328H, 1428H, 1528H, 1628H, 1728H, 1828H, 1928H, 1A28H, 1B28H, and 1C28H: RPPS Path Interrupt Status

Bit	Type	Function	Default
Bit 7	R	DPAIS	X
Bit 6	R	RPOPI	X
Bit 5	R	RTALI	X
Bit 4	R	SPTBI	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	DPGMI	X
Bit 0	—	Unused	X

This register, together with the Section/Line Interrupt Status register, allows the source of an active interrupt for the receive side to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source. These register bits are not cleared on read.

DPGMI

The DPGMI bits are high when an interrupt request is active from the DPGM block.

SPTBI

The SPTBI bit is high when an interrupt request is active from the SPTB block.

RTALI

The RTALI bits is high when an interrupt request is active from the RTAL block.

RPOPI

The RPOPI bit is high when an interrupt request is active from the RPOP block.

DPAIS

The Drop bus alarm indication signal (DPAIS) bit is set high when path AIS is inserted in the Drop bus. Drop bus Path AIS assertion can be automatic using the SPECTRA 4x155 RPPS Path AIS Control #1 and #2 registers or manual using the RTAL Control registers. Note: DPAIS is not an interrupt bit.

Registers 112CH, 122CH, 132CH, 142CH, 152CH, 162CH, 172CH, 182CH, 192CH, 1A2CH, 1B2CH, and 1C2CH: RPPS Auxiliary Path Interrupt Enable #1

Bit	Type	Function	Default
Bit 7	R/W	PRDIE	0
Bit 6	R/W	PAISE	0
Bit 5	R/W	PSLUE	0
Bit 4	R/W	PSLME	0
Bit 3	R/W	LOPE	0
Bit 2	R/W	LOME	0
Bit 1	R/W	TIUE	0
Bit 0	R/W	TIME	0

This register controls the interrupt generation on output INTB by the corresponding interrupt status in the Auxiliary Path Interrupt Status #1 register. Note: These enable bits do not affect the actual interrupt bits found in the RPPS Auxiliary Path Interrupt Status #1 register.

These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

TIME

The path trace identifier (mode 1) mismatch (TIM) interrupt enable bit enables interrupt generation on output INTB by the auxiliary TIM interrupt status.

TIUE

The path trace identifier (mode 1) unstable (TIU) interrupt enable bit enables interrupt generation on output INTB by the auxiliary TIU interrupt status.

LOME

The LOM interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOM interrupt status.

LOPE

The LOP interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOP interrupt status.

PSLME

The path signal label mismatch (PSLM) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PSLM interrupt status.

PSLUE

The path signal label unstable (PSLU) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PSLU interrupt status.

PAISE

The path alarm indication signal (PAIS) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PAIS interrupt status.

PRDIE

The path RDI (PRDI) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PRDI interrupt status.

Registers 112DH, 122DH, 132DH, 142DH, 152DH, 162DH, 172DH, 182DH, 192DH, 1A2DH, 1B2DH, and 1C2DH: RPPS Auxiliary Path Interrupt Enable #2

Bit	Type	Function	Default
Bit 7	R/W	LOPCONE	0
Bit 6	R/W	PAISCONE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	PERDIE	0

This register controls the interrupt generation on output INTB by the corresponding interrupt status in the RPPS Auxiliary Path Interrupt Status #2 register. Note: These enable bits do not affect the actual interrupt status bits found in the RPPS Auxiliary Path Interrupt Status #2 register.

These register bits should normally be set low when the RPPS is configured as a slave unless indicated otherwise.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

PERDIE

The path enhanced RDI (PERDI) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PERDI interrupt status.

TIU2E

The path trace identifier mode 2 unstable (TIU2) interrupt enable bit enables interrupt generation on output INTB by the auxiliary TIU2 interrupt status.

PAISCONE

The path alarm indication signal concatenation (PAISCON) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PAISCON interrupt status.

Note: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

LOPCONE

The loss of pointer concatenation (LOPCON) interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOPCON interrupt status.

Note: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

Registers 1130H, 1230H, 1330H, 1430H, 1530H, 1630H, 1730H, 1830H, 1930H, 1A30H, 1B30H, and 1C30H: RPPS Auxiliary Path Interrupt Status #1

Bit	Type	Function	Default
Bit 7	R/W	PRDII	X
Bit 6	R/W	PAISI	X
Bit 5	R/W	PSLUI	X
Bit 4	R/W	PSLMI	X
Bit 3	R/W	LOPI	X
Bit 2	R/W	LOMI	X
Bit 1	R/W	TIUI	X
Bit 0	R/W	TIMI	X

This register, along with the RPPS Auxiliary Path Interrupt Status #2 register, replicates the path interrupts that can be found in the RPOP and the SPTB registers. However, unlike the RPOP and the SPTB interrupt register bits that clear-on-read, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

TIMI

The path trace identifier mismatch interrupt status bit (TIMI) is set high on changes in the path trace identifier mismatch status.

TIUI

The path trace identifier (mode 1) unstable interrupt status bit (TIUI) is set high on changes in the path trace identifier (mode 1) unstable status (TIU).

LOMI

The loss of multi-frame interrupt status bit (LOMI) is set high on changes in the loss of multi-frame status.

LOPI

The loss of pointer interrupt status bit (LOPI) is set high on the change of loss of pointer status.

PSLMI

The path signal label mismatch interrupt status bit (PSLMI) is set high on changes in the path signal label mismatch status.

PSLUI

The path signal label unstable interrupt status bit (PSLUI) is set high on changes in the path signal label unstable status.

PAISI

The path AIS interrupt status bit (PAISI) is set high on changes in the path AIS status.

PRDII

The path RDI interrupt status bit (PRDII) is set high on changes in the path RDI status.

Registers 1131H, 1231H, 1331H, 1431H, 1531H, 1631H, 1731H, 1831H, 1931H, 1A31H, 1B31H, and 1C31H: RPPS Auxiliary Path Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R/W	LOPCONI	X
Bit 6	R/W	PAISCONI	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	Reserved	X
Bit 3	R/W	Reserved	X
Bit 2	R/W	Reserved	X
Bit 1	R/W	Reserved	X
Bit 0	R/W	PERDII	X

This register, along with the RPPS Auxiliary Path Interrupt Status #1 register, replicates the path interrupts that can be found in the RPOP and the SPTB registers. However, unlike the RPOP and the SPTB interrupt register bits that clear-on-reads, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

PERDII

The path enhanced RDI interrupt (PERDII) bits are set high when the RPOP detects a change in the path enhanced remote defect state.

TIU2I

The path trace identifier unstable mode 2 interrupt status bit (TIU2I) is set high on changes in the path trace identifier unstable status for mode 2 operation.

PAISCONI

The path AIS concatenation interrupt (PAISCONI) bit is set high when there is a change of the path AIS concatenation state. This auxiliary interrupt status corresponds to the AU-3PAISCONI status in the RPOP Alarm Interrupt Status register.

LOPCONI

The loss of pointer concatenation interrupt (LOPCONI) bit is set high when there is a change of the pointer concatenation state. This auxiliary interrupt status corresponds to the AU-3LOPCONI status in the RPOP Alarm Interrupt Status register.

Registers 1134H, 1234H, 1334H, 1434H, 1534H, 1634H, 1734H, 1834H, 1934H, 1A34H, 1B34H, and 1C34H: RPPS Auxiliary Path Status

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R	ERDIV[0]	X

ERDIV[2:0]

The ERDIV[2:0] bits reflect the current filtered value of the enhanced RDI codepoint (G1 bits 5, 6, and 7) for the receive SONET/SDH stream.

Filtering is controlled using the RDI10 bit in the RPOP, Pointer MSB register. This register reflects the same ERDIV[2:0] value that can be found in the RPOP, Status and Control (EXTD=1) register. This register can be used for interrupt handling if it is undesirable to use the EXTD feature.

Registers 1140H, 1240H, 1340H, 1440H, 1540H, 1640H, 1740H, 1840H, 1940H, 1A40H, 1B40H, and 1C40H: RPOP Status and Control (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	AU-3LOPCONV	X
Bit 5	R	LOPV	X
Bit 4	R	AU-3PAISCONV	X
Bit 3	R	PAISV	X
Bit 2	R	PRDIV	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

This register provides configuration and reports the status of the corresponding RPOP if the EXTD bit is set low in the RPOP Pointer MSB register.

NEWPTRE

When a logic one is written to the NEWPTRE interrupt enable bit position, the reception of a new_point indication will activate the interrupt (INT) output.

NEWPTRI

The NEWPTRI bit is set to logic one when a new_point indication is received. This bit (and the interrupt) is cleared when this register is read.

PRDIV

The path RDI status bit (PRDI) indicates reception of path RDI alarm in the receive stream.

PAISV

The path AIS status bit (PAISV) indicates reception of path AIS alarm in the receive stream.

AU-3PAISCONV

The AU-3 concatenation path AIS status bit (AU-3PAISCONV) indicates reception of path AIS alarm in the concatenation indication in the receive STS-1 (STM-0/AU-3) or equivalent stream.

LOPV

The loss of pointer status bit (LOPV) indicates entry to the LOP_state in the RPOP pointer interpreter state machine.

AU-3LOPCONV

The AU-3 concatenated loss of pointer status bit (AU-3LOPCONV) indicates entry to LOPCON_state for the receive STS-1 (STM-0/AU-3) or equivalent stream in the RPOP pointer interpreter.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

Registers 1140H, 1240H, 1340H, 1440H, 1540H, 1640H, 1740H, 1840H, 1940H, 1A40H, 1B40H, and 1C40H: RPOP Status and Control (EXTD=1)

Bit	Type	Function	Default
Bit 7	R/W	TCDLT	0
Bit 6	R/W	IINVCNT	0
Bit 5	R/W	PSL5	0
Bit 4	R/W	Reserved	0
Bit 3	—	Reserved	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R	ERDIV[0]	X

This register provides configuration and reports the status of the corresponding RPOP if the EXTD bit is set high in the RPOP Pointer MSB register.

ERDIV[2:0]

The ERDIV[2:0] bits reflect the current state of the detected enhanced RDI, (filtered G1 bits 5, 6, and 7).

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

PSL5

The PSL5 bit controls the filtering of the path signal label (PSL) byte (C2). When a logic one is written to PSL5, the PSL is updated when the same value is received for five consecutive frames. When a logic zero is written to PSL5, the PSL is updated when the same value is received for three consecutive frames.

IINVCNT

When a logic one is written to the IINVCNT (Intuitive Invalid Pointer Counter) bit, if in the LOP state, 3 x new point will reset the inv_point count. If this bit is set to logic zero, the inv_point count will not be reset if in the LOP state and 3 x new pointers are detected.

TCDLT

When a logic one is written to the TCDLT (Tandem Connection Data Link Transparent) bit, the data link field of the Z5 byte will be passed transparently if no data is inserted via the tandem connection overhead data signal (RTCOH). If this bit is set to logic zero, all-ones will be inserted into the data link field of the Z5 byte, provided no data is inserted via the tandem connection overhead data signal (RTCOH).

Registers 1141H, 1241H, 1341H, 1441H, 1541H, 1641H, 1741H, 1841H, 1941H, 1A41H, 1B41H, and 1C41H: RPOP Alarm Interrupt Status (EXTD=0)

Bit	Type	Function	Default
Bit 7	R	PSLI	X
Bit 6	R	AU-3LOPCONI	X
Bit 5	R	LOPI	X
Bit 4	R	AU-3PAISCONI	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	PREII	X

This register allows identification and acknowledgment of path level alarm and error event interrupts when the EXTD bit is set low in the RPOP Pointer MSB register. These bits (and the interrupt) are cleared when this register is read.

PREII

The PREI interrupt status bit (PREII) is set high when a path REI is detected.

BIPEI

The BIP error interrupt status bit (BIPEI) is set high when a path BIP-8 error is detected.

PRDII

The PRDII interrupt status bit is set high on assertion and removal of the corresponding path RDI status.

PAISI

The PAISI interrupt status bit is set high on assertion and removal of the corresponding path alarm indication signal status.

AU-3PAISCONI

The AU-3PAISCONI interrupt status bit is set high on assertion and removal of the corresponding AU-3 path alarm indication signal concatenation status.

LOPI

The LOPI interrupt status bit is set high on assertion and removal of the corresponding loss of pointer status.

AU-3LOPCONI

The AU-3LOPCONI interrupt status bit is set high on assertion and removal of the corresponding AU-3 loss of pointer concatenation status.

PSLI

The PSLI bit is set to logic one when a change is detected in the path signal label register. The current path signal label can be read from the Path Signal Label register.

Registers 1141H, 1241H, 1341H, 1441H, 1541H, 1641H, 1741H, 1841H, 1941H, 1A41H, 1B41H, and 1C41H: RPOP Alarm Interrupt Status (EXTD=1)

Bit	Type	Function	Default
Bit 7	—	Unused	—
Bit 6	—	Unused	—
Bit 5	—	Unused	—
Bit 4	—	Unused	—
Bit 3	—	Unused	—
Bit 2	—	Unused	—
Bit 1	—	Unused	—
Bit 0	R	ERDII	X

This register allows identification and acknowledgment of path level alarm and error event interrupts when the EXTD bit is set high in the RPOP Pointer MSB register. These bits (and the interrupt) are cleared when the Interrupt Status Register is read.

ERDII

The ERDII bit is set to logic one when a change is detected in the received enhanced RDI state.

Registers 1142H, 1242H, 1342H, 1442H, 1542H, 1642H, 1742H, 1842H, 1942H, 1A42H, 1B42H, and 1C42H: RPOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6	R	CONCATI	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	ILLPTRI	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts. These bits (and the interrupt) are cleared when this register is read. Please refer to the pointer interpreter state diagram and notes in the Function Description of the RPOP for alarm definitions.

NDFI

The NDF enabled indication interrupt status bit (NDFI) is set high when one of the NDF enable patterns is observed in the receive stream.

PSEI, NSEI

The positive and negative justification event interrupt status bits (PSEI, NSEI) are set high when the RPOP block responds to an inc_ind or dec_ind indication, respectively, in the receive stream.

ILLPTRI

The illegal pointer interrupt status bit (ILLPTRI) is set high when an illegal pointer observed on the receive stream.

INVNDFI

The invalid NDF interrupt status bit (NDFI) is set high when an invalid NDF code is observed on the receive stream.

DISCOPAI

The discontinuous pointer change interrupt status bit (DISCOPAI) is set high when the RPOP active offset is changed due to receiving the same valid pointer for three consecutive frames (3 x eq_new_point indication).

ILLJREQI

The illegal justification request interrupt status bit (ILLJREQI) is set high when the RPOP detects a positive or negative pointer justification request (inc_req, dec_req) that occurs within three frames of a previous justification event (inc_ind, dec_ind) or an active offset change due to an NDF enable indication (NDF_enable).

CONCATI

The concatenation indication error interrupt status bit (CONCATI) is set high when the H1, H2 bytes do not match the concatenation indication ('b1001xx1111111111).

This interrupt bit should be ignored for a master slice.

Registers 1143H, 1243H, 1343H, 1443H, 1543H, 1643H, 1743H, 1843H, 1943H, 1A43H, 1B43H, and 1C43H: RPOP Alarm Interrupt Enable (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	PSLE	0
Bit 6	R/W	AU-3LOPCONE	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	AU-3PAISCONE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	PREIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set low in the RPOP Pointer MSB register.

PREIE

When a logic one is written to the PREIE interrupt enable bit position, the reception of one or more path REIs will activate the interrupt (INTB) output.

BIPEE

When a logic one is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt (INTB) output.

PRDIE

When a logic one is written to the PRDIE interrupt enable bit position, a change in the path RDI state will activate the interrupt (INTB) output.

PAISE

When a logic one is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt (INTB) output.

AU-3PAISCONE

When a logic one is written to the AU-3PAISCONE interrupt enable bit position, a change in the AU-3 concatenation path AIS state will activate the interrupt (INTB) output.

LOPE

When a logic one is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt (INTB) output.

AU-3LOPCONE

When a logic one is written to the AU-3LOPCONE interrupt enable bit position, a change in the AU-3 concatenation LOP state will activate the interrupt (INTB) output.

PSLE

When a logic one is written to the PSLE interrupt enable bit position, a change in the path signal label will activate the interrupt (INT) output.

Registers 1143H, 1243H, 1343H, 1443H, 1543H, 1643H, 1743H, 1843H, 1943H, 1A43H, 1B43H, and 1C43H: RPOP Alarm Interrupt Enable and Concat Pointer Status (EXTD=1)

Bit	Type	Function	Default
Bit 7	R	LOPCONV	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	PAISCONV	X
Bit 3	—	Reserved	X
Bit 2	—	Reserved	X
Bit 1	—	Reserved	X
Bit 0	R/W	ERDIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set high in the RPOP Pointer MSB register.

ERDIE

When a logic one is written to the RDIE interrupt enable bit position, a change in the path enhanced RDI state will activate the interrupt (INT) output.

Reserved

The Reserved bits are status bits and must be ignored when this register is read.

LOPCONV

The concatenated loss of pointer value bit (LOPCONV) indicates the loss of concatenated pointer status for the STS-1 (STM-1/AU-3) equivalent stream of the STS-3c (STM1/AU4) being processed in the slave slice.

PAISCONV

The concatenated path alarm indication bit (PAISCONV) indicates the presence of all-ones instead of the concatenation indicator in the payload pointer bytes. The pointer bytes refers to the H1/H2 bytes of the STS-1 (STM-1/AU-3) equivalent stream of the STS-3c (STM1/AU4) being processed in the slave slice.

Registers 1144H, 1244H, 1344H, 1444H, 1544H, 1644H, 1744H, 1844H, 1944H, 1A44H, 1B44H, and 1C44H: RPOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	CONCATE	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	ILLPTRE	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register allows interrupt generation to be enabled or disabled for pointer events.

NDFE

When a logic one is written to the NDFE interrupt enable bit position, the detection of an NDF_enable indication will activate the interrupt (INTB) output.

PSEE

When a logic one is written to the PSEE interrupt enable bit position, a positive pointer adjustment event will activate the interrupt (INTB) output.

NSEE

When a logic one is written to the NSEE interrupt enable bit position, a negative pointer adjustment event will activate the interrupt (INTB) output.

ILLPTRE

When a logic one is written to the ILLPTRE interrupt enable bit position, an illegal pointer will activate the interrupt (INT) output.

INVNDFE

When a logic one is written to the INVNDFE interrupt enable bit position, an invalid NDF code will activate the interrupt (INTB) output.

DISCOPAE

When a logic one is written to the DISCOPAE interrupt enable bit position, a change of pointer alignment event will activate the interrupt (INTB) output.

CONCATE

When a logic one is written to the CONCATE interrupt enable bit position, an invalid Concatenation Indicator event will activate the interrupt (INTB) output.

ILLJREQE

When a logic one is written to the ILLJREQE interrupt enable bit position, an illegal pointer justification request will activate the interrupt (INTB) output.

Registers 1145H, 1245H, 1345H, 1445H, 1545H, 1645H, 1745H, 1845H, 1945H, 1A45H, 1B45H, and 1C45H: RPOP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

The register reports the lower eight bits of the active offset.

PTR[7:0]

The PTR[7:0] bits contain the eight LSBs of the active offset value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not change during the register read.

Registers 1146H, 1246H, 1346H, 1446H, 1546H, 1646H, 1746H, 1846H, 1946H, 1A46H, 1B46H, and 1C46H: RPOP Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDFPOR	0
Bit 6	R/W	EXTD	0
Bit 5	R/W	RDI10	0
Bit 4	R	CONCAT	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

This register reports the upper two bits of the active offset, the SS bits in the receive pointer.

PTR[9:8]

The PTR[9:8] bits contain the two MSBs of the current pointer value as derived from the H1 and H2 bytes. Thus, to ensure reading a valid pointer, the NDFI, NSEI, and PSEI bits of the Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced.

CONCAT

The CONCAT bit is set high if the H1, H2 pointer byte received matches the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

RDI10

The RDI10 bit controls the filtering of the RDI, the auxiliary RDI and the enhanced RDI. When RDI10 is set high, the RDI and ERDI status is updated when the same value is received in the corresponding bit/bits of the G1 byte for 10 consecutive frames. When RDI10 is set low, the RDI and ERDI status is updated when the same value is received for five consecutive frames.

EXTD

The EXTD bit extends the RPOP registers to facilitate Additional mapping. If this bit is set to logic one the register mapping, for the RPOP Status and Control register, the RPOP Alarm Interrupt Status register and the RPOP Alarm Interrupt Enable registers are extended.

NDFPOR

The NDFPOR (new data flag pointer of range) bit controls the definition of the NDF_enable indication for entry to the LOP state under 8xNDF_enable events. When NDFPOR is set high, for the purposes of detect of loss of events only, the definition of the NDF_enable indication does not require the pointer value to be within the range of 0 to 782. When NDFPOR is set low, NDF_enable indications require the pointer to be within 0 to 782.

Registers 1147H, 1247H, 1347H, 1447H, 1547H, 1647H, 1747H, 1847H, 1947H, 1A47H, 1B47H, and 1C47H: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

This register reports the path label byte in the receive stream..

PSL[7:0]

The PSL[7:0] bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three or five consecutive frames as selected using the PSL5 bit in the RPOP Status and Control (EXTD=1) register.

Registers 1148H, 1248H, 1348H, 1448H, 1548H, 1648H, 1748H, 1848H, 1948H, 1A48H, 1B48H, and 1C48H: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	BE[7]	X
Bit 6	R	BE[6]	X
Bit 5	R	BE[5]	X
Bit 4	R	BE[4]	X
Bit 3	R	BE[3]	X
Bit 2	R	BE[2]	X
Bit 1	R	BE[1]	X
Bit 0	R	BE[0]	X

Registers 1149H, 1249H, 1349H, 1449H, 1549H, 1649H, 1749H, 1849H, 1949H, 1A49H, 1B49H, and 1C49H: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	BE[15]	X
Bit 6	R	BE[14]	X
Bit 5	R	BE[13]	X
Bit 4	R	BE[12]	X
Bit 3	R	BE[11]	X
Bit 2	R	BE[10]	X
Bit 1	R	BE[9]	X
Bit 0	R	BE[8]	X

BE[15:0]

Bits BE[15:0] represent the number of path BIP errors that have been detected since the last time the path BIP-8 registers were polled by writing to the SPECTRA 4x155 Reset and Identity register. The write access transfers the internally accumulated error count to the path BIP-8 registers within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Registers 114AH, 124AH, 134AH, 144AH, 154AH, 164AH, 174AH, 184AH, 194AH, 1A4AH, 1B4AH, and 1C4AH: RPOP Path REI LSB

Bit	Type	Function	Default
Bit 7	R	FE[7]	X
Bit 6	R	FE[6]	X
Bit 5	R	FE[5]	X
Bit 4	R	FE[4]	X
Bit 3	R	FE[3]	X
Bit 2	R	FE[2]	X
Bit 1	R	FE[1]	X
Bit 0	R	FE[0]	X

Registers 114BH, 124BH, 134BH, 144BH, 154BH, 164BH, 174BH, 184BH, 194BH, 1A4BH, 1B4BH, and 1C4BH: RPOP Path REI MSB

Bit	Type	Function	Default
Bit 7	R	FE[15]	X
Bit 6	R	FE[14]	X
Bit 5	R	FE[13]	X
Bit 4	R	FE[12]	X
Bit 3	R	FE[11]	X
Bit 2	R	FE[10]	X
Bit 1	R	FE[9]	X
Bit 0	R	FE[8]	X

FE[15:0]

Bits FE[15:0] represent the number of path REIs that have been received since the last time the Path REI registers were polled by writing to the SPECTRA 4x155 Reset and Identity register. The write access transfers the internally accumulated error count to the path REI registers within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Registers 114CH, 124CH, 134CH, 144CH, 154CH, 164CH, 174CH, 184CH, 194CH, 1A4CH, 1B4CH, and 1C4CH: RPOP Tributary Multi-frame Status and Control

Bit	Type	Function	Default
Bit 7	R	LOMI	X
Bit 6	R	LOMV	X
Bit 5	R/W	LOME	0
Bit 4	R/W	BLKREI	0
Bit 3	R	COMAI	X
Bit 2	R/W	COMAE	0
Bit 1	R/W	Reserved	0
Bit 0	R	Reserved	X

This register reports the status of the multi-frame framer and enables interrupts due to framer events.

Reserved

The Reserved bit must be set low for correct operation of the SPECTRA 4x155 device. The Reserved read bits must be ignored when this register is read.

COMAE

The change of multi-frame alignment interrupt enable bit (COMAE) controls the generation of interrupts on when the SPECTRA 4x155 detect a change in the multi-frame phase. When LOME is set high, an interrupt is generated upon change of multi-frame alignment. When COMAE is set low, COMA has no effect on the interrupt output (INTB).

COMAI

The change of multi-frame alignment interrupt status bit (COMAI) is set high on changes in the multi-frame alignment. This bit is cleared (and the interrupt acknowledged) when this register is read.

BLKREI

When set high, the block REI bit (BLKREI) indicates that path REI counts are to be reported and accumulated on a block basis. A single REI error is accumulated if the received REI code is between one and eight inclusive. When BLKREI is set low, REI errors are accumulated literally.

LOME

The loss of multi-frame interrupt enable bit (LOME) controls the generation of interrupts on declaration and removal of loss of multi-frame indication (LOM). When LOME is set high, an interrupt is generated upon loss of multi-frame. When LOME is set low, LOM has no effect on the interrupt output (INTB).

LOMV

The loss of multi-frame status bit (LOMV) reports the current state of the multi-frame framer monitoring the receive stream. LOMV is set high when loss of multi-frame is declared and is set low when multi-frame alignment has been acquired.

LOMI

The loss of multi-frame interrupt status bit (LOMI) is set high on changes in the loss of multi-frame status. This bit is cleared (and the interrupt acknowledged) when this register is read.

Registers 114DH, 124DH, 134DH, 144DH, 154DH, 164DH, 174DH, 184DH, 194DH, 1A4DH, 1B4DH, and 1C4DH: RPOP Ring Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	DISFS	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	RTC_EN	0

This register contains ring control bits.

Reserved

Reserved register bits must be set low for proper functioning of the SPECTRA 4x155.

RTC_EN

When set high, the RTC_EN bit configures enables the functioning of the RTCEN and RTCOH ports. The RTCEN and RTCOH ports can be used to insert the Z5 path overhead growth byte onto the Drop bus.

BLKBIPO

When set high, the block BIP-8 output bit (BLKBIPO) indicates that path BIP-8 errors are to be reported (on RAD and B3E) on a block basis. A single BIP error is reported to the return transmit path overhead processor if any of the BIP-8 results indicates a mismatch. When BLKBIPO is set low, BIP-8 errors are reported on a bit basis. In in-band error reporting mode, the REI count of the G1 byte is set on a bit basis.

DISFS

When set high, the DISFS bit controls the BIP-8 calculations to ignore the fixed stuffed columns in an AU-3 carrying a VC-3. When DISFS is set low, BIP-8 calculations include the fixed stuff columns in an STS-1 (STM-0/AU-3) stream. This bit must be set low when the RPPS containing the RPOP is processing an STS-3c (STM-1/AU-4) stream.

BLKBIP

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be reported and accumulated on a block basis. A single BIP error is accumulated and reported to the return transmit path overhead processor if any of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated on a bit basis.

ENSS

The enable size bit (ENSS) controls whether the SS bits in the payload pointer are used to determine offset changes in the pointer interpreter state machine. When a logic one is written to this bit, an incorrect SS bit pattern (that is, b'10) will prevent RPOP from issuing NDF_enable, inc_ind and dec_ind indications. When a logic zero is written to this bit, the SS bits received do not affect active offset change events.

SOS

The stuff opportunity spacing control bit (SOS) controls the spacing between consecutive pointer justification events on the receive stream. When a logic one is written to this bit, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred a least three frame ago. When a logic zero is written to this bit, pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Registers 1154H, 1254H, 1354H, 1454H, 1554H, 1654H, 1754H, 1854H, 1954H, 1A54H, 1B54H, and 1C54H: PMON Receive Positive Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	RPJE[7]	X
Bit 6	R	RPJE[6]	X
Bit 5	R	RPJE[5]	X
Bit 4	R	RPJE[4]	X
Bit 3	R	RPJE[3]	X
Bit 2	R	RPJE[2]	X
Bit 1	R	RPJE[1]	X
Bit 0	R	RPJE[0]	X

This register reports the number of positive pointer justification events that occurred on the receive side in the previous accumulation interval. The counter is selectable to accumulate positive pointer justifications in the receive stream when the MONRS bit in the RPPS Path Configuration register is set high, and to accumulate justifications on the Drop bus when MONRS is set low.

RPJE[7:0]

Bits RPJE[7:0] represent the number of positive pointer justification events observed on the receive side since the RPJE register was last updated. An update transfers the internal counter to the register. A transfer may be initiated by writing to the SPECTRA 4x155 Identity and Reset register, or writing to the Channel Reset, Identity and Accumulation Trigger register or writing to any of the PMON counter registers. The write access transfers the internally accumulated error count to the RPJE register within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Registers 1155H, 1255H, 1355H, 1455H, 1555H, 1655H, 1755H, 1855H, 1955H, 1A55H, 1B55H, and 1C55H: PMON Receive Negative Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	RNJE[7]	X
Bit 6	R	RNJE[6]	X
Bit 5	R	RNJE[5]	X
Bit 4	R	RNJE[4]	X
Bit 3	R	RNJE[3]	X
Bit 2	R	RNJE[2]	X
Bit 1	R	RNJE[1]	X
Bit 0	R	RNJE[0]	X

This register reports the number of negative pointer justification events that occurred on the receive side in the previous accumulation interval. The counter is selectable to accumulate negative pointer justifications in the receive stream when the MONRS bit in the RPPS Path Configuration register is set high, and to accumulate justifications on the Drop bus when MONRS is set low.

RNJE[7:0]

Bits RNJE[7:0] represent the number of negative pointer justification events observed on the receive side since the RNJE register was last updated. An update transfers the internal counter to the register. A transfer may be initiated by writing to the SPECTRA 4x155 Identity and Reset register, writing to the Channel Reset, Identity and Accumulation Trigger register or writing to any of the PMON counter registers. The write access transfers the internally accumulated error count to the RNJE register within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Registers 1156H, 1256H, 1356H, 1456H, 1556H, 1656H, 1756H, 1856H, 1956H, 1A56H, 1B56H, and 1C56H: PMON Transmit Positive Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	TPJE [7]	X
Bit 6	R	TPJE [6]	X
Bit 5	R	TPJE [5]	X
Bit 4	R	TPJE [4]	X
Bit 3	R	TPJE [3]	X
Bit 2	R	TPJE [2]	X
Bit 1	R	TPJE [1]	X
Bit 0	R	TPJE [0]	X

This register reports the number of positive pointer justification events that occurred on the corresponding transmit stream in the previous accumulation interval.

TPJE[7:0]

Bits TPJE[7:0] represent the number of positive pointer justification events observed on the receive side since the TPJE register was last updated. An update transfers the internal counter to the register. A transfer may be initiated by writing to the SPECTRA 4x155 Identity and Reset register, writing to the Channel Reset, Identity and Accumulation Trigger register or writing to any of the PMON counter registers. The write access transfers the internally accumulated error count to the TPJE register within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Registers 1157H, 1257H, 1357H, 1457H, 1557H, 1657H, 1757H, 1857H, 1957H, 1A57H, 1B57H, and 1C57H: PMON Transmit Negative Pointer Justification Count

Bit	Type	Function	Default
Bit 7	R	TNJE [7]	X
Bit 6	R	TNJE [6]	X
Bit 5	R	TNJE [5]	X
Bit 4	R	TNJE [4]	X
Bit 3	R	TNJE [3]	X
Bit 2	R	TNJE [2]	X
Bit 1	R	TNJE [1]	X
Bit 0	R	TNJE [0]	X

This register reports the number of negative pointer justification events that occurred on the corresponding transmit stream in the previous accumulation interval.

TNJE[7:0]

Bits TNJE[7:0] represent the number of negative pointer justification events observed on the receive side since the TNJE register was last updated. An update transfers the internal counter to the register. A transfer may be initiated by writing to the SPECTRA 4x155 Identity and Reset register, writing to the Channel Reset, Identity and Accumulation Trigger register or writing to any of the PMON counter registers. The write access transfers the internally accumulated error count to the TNJE register within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Registers 1158H, 1258H, 1358H, 1458H, 1558H, 1658H, 1758H, 1858H, 1958H, 1A58H, 1B58H, and 1C58H: RTAL Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	H4BYP	0
Bit 5	R/W	CLRFS	0
Bit 4	R/W	SSS	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	DPJEE	0
Bit 0	R/W	IPAIS	0

This register allows the operation of the Receive TelecomBus Aligner to be configured.

IPAIS

The insert path alarm indication signal (IPAIS) bit controls the insertion of PAIS in the Drop bus. When IPAIS is set high, path AIS is inserted in the Drop bus. The pointer bytes (H1, H2 and H3) and the entire SPE (VC) are set to all-ones. Normal operation resumes when the IPAIS bit is set low.

If IPAIS is set a master slice, the slave slices in the same channel will also force their SPE to all-ones generating proper STS-3c/STM-1(AU4) path AIS.

DPJEE

The Drop bus pointer justification event interrupt enable bit (DPJEE) controls the activation of the interrupt output when a pointer justification is inserted in the Drop bus. When DPJEE is set high, insertion of pointer justification events in the Drop bus will activate the interrupt (INTB) output. When DPJEE is set low, insertion of pointer justification events in the Drop bus will not affect INTB.

ESEE

The elastic store error interrupt enable bit (ESEE) controls the activation of the interrupt output when a FIFO underflow or overflow has been detected in the elastic store. When ESEE is set high, FIFO flow error events affect the interrupt (INTB) output. When ESEE is set low, FIFO flow error events will not affect INTB.

Reserved

The Reserved bit must be set low for correct operation of the SPECTRA 4x155.

SSS

The set ss bit (SSS) controls the value of the ss field in the H1 pointer byte in the Drop bus. When SSS is set high, the ss bits are set to 'b10. When SSS is set low, the ss bits are set to 'b00.

CLRFS

The clear fixed stuff column bit (CLRFS) enables the setting of the fixed stuff columns in virtual tributary (low order tributary) mappings to zero. When a logic one is written to CLRFS, the fixed stuff column data are set to 00H. When a logic zero is written to CLRFS, the fixed stuff column data from the receive stream is placed on the Drop bus unchanged. The location of the fixed stuff columns in the SPE (VC) is dependent on the whether the RPPS containing the RTAL is processing concatenated payload.

H4BYP

The tributary multi-frame bypass bit (H4BYP) controls whether the RTAL block overwrites the H4 byte in the path overhead with an internally generated sequence. When H4BYP is set high, the H4 byte carried in the receive stream is placed on the Drop bus unchanged. When H4BYP is set low, the H4 byte is replaced by the sequence 'hFC, 'hFD, 'hFE and 'hFF. The phase of the four frames in the multi-frame is synchronized by the multi-frame framer in the RPOP block.

Registers 1159H, 1259H, 1359H, 1459H, 1559H, 1659H, 1759H, 1859H, 1959H, 1A59H, 1B59H, and 1C59H: RTAL Interrupt Status and Control

Bit	Type	Function	Default
Bit 7	R/W	DOPJ[1]	0
Bit 6	R/W	DOPJ[0]	0
Bit 5	R/W	ESD[1]	1
Bit 4	R/W	ESD[0]	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	DLOP	0

This register allows the control of the Drop bus interface and the checking of the interrupt status.

DLOP

The diagnose loss of pointer control bit (DLOP) allows downstream pointer processing elements to be diagnosed. When DLOP is set high, the new data flag (NDF) field of the payload pointer inserted in the Drop bus is inverted causing downstream pointer processing elements to enter a LOP state.

NPJI

The Drop bus negative pointer justification interrupt status bit (NPJI) is set high when the RTAL inserts a negative pointer justification event on the Drop bus.

PPJI

The Drop bus positive pointer justification interrupt status bit (PPJI) is set high when the RTAL inserts a positive pointer justification event on the Drop bus.

ESEI

The Drop bus elastic store error interrupt status bit (ESEI) is set high when the FIFO in RTAL underflows or overflows. This will cause the RTAL to reset itself. It can thus loose the J1, and go out of AIS for a short period of time if it was in AIS state.

ESD0- ESD1

The elastic store depth control bits (ESD[1:0]) set elastic store FIFO fill thresholds. I.e., the thresholds for the ES_upperT and ES_lowerT indications. The thresholds for the four ESD[1:0] codes are:

Table 12 Receive ESD[1:0] Codepoints

ESD[1:0]	Hard neg limit	Soft neg limit	Soft pos limit	Hard pos limit
00	4	0	0	4
01	5	1	1	4
10	6	4	4	6
11	7	6	6	7

Definitions:

Soft neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the soft region of the FIFO (In the soft region, the RTAL generates outgoing negative justifications at the rate of 1 in every 16 frames).

Hard neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the hard region of the FIFO (In the hard region, the RTAL generates outgoing negative justification at the rate of 1 in every 4 frames).

Soft pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the soft region of the FIFO (In the soft region, the RTAL generates outgoing positive justification at the rate of 1 in every 16 frames).

Hard pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the hard region of the FIFO (In the hard region the RTAL will start generates outgoing positive justification at the rate of 1 in every 4 frames).

DOPJ0- DOPJ1

The diagnose pointer justification bits (DOPJ[1:0]) allow downstream pointer processing elements to be diagnosed for correct reaction to pointer justification events using the Drop bus H1 and H2 bytes. Setting DOPJ[1] high and DOPJ[0] low, forces the RTAL to generate positive stuff justification events on the Drop bus at the rate of one every four frames regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to overflow and a set NDF will be inserted in the pointer sequence. Setting DOPJ[1] low and DOPJ[0] high, forces the RTAL to generate negative stuff justification events at the rate of one every four frames, regardless of the current depth of the internal FIFO. Prolonged application may cause the FIFO to underflow and a set NDF will be inserted in the pointer sequence. Setting both DOPJ[1] and DOPJ[0] high disables the RTAL from generating pointer justification events. If the incoming and outgoing clocks have a frequency offset, the internal FIFO may under/overflow depending on the relative frequencies of the clocks. Pointer justification events are generated based on the current depth of the internal FIFO when DOPJ[1] and DOPJ[0] are both set low. When DOPJ[1:0] is set to values other than 'b00, the detection of elastic store over/underflow is disabled.

Using these bit to force justifications will result in an incorrect telecom bus DC1J1V1 signal. Multiple J1 pulses will occur. This register should only be used to test downstream pointer interpreters.

The interrupt bits (and the interrupt) are cleared when this register is read.

Registers 115AH, 125AH, 135AH, 145AH, 155AH, 165AH, 175AH, 185AH, 195AH, 1A5AH, 1B5AH, and 1C5AH: RTAL Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	H4AISB	0
Bit 4	R/W	ITUAIS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	DH4	0

This register reports alarms and controls diagnostics on the Drop bus.

DH4

The diagnose multi-frame indicator enable bit (DH4) controls the inversion of the multi-frame indicator (H4) byte in the Drop bus. This bit may be used to cause an out of multi-frame alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic zero is written to this bit position, the H4 byte is unmodified. When a logic one is written to this bit position, the H4 byte is inverted.

ESAIS

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the Drop bus when a FIFO underflow or overflow has been detected in the elastic store. When ESAIS is set high, detection of FIFO flow error will cause path AIS to be inserted in the Drop bus for three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

Reserved

The Reserved bit must be set low for correct operation of the SPECTRA 4x155.

ITUAIS

The insert tributary path AIS bits controls the insertion of Tributary Path AIS on the Drop bus for VT1.5 (TU11), VT2 (TU12), VT3 and VT6 (TU2) payloads. For the current slice, when ITUAIS is set high, columns in the Drop bus carrying tributary traffic are set to all-ones. The pointer bytes (H1, H2, and H3), the path overhead column, and the fixed stuff columns are unaffected. Normal operation resumes when the ITUAIS bit is set low. The ITUAIS bit is not applicable for TU3 tributary payloads and the ITUAIS bit must be set low. The STM1_CONCAT register bit must be set for TU2, TU11, and TU12 payloads in a VC-4.

H4AISB

The insert H4 AIS bits controls the insertion of the all-ones AIS pattern in the H4 byte. When H4AISB is set low, the H4 byte will be over-written with 'hFF when path AIS is inserted in the Drop bus. When H4AISB is set high, the H4 byte is not over-written during path AIS insertion.

Registers 1160H, 1260H, 1360H, 1460H, 1560H, 1660H, 1760H, 1860H, 1960H, 1A60H, 1B60H, and 1C60H: SPTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	TIMODE	0
Bit 5	R/W	RTIUE	0
Bit 4	R/W	RTIME	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive (for RPPS) and transmit (for corresponding TPPS) portions of the SPTB.

LEN16

The path trace message length bit (LEN16) selects the length of the path trace message to be 16 bytes or 64 bytes. When LEN16 is set high, the path trace message length is 16 bytes. When LEN16 is set low, the path trace message length is 64 bytes.

NOSYNC

The path trace message synchronization disable bit (NOSYNC) disables the writing of the path trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive path trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

TNULL

The transmit null bit (TNULL) controls the insertion of an all-zero path trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer is ignore and all-zeros bytes are provided to the TPOP block. When TNULL is set low the contents of the transmit path trace buffer is sent to TPOP. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5

The receive trace identifier persistence bit (PER5) controls the number of times a path trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIME

The receive path trace identifier (mode 1) mismatch interrupt enable bit (RTIME) controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state from match to mismatch and vice versa. When RTIME is set high, changes in match state activates the interrupt (INTB) output. When RTIME is set low, path trace identifier (mode 1) match/mismatch state changes will not affect INTB. This bit is should be disabled in Trace identifier Mode 2 since the RTIM is generate using the Mode 1 algorithm.

RTIUE

The receive path trace identifier (mode 1) unstable interrupt enable bit (RTIUE) controls the activation of the interrupt output when the receive identifier message state (RTIUV) changes from stable to unstable and vice versa. The State changes are dependent on the Trace Identifier Mode. When RTIUE is set high, changes in the receive path trace identifier unstable (RTIUV) state will activate the interrupt (INTB) output. When RTIUE is set low, path trace identifier unstable state changes will not affect INTB.

TIMODE

The Trace Identifier Mode is used to set the mode for the received path trace identifier. Setting this bit to low sets the Trace Identifier Mode to Mode 1. In this mode the path trace identifier is defined as a regular 16 or 64-byte trace message and persistency is based on the whole message. Receive trace identifier mismatch (RTIM) and unstable (RTIU) alarms are declared on the trace message. Setting this bit to high sets the Trace Identifier Mode to Mode2. In this mode the path trace identifier is defined as a 16-byte message with a single repeating byte that is monitored for persistency and errors. A receive trace identifier unstable (RTIU) alarm is declared when one or more byte errors are detected in three consecutive 16-byte windows. RTIM is not defined in this mode.

ZEROEN

The zero enable bit (ZEROEN) is defined for Trace Identifier Mode 1 only and enables trace identifier mismatch (RTIM) assertion and removal based on an all-zeros path trace message string. When ZEROEN is set high, all-zeros path trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all-zeros path trace message strings are ignored. Trace identifier unstable (RTIU) assertion and removal is not affected by setting this register bit.

Registers 1161H, 1261H, 1361H, 1461H, 1561H, 1661H, 1761H, 1861H, 1961H, 1A61H, 1B61H, and 1C61H: SPTB Path Trace Identifier Status

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R	UNEQI	X
Bit 4	R	UNEQV	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the path trace identifier status of the SPTB.

RTIMV

The receive path trace identifier mismatch status bit (RTIMV) is set high in Trace Identifier Mode 1 when the accepted message differs from the expected message. The accepted message is the last message to have been received five times consecutively. RTIMV is set low when the accepted message is equal to the expected message. If the accepted path trace message string is all-zeros, the mismatch is not declared unless the ZEROEN register bit in the Control register is set. This bit is usually ignored in Trace Identifier Mode 2.

RTIMI

The receive trace identifier mismatch indication status bit (RTIMI) is set high in Trace Identifier Mode 1 when the match/mismatch status (RTIMV) of the trace identifier framer changes state. This bit (and the interrupt) is cleared when this register is read. This bit is usually ignored in Trace Identifier Mode 2.

RTIUV

The receive path trace identifier unstable status bit (RTIUV) is dependent on the Trace Identifier Mode. In Mode 1, the bit is set high when eight trace messages mismatching against their immediate predecessor message have been received without a persistent message being detected. The unstable counter is incremented on each message that mismatches its predecessor and is cleared on the reception of a persistent message (three or five consecutive matching messages). RTIUV is set high when the unstable counter reaches eight. RTIUV is set low and the unstable counter cleared once a persistent message has been received.

In Mode 2, RTIUV is set low during the stable state, which is declared after having received the same 16-byte trace message three consecutive times (stable trace byte for forty-eight consecutive frames). The stable byte is declared the accepted byte. RTIUV is set high when mismatches between the accepted byte and the received byte have been detected in three consecutive 16-byte windows. The 16-byte windows do not overlap and start immediately upon the first detected error.

RTIUI

The receive path trace identifier unstable interrupt status bit is set high when the path trace identifier unstable status (RTIUV) changes state. The setting of this bit is dependent on the unstable status (RTIUV), which is dependent on the Trace Identifier Mode. This bit and the interrupt are cleared when this register is read.

UNEQV

The unequipped status bit (UNEQV) is dependent on the PSL Mode. In Mode 1, this bit is set high when the accepted path signal label indicates that the path connection is unequipped. UNEQV is set low when the accepted path signal label indicates the path connection is not unequipped.

When in PSL Mode 2, the UNEQV is set high upon the reception of five consecutive frames with an unequipped (00h) label. The bit is set low when five consecutive frames are received with a label other than the unequipped label. The five consecutive labels needed to lower the alarm do not need to be the same. The Assertion of UNEQV will automatically deassert the PSLM alarm.

UNEQI

The unequipped indication status bit (UNEQI) is set high when the equipped/unequipped status (UNEQV) of the path connection changes state. The setting of this bit is dependent on the UNEQV status, which is dependent on the PSL Mode. This bit (and the interrupt) is cleared when this register is read.

Registers 1162H, 1262H, 1362H, 1462H, 1562H, 1662H, 1762H, 1862H, 1962H, 1A62H, 1B62H, and 1C62H: SPTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	A[7]	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the Address used to index into path trace identifier buffers. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. If RWB is set high, a read access is initiated. The data read can be found in the SPTB Indirect Data register. If RWB is set low, a write access is initiated. The data in the SPTB Indirect Data register will be written to the Address specified.

A[7:0]

The indirect read Address bits (A[7:0]) indexes into the path trace identifier buffers. Addresses 0 to 63 reference the transmit message buffer that contains the identifier message to be inserted into the J1 byte of the transmit stream. Addresses 64 to 127 reference the receive accepted message page. A receive message is accepted into this page when it is received unchanged three or five times consecutively as determined by the PER5 bit setting. Addresses 128 to 191 reference the receive capture page while Addresses 192 to 255 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message down-loaded from the microprocessor.

A[7:0]	RAM Contents
0-63d	Transmit Trace Message
64-127d	Receive Accepted Trace Message
128-191d	Receive Captured Trace Message
192-255d	Receive Expected Trace Message

Registers 1163H, 1263H, 1363H, 1463H, 1563H, 1663H, 1763H, 1863H, 1963H, 1A63H, 1B63H, and 1C63H: SPTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the path trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Registers 1164H, 1264H, 1364H, 1464H, 1564H, 1664H, 1764H, 1864H, 1964H, 1A64H, 1B64H, and 1C64H: SPTB Expected Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	EX_PSL[7]	0
Bit 6	R/W	EX_PSL[6]	0
Bit 5	R/W	EX_PSL[5]	0
Bit 4	R/W	EX_PSL[4]	0
Bit 3	R/W	EX_PSL[3]	0
Bit 2	R/W	EX_PSL[2]	0
Bit 1	R/W	EX_PSL[1]	0
Bit 0	R/W	EX_PSL[0]	0

This register contains the expected path signal label byte in the receive stream.

EX_PSL[7:0]

The EX_PSL[7:0] bits contain the expected path signal label byte (C2). In PSL Mode 1, EPSL[7:0] is compared with the accepted path signal label extracted from the receive stream. A path signal label mismatch (PSLM) is declared if the accepted PSL differs from the expected PSL. In PSL Mode 2, EPSL[7:0] is compared with the received path signal label extracted from the receive stream. A path signal label mismatch (PSLM) is declared if five consecutively received PSLs (other than 00h) differ from the expected PSL. If enabled, an interrupt is asserted upon declaration and removal of PSLM.

Registers 1165H, 1265H, 1365H, 1465H, 1565H, 1665H, 1765H, 1865H, 1965H, 1A65H, 1B65H, and 1C65H: SPTB Path Signal Label Control and Status

Bit	Type	Function	Default
Bit 7	R/W	RPSLUE	0
Bit 6	R/W	RPSLME	0
Bit 5	R/W	UNEQE	0
Bit 4	R/W	PSLMODE	0
Bit 3	R	RPSLUI	X
Bit 2	R	RPSLUV	X
Bit 1	R	RPSLMI	X
Bit 0	R	RPSLMV	X

This register reports the path signal label status of the SPTB.

RPSLMV

The receive path signal label mismatch status bit (RPSLMV) is dependent on the PSL Mode. In Mode 1, this bit reports the match/mismatch status between the expected and the accepted path signal label. RPSLMV is set high when the accepted PSL differs from the expected PSL written by the microprocessor. PSLMV is set low when the accepted PSL matches the expected PSL. In Mode 2, this bit reports the match/mismatch status between the expected and the received path signal label. RPSLMV is set high when the received PSL differs from the expected PSL written by the microprocessor. PSLMV is set low when the accepted PSL matches the expected PSL.

RPSLMI

The receive path signal label mismatch interrupt status bit (RPSLMI) is set high when the match/mismatch (RPSLMV) status between the accepted and the expected path signal label changes state. The setting of this bit is dependent on the unstable status (RPSLMV), which is dependent on the PSL Mode. This bit (and the interrupt) is cleared when this register is read.

RPSLUV

The receive path signal label unstable status bit (RPSLUV) is independent on the PSL Mode. This bit reports the stable/unstable status of the path signal label in the receive stream. RPSLUV is set high when five labels that differ from its immediate predecessor are received. RPSLUV is set low and the unstable label count is reset when five consecutive identical labels are received.

RPSLUI

The receive path signal label unstable interrupt status bit (RPSLUI) is set high when the stable/unstable (RPSLUV) status of the path signal label changes state. This bit (and the interrupt) is cleared when this register is read.

PSLMODE

The PSL Mode is used to set the mode used for the path signal label alarm algorithms. Setting this bit to low sets the PSL Mode to Mode 1. Setting this bit to high sets the PSL Mode to Mode 2.

UNEQE

The unequipped interrupt enable bit (UNEQE) controls the activation of the interrupt output when the path signal label indicates the path connection has changed state from equipped to unequipped and vice versa. When UNEQE is set high, changes in unequipped state (UNEQI) activates the interrupt (INTB) output. When UNEQE is set low, unequipped state changes will not affect INTB.

RPSLME

The receive path signal label mismatch interrupt enable bit (RPSLME) controls the activation of the interrupt output when the comparison between accepted and the expected path signal label changes state from match to mismatch and vice versa. When RPSLME is set high, changes in match state (RPSLMI) activates the interrupt (INTB) output. When RPSLME is set low, path signal label state changes will not affect INTB.

RPSLUE

The receive path signal label unstable interrupt enable bit (RPSLUE) controls the activation of the interrupt output when the received path signal label changes state from stable to unstable and vice versa. When RPSLUE is set high, changes in stable state (RPSLUI) activates the interrupt (INTB) output. When RPSLUE is set low, path signal label state changes will not affect INTB.

Registers 1166H, 1266H, 1366H, 1466H, 1566H, 1666H, 1766H, 1866H, 1966H, 1A66H, 1B66H, and 1C66H: SPTB Path Trace Operation Trigger

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6	R/W	RWB	0
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	—	Unused	X
Bit 0	—	Unused	X

RWB

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer. The access will be performed when the SPTB indirect address register is written to. If RWB is set high, a read access is initiated. The data read can be found in the SPTB Indirect Data register. If RWB is set low, a write access is initiated. The data in the SPTB Indirect Data register will be written to the address specified.

BUSY

The BUSY bit reports whether a previously initiated indirect read or write to the path trace RAM has been completed. BUSY is set high upon writing to the SSTB Path Trace Indirect Address register, and stays high until the initiated access has completed. At this point, BUSY is set low. This register should be polled to determine when new data is available in the SPTB Indirect Data register. The maximum latency for the BUSY to return low is 10 µs.

Registers 1170H, 1270H, 1370H, 1470H, 1570H, 1670H, 1770H, 1870H, 1970H, 1A70H, 1B70H, and 1C70H: DPGM Generator Control #1

Bit	Type	Function	Default
Bit 7	R/W	GEN_A1A2_EN	0
Bit 6	R/W	GEN_INV_PRBS	0
Bit 5	R/W	GEN_AUTO	0
Bit 4	R/W	GEN_FERR	0
Bit 3	R/W	GEN_SIGE	0
Bit 2	R/W	GEN_FSENB	0
Bit 1	R/W	GEN_REGEN	0
Bit 0	R/W	GEN_EN	0

GEN_EN

The Generator Enable (GEN_EN) bit enables the insertion of a pseudo random bit sequence (PRBS) into the Drop Bus payload. When GEN_EN is set high, the PRBS bytes will overwrite the processed payload data. When GEN_EN is set low, the incoming payload is unaltered. This bit has not effect in Autonomous Input Mode.

GEN_REGEN

The Generator Regenerate (GEN_REGEN) bit can be used to re-initialize the generator LFSR and begin regenerating the pseudo random bit sequence (PRBS) from the known reset state. The LFSR reset state is dependent on the set sequence number. Setting this bit in a master generator will automatically force all slaves to reset at the same time. This bit will clear itself when the operation is complete. Upon a frame realignment on the Drop bus, the Generators must be regenerated.

GEN_FSENB

The Generator Fixed Stuff Enable (GEN_FSENB) bit determines whether the pseudo random bit sequence (PRBS) is inserted into the (STS-1/STM-0) fixed stuff bytes of the processed payload. When set to logic one, the PRBS is not inserted into the fixed stuff bytes and the bytes are output unaltered. When set to logic zero, the PRBS is inserted into the fixed stuff bytes. The fixed stuff columns are columns 30 and 59 of the STS-1 payload.

GEN_FSEN should be disabled when using the generator in master/slave configuration to support de-multiplexed concatenated payloads.

GEN_SIGE

The Generator Signature Interrupt Enable (GEN_SIGE) bit allows an interrupt to be asserted on INT when a signature verification mismatch occurs. When GEN_SIGE is set high, a change in the signature verification state (GEN_SIGV) will trigger an interrupt. When GEN_SIGE is set low, no interrupt will be asserted.

GEN_FERR

The Generator Force Error (GEN_FERR) bit is used to force bit errors in the inserted pseudo random bit sequence (PRBS). When logic one is written to this bit, the MSB of the PRBS byte will be inverted, inducing a single bit error. The register bit will clear itself when the operation is complete. A second forced error must not be attempted for at least 200 ns after this bit has been read back to '0'.

GEN_AUTO

The Generator Autonomous Mode (GEN_AUTO) bit places the Generator in the Autonomous Input Mode. In this mode the payload frame is forced to an active offset of zero. The generated frame will have all-zeros TOH and POH bytes. The H1, H2 pointer bytes are set to indicate an active SPE/VC offset of zero and the payload will be filled with a PRBS. When a logic zero is written to this bit, the active offset is determined by the received stream.

GEN_INV_PRBS

The Generator Invert PRBS (GEN_INV_PRBS) bit is used to invert the calculated PRBS byte before insertion into the payload. Setting this bit to logic one enables the logic inversion of all PRBS bits before insertion into the payload. Setting this bit to logic zero does not invert the generated PRBS.

GEN_A1A2_EN

The Generator Framing A1/A2 Enable (GEN_A1A2_EN) bit enables the insertion of the F6h and 28h bit pattern in the A1 and A2 respective byte positions of the processed stream. Setting to logic one this bit enables the A1 and A2 byte insertion. Setting this bit to logic zero passes through the input A1 and A2 bytes from the FIFO, resulting in zero in these bytes on the Drop Bus. This feature has priority over the all zero A1/A2 generated in Autonomous Input Mode. This feature can be used in any DPGM mode, including disabled mode.

Registers 1171H, 1271H, 1371H, 1471H, 1571H, 1671H, 1771H, 1871H, 1971H, 1A71H, 1B71H, and 1C71H: DPGM Generator Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

GEN_H4_EN

The Generator multi-frame indicator H4 Enable (GEN_H4_EN) bit enables the insertion of the H4 indicator into the H4 byte position of the processed payload. Setting to logic one this bit enables the insertion of a valid H4 byte. The inserted value of H4 is derived from the received stream H4 byte. This feature is duplicated in the RTAL block. By default RTAL should be used to insert H4.

Registers 1172H, 1272H, 1372H, 1472H, 1572H, 1672H, 1772H, 1872H, 1972H, 1A72H, 1B72H, and 1C72H: DPGM Generator Concatenate Control

Bit	Type	Function	Default
Bit 7	—	Unused	0
Bit 6	—	Unused	0
Bit 5	R/W	GEN_SEQ[3]	1
Bit 4	R/W	GEN_SEQ[2]	1
Bit 3	R/W	GEN_SEQ[1]	1
Bit 2	R/W	GEN_SEQ[0]	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	GEN_GMODE	0

GEN_GMODE

The GEN_GMODE bits control the operational mode of the pseudo random sequence generator as summarized in the table below. When GEN_GMODE is set to 0, the generator will generate the complete sequence for an STS-1 (STM-0/AU-3) stream. When GEN_GMODE is set to logic one, the generator will generate one third or one in three bytes of the complete sequence for an STS-1 (STM-0/AU-3) equivalent in an STS-3c (STM-1/AU-4) stream.

GEN_GMODE	Generator Gap Mode Description
0	1in1 Gap Mode. Generator inserts the complete PRBS.
1	1in3 Gap Mode. Generator generates 1 of 3 (1in3) PRBS bytes. The generator will also generate 1in2 bytes to skip over path overhead columns.

GEN_SEQ[3:0]

The Generator Sequence (GEN_SEQ[3:0]) sets the reset state of the LFSR and places the generator in the master or slave mode. The sequence number identifies the multiplexing order of the outgoing data into the concatenating stream. The sequence number also affects the signature bit calculation.

GEN_SEQ [3:0]	Mode	Signature bit	Reset Value
0000	Master	96^{th} PRBS bit from current state. MSB of 12^{th} PRBS byte.	All-ones.
0001	Slave1	88^{th} PRBS bit from current state. MSB of 11^{th} PRBS byte.	Master+8 states
0010	Slave2	80^{th} PRBS bit from current state. MSB of 10^{th} PRBS byte.	Master+16 states
0011-1110	Reserved	N/A	
1111	Master	96^{th} PRBS bit from current state. MSB of 12^{th} PRBS byte.	All-ones.

Registers 1173H, 1273H, 1373H, 1473H, 1573H, 1673H, 1773H, 1873H, 1973H, 1A73H, 1B73H, and 1C73H: DPGM Generator Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	GEN_SIGI	X
Bit 0	R	GEN_SIGV	X

GEN_SIGV

The Generator Signature Status (GEN_SIGV) bit indicates if the partial pseudo random sequence (PRBS) begin generated is correctly aligned with the partial PRBS begin generated in the master generator. When GEN_SIGV is low, the signature verification is a match, and the partial PRBS is aligned with that of the master. When GEN_SIGV is high, the signature verification is a mismatch, and the partial PRBS is not aligned with that of the master.

If non-alignment persists, a forced re-start of the sequence generation by all generators processing the concatenated stream should be initiated using the GEN_REGEN register bit in the master generator. This bit is only valid in slave generators and when out of alignment may toggle high and low. Persistent reads at low or reading the interrupt at low assures that the signature is correct.

GEN_SIGI

The Generator Signature Interrupt Status (GEN_SIGI) bit indicates a change in the signature verification state (GEN_SIGV) by a slave generator. When GEN_SIGI is set high, the slave generator has either transition from the signature match state to the signature mismatch state or vice versa. This bit is cleared when this register is read. This bit will continuously be set when in the out of alignment state since the status GEN_SIGV will toggle. This bit is only valid in slave generators.

Registers 1178H, 1278H, 1378H, 1478H, 1578H, 1678H, 1778H, 1878H, 1978H, 1A78H, 1B78H, and 1C78H: DPGM Monitor Control #1

Bit	Type	Function	Default
Bit 7	R/W	MON_AUTORESYNC	1
Bit 6	R/W	MON_INV_PRBS	0
Bit 5	R/W	MON_SYNCE	X
Bit 4	R/W	MON_ERRE	0
Bit 3	R/W	MON_FSENB	0
Bit 2	R/W	MON_SIGE	0
Bit 1	R/W	MON_RESYNC	0
Bit 0	R/W	MON_EN	0

MON_EN

The Monitor Enable (MON_EN) bit enables the monitoring of a pseudo random bit sequence (PRBS) in the processed payload. When MON_EN is set high, the incoming payload is extracted and the data monitored for the PRBS. When MON_EN is set low, no monitoring on the data is done.

MON_RESYNC

The Monitor Resynchronize (MON_RESYNC) bit allows a forced resynchronization of the monitor to the incoming pseudo random bit sequence (PRBS). When set to logic one, the monitor's will go out of synchronization and begin re-synchronizing the to the incoming PRBS payload. Setting this bit in a master monitor will automatically force all slaves to re-synchronize at the same time. This register bit will clear itself when the re-synchronizing has been triggered.

MON_FSENB

The Monitor Fixed Stuff Enable (MON_FSENB) bit determines whether a PRBS is monitored for in the fixed stuff columns (columns 30 and 59) of the processed payload. When logic one is written to this bit, the PRBS is not monitored for in the fixed stuff columns. When a logic zero is written to this bit, the PRBS is monitored for in the fixed stuff columns. MON_FSENB should be disabled when using the monitor in master/slave configuration to support de-multiplexed concatenated payloads.

MON_SIGE

The Monitor Signature Interrupt Enable (MON_SIGE) bit allows an interrupt to be asserted on INT when a signature verification mismatch occurs. When MON_SIGE is set high, a change in the signature verification state (MON_SIGV) will trigger an interrupt. When MON_SIGE is set low, no interrupt is reported. Note: This bit is ignored in a master DPGM.

MON_ERRE

The Monitor Byte Error Interrupt Enable (MON_ERRE) bit allows an interrupt to be asserted on INT when a PRBS byte error has been detected in the incoming payload. When MON_ERRE is set high, a detected PRBS error in the incoming data will trigger an interrupt. When MON_ERRE is set low, no interrupt is generated.

MON_SYNCE

The Monitor Synchronize Interrupt Enable (MON_ERRE) bit allows an interrupt to be asserted on INT when change in the synchronization state of the monitor occurs. When MON_SYNCE is set high, a change in the synchronization state (MON_SYNCV) will trigger an interrupt. When MON_SYNCE is set low, no interrupt is generated.

MON_INV_PRBS

The Monitor Invert PRBS (MON_INV_PRBS) bit is used to invert the received payload data before monitoring the data for a pseudo random bit sequence (PRBS). When set to logic one, the incoming payload PRBS bits are inverted before being verified against the monitor expected PRBS. When set to logic zero, the incoming payload PRBS is not inverted and verified as is.

MON_AUTORESYNC

The Monitor Automatic Resynchronization (MON_AUTORESYNC) bit enables the automatic resynchronization of the monitor after detecting 16 consecutive PRBS byte errors. Setting this bit to logic one, enables the monitor to automatically fall out of synchronization after 16 consecutive errors. Once out of synchronization, the monitor will attempt to resynchronize to the incoming PRBS and verify the synchronization with 32 consecutive PRBS matches. Setting this bit to logic zero disables the automatic resynchronization

Registers 117AH, 127AH, 137AH, 147AH, 157AH, 167AH, 177AH, 187AH, 197AH, 1A7AH, 1B7AH, and 1C7AH: DPGM Monitor Concatenate Control

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	MON_SEQ[3]	1
Bit 4	R/W	MON_SEQ[2]	1
Bit 3	R/W	MON_SEQ[1]	1
Bit 2	R/W	MON_SEQ[0]	1
Bit 1	R/W	MON_GMODE[1]	1
Bit 0	R/W	MON_GMODE[0]	1

MON_GMODE

The MON_GMODE bit controls the operational mode of the pseudo random sequence monitor as summarized in the table below. When MON_GMODE[1:0] is set to "00", the monitor expects the complete sequence for an STS-1 (STM-0/AU-3) stream. When MON_GMODE[1:0] is set to "01", the monitor expects one third or 1 in 3 bytes of the complete sequence in an STS-1 (STM-0/AU-3) equivalent of an STS-3c (STM-1/AU-4) stream.

MON_GMODE [1:0]	Monitor Gap Mode Description
00	1in1 Gap Mode. Monitor monitors for a complete PRBS.
01	1in3 Gap Mode. Monitor will monitor for the presence of every 3rd PRBS byte. The Monitor will also monitor for every 2nd PRBS byte after the POH columns.
10	Reserved
11	Reserved

MON_SEQ[3:0]

The Monitor Sequence (MON_SEQ[3:0]) sets the Monitor in master or slave mode and is used to identify the multiplexed order of the monitored data in the concatenated payload. The sequence order affects the signature bit calculation.

MON_SEQ [3:0]	Mode	Signature bit
0000	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.
0001	Slave1	88th PRBS bit from current state. MSB of 11th PRBS byte.
0010	Slave2	80th PRBS bit from current state. MSB of 10th PRBS byte.
0011-1110	Reserved	
1111	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.

Registers 117BH, 127BH, 137BH, 147BH, 157BH, 167BH, 177BH, 187BH, 197BH, 1A7BH, 1B7BH, and 1C7BH: DPGM Monitor Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	MON_ERRI	X
Bit 3	R	MON_SYNCI	X
Bit 2	R	MON_SYNCV	X
Bit 1	R	MON_SIGI	X
Bit 0	R	MON_SIGV	X

MON_SIGV

The Monitor Signature Status (MON_SIGV) bit indicates if the partial pseudo random sequence (PRBS) begin monitored for is correctly aligned with the partial PRBS begin monitored for by the master generator. When MON_SIGV is low, the signature verification is a match, and the calculated partial PRBS is aligned with that of the master. When MON_SIGV is high, the signature verification is a mismatch, and the calculated partial PRBS is not aligned with that of the master.

If non-alignment persists, a forced re-synchronization of all monitors processing the concatenated stream should be initiated using the MON_RESYNC register bit in the master generator. This bit is only valid in slave generators.

MON_SIGI

The Monitor Signature Interrupt Status (MON_SIGI) bit indicates a change in the signature verification state (MON_SIGV) by a slave monitor. When MON_SIGI is set high, the Monitor has either transition from the signature match state to the signature mismatch state or vice versa. This bit is cleared when this register is read. This bit is only valid in slave monitor.

MON_SYNCV

The Monitor Synchronize Status (MON_SYNCV) is set high when the monitor is out of synchronization. The monitor falls out of synchronization after detecting 16 consecutive mismatched PRBS bytes or being forced to re-synchronize. A forced re-synchronize may be due to setting the MON_RESYNC register bit or a master generator. Once out of synchronization, the Synchronized State can only be achieved after re-synchronizing to the incoming PRBS and verifying the resynchronization with 32 consecutive non-erred PRBS bytes. This bit is set low when in the Synchronized State.

MON_SYNCI

The Monitor Synchronize Interrupt Status (MON_SYNCI) bit indicates a change in the synchronization state (MON_SYNCV) of the monitor. When MON_SYNCI is set high, the monitor has transitioned from the Synchronized to Out-of-Synchronization State or vice versa. This bit is cleared when this register is read.

MON_ERRI

The Monitor Byte Error Interrupt Status (MON_ERRI) bit indicates that an error has been detected in the received PRBS byte while the monitor was in the Synchronized State. MON_ERRI is set high, when one or more PRBS bit errors have been detected in the received PRBS data byte. This bit is cleared when this register is read.

Registers 117CH, 127CH, 137CH, 147CH, 157CH, 167CH, 177CH, 187CH, 197CH, 1A7CH, 1B7CH, and 1C7CH: DPGM Monitor Error Count #1

Bit	Type	Function	Default
Bit 7	R	PRSE[7]	X
Bit 6	R	PRSE[6]	X
Bit 5	R	PRSE[5]	X
Bit 4	R	PRSE[4]	X
Bit 3	R	PRSE[3]	X
Bit 2	R	PRSE[2]	X
Bit 1	R	PRSE[1]	X
Bit 0	R	PRSE[0]	X

Registers 117DH, 127DH, 137DH, 147DH, 157DH, 167DH, 177DH, 187DH, 197DH, 1A7DH, 1B7DH, and 1C7DH: DPGM Monitor Error Count #2

Bit	Type	Function	Default
Bit 7	R	PRSE[15]	X
Bit 6	R	PRSE[14]	X
Bit 5	R	PRSE[13]	X
Bit 4	R	PRSE[12]	X
Bit 3	R	PRSE[11]	X
Bit 2	R	PRSE[10]	X
Bit 1	R	PRSE[9]	X
Bit 0	R	PRSE[8]	X

PRSE[15:0]

The PRSE[15:0] bits represent the number of PRBS byte errors detected since the last accumulation interval. Errors are only accumulated in the synchronized state and each PRBS data byte can only have one error. The transfer of the error accumulation counter to these registers is triggered by a write to either of the GPGM Monitor Error Counters and the contents of these registers will be valid only four clock cycles after the transfer is triggered.

Registers 1180H, 1280H, 1380H, 1480H, 1580H, 1680H, 1780H, 1880H, 1980H, 1A80H, 1B80H, and 1C80H: SPECTRA 4x155 TPPS Configuration

Bit	Type	Function	Default
Bit 7	R/W	MASTER	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	STM1_CONCAT	0
Bit 4	R/W	SLLBEN	0
Bit 3	R	TX_SLICE_ID[3]	X
Bit 2	R	TX_SLICE_ID[2]	X
Bit 1	R	TX_SLICE_ID[1]	X
Bit 0	R	TX_SLICE_ID[0]	X

This register allows the operational mode of the SPECTRA 4x155 TPPS to be configured.

TX_SLICE_ID[3:0]

The TX_SLICE_ID[3:0] bits indicate the TPPS numbers 1 to 12. These register bits exist for test purposes only. The read back values are from zero to eleven, zero being slice 1 and eleven being slice 12.

SLLBEN

When set high, the system side line loop back enable bit (SLLBEN) activates line loop back of the receive STS-1 (STM-0/AU-3) or equivalent stream processed by the corresponding RPPS. The receive stream replaces the transmit STS-1 (STM-0/AU-3) or equivalent stream from the Add bus. When SLLBEN is set low, system side line loop back of the corresponding receive stream is disabled, the data stream from the Add bus is processed normally. STM1_CONCAT

The STM1_CONCAT bit is used to configure the TPPS to be processing TU2, TU11, or TU12 inside an STM-1(VC-4). When configured, TUAIS is properly asserted as defined by the ITUAIS in the TTAL. When set high, the TTAL fixed stuff columns are columns 1, 2, and 3. This supports TU2, TU11, and TU12 payloads in a VC-4. When set low, the TTAL fixed stuff columns are columns 30 and 59. When set low TUAIS can not be inserted properly. This bit can otherwise be set low.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

MASTER

When set high, the MASTER bit enables the TPPS to control and co-ordinate the processing of an STS-1 (STM-0/AU-3) or an STS-3c (STM-1/AU-4) transmit stream as the master. It also enables the TPPS to control and to co-ordinate the distributed PRBS payload sequence generation and monitoring. When the MASTER bit is set low, the TPPS operates in a slave mode and its operation is co-ordinated by the associated master TPPS.

Registers 1182H, 1282H, 1382H, 1482H, 1582H, 1682H, 1782H, 1882H, 1982H, 1A82H, 1B82H, and 1C82H: TPPS Path Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	DISJ1V1	0
Bit 1	R/W	RXSEL[1]	0
Bit 0	R/W	RXSEL[0]	0

This register allows the operational mode of the SPECTRA 4x155 TPPS Path functions to be configured. These register bits should normally be set low when the TPPS is configured as a slave unless indicated otherwise.

RXSEL[1:0]

The RXSEL[1:0] bits controls the source of the associated receive section of the transmit stream. When RXSEL[1:0] is set to 'b00, the receive section is chosen to be one in the local SPECTRA 4x155. The path REI count and path RDI status of the transmit stream is derived from the local RPOP. Local REI's must be enabled by setting the AUTOPREI bit in the RPPS Path REI/RDI Control #1 register.

When RXSEL[1:0] is set to 'b01, a remote receive device (via the TAD port) is chosen and it reports the detected path BIP-8 error count and generated path RDI status to be inserted via the transmit alarm port. The path status byte in the transmit stream carries the path REI and path RDI indications reported in the transmit alarm port (TAD). If the remote receive section is another SPECTRA 4x155, the RAD port can be connected to the TAD port and the AUTOPREI bit in the RPPS Path REI/RDI Control #1 register set so that the detected path BIP-8 error counts can be extracted onto the RAD port. The TAD port can not handle the REI insertion a maximum errored payload rate of eight errors per frame

When RXSEL[1:0] is set to 'b10, in-band error reporting is chosen. The associated receive section forms a new G1 byte reporting on the path BIP-8 errors detected. The SPECTRA 4x155 receive section does not support in-band error reporting of RDI codes. The local transmit section pass the path REI and path RDI bits on the Add bus to the transmit stream unmodified.

When RXSEL[1:0] is set to 'b11, the path status byte in the transmit stream is not associate with any receive stream. Neither path REI nor path RDI will be reported.

Table 13 RXSEL[1:0] Codepoints for STS-1 and STS-3c.

RXSEL[1:0]	Source
00	Local SPECTRA 4x155
01	Remote receive (TAD port)
10	In-band reporting
11	no reporting

DISJ1V1

When set high, the DISJ1V1 bit configures the SPECTRA 4x155 to only expect C1 byte indications on the AC1J1V1 input. When only C1 byte indications are provided, the SPECTRA 4x155 will interpret the pointer of the Add bus to identify the J1 and V1 byte positions. When set low, the SPECTRA 4x155 expects the AC1J1V1 input to indicate C1, J1 and V1.

DISJ1V1 is only valid for TelecomBus operation.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

Registers 1186H, 1286H, 1386H, 1486H, 1586H, 1686H, 1786H, 1886H, 1986H, 1A86H, 1B86H, and 1C86H: TPPS Path Transmit Control

Bit	Type	Function	Default
Bit 7	R/W	ADDUEV	0
Bit 6	R/W	ADDUE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TDIS	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	TPTBEN	0

This register controls the insertion of path overhead and unequipped payload pattern (FFH, 00H) in the transmit stream.

TPTBEN

The TPTBEN bit controls whether the path trace message stored in the TPTB (in SPTB) block is inserted in the transmit stream. When TPTBEN is set high, the message in the corresponding transmit path trace buffer (TPTB) is inserted in the transmit stream. When TPTBEN is set low, the path trace message is supplied by the TPOP block.

Note: This register bit should normally be set low when the TPPS is configured as a slave.

Reserved:

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

TDIS

The TDIS bit controls the insertion of path overhead bytes in the transmit stream. When TDIS is set high, the path overhead bytes of the corresponding transmit stream are sourced from the Add bus. . When TDIS is set low, path overhead is processed normally.

For slave slices, TDIS must be set high.

ADDUE

When set high, the ADDUE bit configures the corresponding transmit stream from the Add bus as unequipped. Payload bytes are overwritten with all-ones or all-zeros as controlled using the ADDUEV bit. When ADDUE is set low, the transmit stream is equipped and carrying valid data.

For configuring paths as unequipped, this bit must be set in all master and slave slices for STS-3c/AU-4 payloads.~~This bit must be set in all master and slave slices for STS-3c/STM-1 payloads.~~

ADDUEV

When set high, the ADDUEV bit selects the all-ones pattern as the overwrite pattern when payload overwrite is enabled using the ADDUE bit. When set low, the ADDUEV bit selects the all-zeros pattern as the overwrite pattern when payload overwrite is enabled using the ADDUE bit.

This bit must be set in all master and slave slices for STS-3c/STM-1 payloads.

Registers 1190H, 1290H, 1390H, 1490H, 1590H, 1690H, 1790H, 1890H, 1990H, 1A90H, 1B90H, and 1C90H: TPPS Path AIS Control

Bit	Type	Function	Default
Bit 7	R/W	LOMTUAIS	0
Bit 6	R/W	TPAIS_EN	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LOPPAIS	0
Bit 2	R/W	PAISPAIS	0
Bit 1	R/W	LOPCONPAIS	0
Bit 0	R/W	PAISCONPAIS	0

This register controls the auto assertion of transmit path/TU AIS. These register bits should normally be set low when the TPPS is configured as a slave unless indicated otherwise.

PAISCONPAIS

When set high, the PAISCONPAIS bit enable path AIS insertion on the transmit stream when path AIS concatenation event is detected. When this bit is set low, the corresponding event has no effect on the transmit stream.

Note: This register bit should only be used when the RPPS is configured as a slave. Otherwise, it should normally be set low.

LOPCONPAIS

When set high, the LOPCONPAIS bit enable path AIS insertion on the transmit stream when loss of concatenated pointer (LOPCON) event is detected. When this bit is set low, the LOPCON event has no effect on the transmit stream.

Note: This register bit should only be used when the TPPS is configured as a slave. Otherwise, it should normally be set low.

PAISPAIS

When set high, the PAISPAIS bit enables path AIS insertion on the transmit stream when path AIS is detected on the Add bus. When PAISPAIS is set low, path AIS events have no effect on the transmit stream.

TPAIS_EN

When set high, the TPAIS_EN bit enables path AIS insertion into the transmit stream via the corresponding time-slot of the TPAIS input signal. When TPAIS_EN is set low, the TPAIS input signal have no effect on the transmit stream. Forcing TPAIS on master slice will force the slave slices into PAIS also.

LOPPAIS

When set high, the LOPPAIS bit enables path AIS insertion on the transmit stream when LOP events are detected on the Add bus. When LOPPAIS is set low, LOP events have no effect on the transmit stream.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

LOMTUAIS

When set high, the LOMTUAIS bit enables tributary path AIS insertion on the transmit stream when LOM events are detected on the Add bus. The path overhead (POH), the fixed stuff, and the pointer bytes (H1, H2) are unaffected. When LOMTUAIS is set low, LOM events have no effect on the transmit stream. LOMTUAIS must be set low when transmitting VT3 (TU3) payloads because the loss of multi-frame condition does not exist.

Registers 11A8H, 12A8H, 13A8H, 14A8H, 15A8H, 16A8H, 17A8H, 18A8H, 19A8H, 1AA8H, 1BA8H, and 1CA8H: TPPS Path Interrupt Status

Bit	Type	Function	Default
Bit 7	R	TPAIS	X
Bit 6	R	Unused	X
Bit 5	R	TTALI	X
Bit 4	R	TPIPI	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	APGMI	X
Bit 0	—	Unused	X

This register, together with the Section/Line Interrupt Status register, allows the source of an active interrupt for the transmit side to be identified down to the block level. Further register accesses to the block in question are required in order to determine each specific cause of an active interrupt and to acknowledge each interrupt source. These register bits are not cleared on read.

APGMI

The APGMI bits are high when an interrupt request is active from the APGM block.

TPIPI

The TPIPI bit is high when an interrupt request is active from the TPIP block.

TTALI

The TTALI bits is high when an interrupt request is active from the TTAL block.

TPAIS

The transmit stream alarm indication signal (TPAIS) bit is set high when path AIS is inserted in the transmit stream being processed by the TPPS. Transmit Path AIS assertion is controlled using the TTAL Control register or the TPPS Path AIS Control register with the Add bus pointer interpretation enabled. Note: TPAIS is not an interrupt bit.

Registers 11ACH, 12ACH, 13ACH, 14ACH, 15ACH, 16ACH, 17ACH, 18ACH, 19ACH, 1AACH, 1BACH, and 1CACH: TPPS Auxiliary Path Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LOPCONE	0
Bit 6	R/W	PAISCONE	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	PAISE	0
Bit 3	R/W	LOPE	0
Bit 2	R/W	LOME	0
Bit 1	R/W	Unused	0
Bit 0	R/W	Unused	0

This register controls the interrupt generation on output INTB by the corresponding interrupt status in the SPECTRA 4x155 TPPS Auxiliary Path Interrupt Status register. Note: These enable bits do not affect the actual interrupt bits found in the SPECTRA 4x155 TPPS Auxiliary Path Interrupt Status register.

These register bits should normally be set low when the TPPS is configured as a slave unless indicated otherwise.

LOME

The LOM interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOM interrupt status.

LOPE

The LOP interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOP interrupt status.

PAISE

The path alarm indication signal (PAIS) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PAIS interrupt status.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

PAISCONE

The path alarm indication signal concatenation (PAISCON) interrupt enable bit enables interrupt generation on output INTB by the auxiliary PAISCON interrupt status.

Note: This register bit should only be used when the TPPS is configured as a slave. Otherwise, it should normally be set low.

LOPCONE

The loss of pointer concatenation (LOPCON) interrupt enable bit enables interrupt generation on output INTB by the auxiliary LOPCON interrupt status.

Note: This register bit should only be used when the TPPS is configured as a slave. Otherwise, it should normally be set low.

Registers 11B0H, 12B0H, 13B0H, 14B0H, 15B0H, 16B0H, 17B0H, 18B0H, 19B0H, 1AB0H, 1BB0H, and 1CB0H: SPECTRA 4x155 TPPS Auxiliary Path Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	LOPCONI	X
Bit 6	R/W	PAISCONI	X
Bit 5	R/W	Reserved	X
Bit 4	R/W	PAISI	X
Bit 3	R/W	LOPI	X
Bit 2	R/W	LOMI	X
Bit 1	R/W	Unused	X
Bit 0	R/W	Unused	X

This register replicates the path interrupts that can be found in the TPIP register. However, unlike the TPIP interrupt register bits that clear-on-reads, these register bits do not clear when read. To clear these registers bits, a logic one must be written to the register bit.

LOMI

The loss of multi-frame interrupt status bit (LOMI) is set high on changes in the loss of multi-frame status.

LOPI

The loss of pointer interrupt status bit (LOPI) is set high on the change of loss of pointer status.

PAISI

The path AIS interrupt status bit (PAISI) is set high on changes in the path AIS status.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

PAISCONI

The path AIS concatenation interrupt (PAISCONI) bit is set high when there is a change of the path AIS concatenation state. This auxiliary interrupt status corresponds to the AU-3PAISCONI status in the TPIP Alarm Interrupt Status register.

LOPCONI

The loss of pointer concatenation interrupt (LOPCONI) bit is set high when there is a change of the pointer concatenation state. This auxiliary interrupt status corresponds to the AU-3LOPCONI status in the TPIP Alarm Interrupt Status register.

Registers 11C0H, 12C0H, 13C0H, 14C0H, 15C0H, 16C0H, 17C0H, 18C0H, 19C0H, 1AC0H, 1BC0H, and 1CC0H: TPOP Control

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	R/W	PERDIEN	0
Bit 5	R/W	PERDISRC	0
Bit 4	R/W	PERSIST	0
Bit 3	R/W	EXCFS	0
Bit 2	R/W	DH4	0
Bit 1	R/W	DB3	0
Bit 0	R/W	Reserved	0

The register controls the operation of the transport overhead processor for downstream diagnostics.

DB3

The diagnose BIP-8 enable bit (DB3) controls the inversion of the path BIP-8 byte (B3) in the transmit stream. When a logic zero is written to this bit position, the B3 byte is transmitted uncorrupted. When a logic one is written to this bit position, the B3 byte is inverted, causing the insertion of eight path BIP-8 errors per frame.

DH4

The diagnose multi-frame indicator enable bit (DH4) controls the inversion of the multi-frame indicator (H4) byte in the transmit stream. This bit may be used to cause an out of multi-frame alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic zero is written to this bit position, the H4 byte is unmodified. When a logic one is written to this bit position, the H4 byte is inverted.

EXCFS

The fixed stuff column BIP-8 exclusion bit (EXCFS) controls the inclusion of bytes in the fixed stuff columns of the STS-1 (STM-0/AU-3) payload carrying tributaries in path BIP-8 calculations. When EXCFS is set high, the value of bytes in the fixed stuff columns do not affect the path BIP-8 byte (B3). When EXCFS is set low, data in the fixed stuff bytes are included in path BIP-8 calculations. This bit must be set low when the TPPS containing the TPOP is processing an STS-3c (STM-1/AU-4) stream.

PERSIST

The path far end receive failure alarm persistence bit (PERSIST) controls the persistence of the RDI asserted into the transmit stream. When PERSIST is a logic one, the RDI code inserted into the transmit stream as a result of consequential actions is asserted for a minimum of 20 frames in non-enhanced RDI mode, or the last valid RDI code before an idle code (idle codes are when bits 5,6,7 are 000, 001, or 011) is asserted for 20 frames in enhanced RDI mode. When PERSIST is logic zero, the transmit RDI code changes immediately based on received alarm conditions.

PERDISRC

The path enhanced RDI source (PERDISRC) bit controls the source of the path enhanced RDI code. When PERDISRC is set high, the path enhanced RDI code is sourced from internal receive side alarms as controlled by the RPPS Path REI/RDI Control (#1, #2) and Path Enhanced RDI Control (#1, #2) registers. When PERDISRC is set low, the path enhanced RDI code is sourced from the TPOP Path Status register.

PERDIEN

The path enhanced RDI enable (PERDIEN) bit controls path RDI insertion. When PERDIEN is set high, path enhanced RDI assertion (bits 5, 6, and 7 of the G1 byte) is enabled while normal path RDI (bit 5 of the G1 byte) and auxiliary path RDI (bit 6 of the G1 byte) are disabled. When PERDIEN is set low, path enhanced RDI assertion is disabled while normal path RDI and auxiliary path RDI are enabled.

Registers 11C1H, 12C1H, 13C1H, 14C1H, 15C1H, 16C1H, 17C1H, 18C1H, 19C1H, 1AC1H, 1BC1H, and 1CC1H: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	FTPTR	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	NDF	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls the pointer generation in the transmit stream.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

NDF

The NDF insert bit controls the insertion of new data flags in the payload pointer. When a logic one is written to this bit, the pattern contained in the NDF[3:0] bits in the TPOP Payload Pointer MSB register is inserted continuously in the payload pointer of the transmit stream. When a logic zero is written to this bit, the normal pattern (‘b0110) is inserted in the payload pointer.

FTPTR

The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer registers into the transmit stream for diagnostic purposes. This allows upstream payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated. If FTPTR is set to logic one, the APTR[9:0] bits of the TPOP Payload Pointer registers are inserted into the H1 and H2 bytes of the transmit stream. When FTPTR is set and immediately reset at least one Arbitrary Pointer substitution is guaranteed to be sent. If FTPTR is logic zero, a valid pointer is inserted.

Registers 11C3H, 12C3H, 13C3H, 14C3H, 15C3H, 16C3H, 17C3H, 18C3H, 19C3H, 1AC3H, 1BC3H, and 1CC3H: TPOP Current Pointer LSB

Bit	Type	Function	Default
Bit 7	R	CPTR[7]	X
Bit 6	R	CPTR[6]	X
Bit 5	R	CPTR[5]	X
Bit 4	R	CPTR[4]	X
Bit 3	R	CPTR[3]	X
Bit 2	R	CPTR[2]	X
Bit 1	R	CPTR[1]	X
Bit 0	R	CPTR[0]	X

Registers 11C4H, 12C4H, 13C4H, 14C4H, 15C4H, 16C4H, 17C4H, 18C4H, 19C4H, 1AC4H, 1BC4H, and 1CC4H: TPOP Current Pointer MSB

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	—	Unused	X
Bit 2	—	Unused	X
Bit 1	R	CPTR[9]	X
Bit 0	R	CPTR[8]	X

CPTR[9:0]

The CPTR[9:0] bits reflect the value of the active offset on the transmit stream as indicated by pulses on the AC1J1V1 signal. It is recommended the CPTR[9:0] value be software debounced to ensure a correct value is received.

Registers 11C5H, 12C5H, 13C5H, 14C5H, 15C5H, 16C5H, 17C5H, 18C5H, 19C5H, 1AC5H, 1BC5H, and 1CC5H: TPOP Payload Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

Registers 11C6H, 12C6H, 13C6H, 14C6H, 15C6H, 16C6H, 17C6H, 18C6H, 19C6H, 1AC6H, 1BC6H, and 1CC6H: TPOP Payload Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	1
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

APTR[9:0]

The APTR[9:0] bits are used to set an arbitrary active offset value in the transmit stream. The arbitrary pointer value is transferred by writing a logic one to the FTPTR bit in the TPOP Pointer Control Register. A legal value (that is, 0 ≤ pointer value ≤ 782) results in a new pointer in the transmit stream.

S1-S0

The payload pointer size bits (S[1:0]) are inserted in the S[1:0] bit positions in the payload pointer in the transmit stream.

NDF[3:0]

The new data flag bits (NDF[3:0]) are inserted in the NDF bit positions when the TPOP makes a discontinuous change in active offset or when the NDF bit in the TPOP Pointer Control register is set to logic one.

Registers 11C7H, 12C7H, 13C7H, 14C7H, 15C7H, 16C7H, 17C7H, 18C7H, 19C7H, 1AC7H, 1BC7H, and 1CC7H: TPOP Path Trace

Bit	Type	Function	Default
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

This register contains the value to be inserted in the path trace byte (J1) of the transmit stream when the Transmit Path Trace Buffer block is disabled (TPTBEN set low).

J1[7:0]

The J1[7:0] bits are inserted in the J1 byte position in the transmit stream when the associated SPTB block is disabled.

Registers 11C8H, 12C8H, 13C8H, 14C8H, 15C8H, 16C8H, 17C8H, 18C8H, 19C8H, 1AC8H, 1BC8H, and 1CC8H: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	0
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	0
Bit 0	R/W	C2[0]	1

This register contains the value to be inserted in the path signal label byte (C2) of the transmit stream.

C2[7:0]

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream when the corresponding TDIS register bit is set low. Upon reset, the register value defaults to 01H, which represents “Equipped – Non Specific Payload.”

Registers 11C9H, 12C9H, 13C9H, 14C9H, 15C9H, 16C9H, 17C9H, 18C9H, 19C9H, 1AC9H, 1BC9H, and 1CC9H: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	PREI[3]	0
Bit 6	R/W	PREI[2]	0
Bit 5	R/W	PREI[1]	0
Bit 4	R/W	PREI[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	PERDI6	0
Bit 1	R/W	PERDI7	0
Bit 0	R/W	G1[0]	0

This register reflects the value inserted in the path status byte (G1) of the transmit stream.

G1[0]

The G1[0] bit is inserted in the unused bit positions of the path status byte when corresponding TDIS register bit is set low.

PERDI6, PERDI7

The PERDI6 and PERDI7 bits control the insertion of the STS path receive defect indication alarm (PRDI6 and PRDI7, respectively) when PERDIEN is logic one, and are inserted in the unused bit positions G1[2:1] in the path status byte when PERDIEN is logic zero. The function is described in Table 14.

Table 14 Transmit RDI Control

PERDIEN	IBER	PERDISRC	Tx G1 bit 5	tx G1 bit 6	tx G1 bit 7
0	0	0	PRDI5+Reg[3]	Reg[2]	Reg[1]
0	0	1	PRDI5+Reg[3]	Reg[2]	Reg[1]
0	1	0	SPE_G1[5]+Reg[3]	Reg[2]	Reg[1]
0	1	1	SPE_G1[5]+Reg[3]	Reg[2]	Reg[1]
1	0	0	Reg[3]	Reg[2]	Reg[1]
1	0	1	PRDI5	PRDI6	PRDI7
1	1	0	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]
1	1	1	SPE_G1[5]	SPE_G1[6]	SPE_G1[7]

Notes

IBER = 1 when in-band reporting is enabled. In-band error reporting is enabled when RXSEL[1:0] = ”10” in the SPECTRA 4x155 TPPS Path Configuration register (bits 1:0).

SPE_G1[7:5] = bits 7 through 5 of the G1 byte on the Add bus

PRDI7, PRDI6, PRDI5 = bits 7 through 5 of the G1 byte from the associated RPOP or the transmit alarm port of the SPECTRA 4x155

Reg[3:1] = PRDI, PERDI6, PERDI7 register bit values, respectively

PRDI

The PRDI bit controls the insertion of the STS path receive defect indication alarm. The function is described in the table above.

PREI[3:0]

The path REI count (PREI[3:0]) is inserted in the path REI bit positions in the path status byte when the corresponding TDIS register bit is set low. The value contained in PREI[3:0] is cleared after being inserted in the path status byte. Any non-zero PREI[3:0] value overwrites the value that would normally have been inserted based on the number of PREIs accumulated from the BIP-8 errors detected by the companion RPOP in the SPECTRA 4x155 during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

Registers 11CAH, 12CAH, 13CAH, 14CAH, 15CAH, 16CAH, 17CAH, 18CAH, 19CAH, 1ACAH, 1BCAH, and 1CCAH: TPOP Path User Channel

Bit	Type	Function	Default
Bit 7	R/W	F2[7]	0
Bit 6	R/W	F2[6]	0
Bit 5	R/W	F2[5]	0
Bit 4	R/W	F2[4]	0
Bit 3	R/W	F2[3]	0
Bit 2	R/W	F2[2]	0
Bit 1	R/W	F2[1]	0
Bit 0	R/W	F2[0]	0

This register contains the value to be inserted in the path user channel byte (F2) of the transmit stream.

F2[7:0]

The F2[7:0] bits are inserted in the F2 byte position in the transmit stream when the corresponding TDIS register bit is set low.

Registers 11CBH, 12CBH, 13CBH, 14CBH, 15CBH, 16CBH, 17CBH, 18CBH, 19CBH, 1ACBH, 1BCBH, and 1CCBH: TPOP Path Growth #1

Bit	Type	Function	Default
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

This register contains the value to be inserted in the path growth byte #1 (Z3) of the transmit stream.

Z3[7:0]

The Z3[7:0] bits are inserted in the Z3 byte position in the transmit stream when the corresponding TDIS register bit is set low ~~or TPOHEN input is low during the corresponding path growth #1 bit positions in the path overhead input stream, TPOH~~.

Registers 11CCH, 12CCH, 13CCH, 14CCH, 15CCH, 16CCH, 17CCH, 18CCH, 19CCH, 1ACCH, 1BCCH, and 1CCCH: TPOP Path Growth #2

Bit	Type	Function	Default
Bit 7	R/W	Z4[7]	0
Bit 6	R/W	Z4[6]	0
Bit 5	R/W	Z4[5]	0
Bit 4	R/W	Z4[4]	0
Bit 3	R/W	Z4[3]	0
Bit 2	R/W	Z4[2]	0
Bit 1	R/W	Z4[1]	0
Bit 0	R/W	Z4[0]	0

This register contains the value to be inserted in the path growth byte #2 (Z4) of the transmit stream.

Z4[7:0]

The Z4[7:0] bits are inserted in the Z4 byte position in the transmit stream when the corresponding TDIS register bit is set low ~~or TPOHEN input is low during the corresponding path growth #2 bit positions in the path overhead input stream, TPOH~~.

Registers 11CDH, 12CDH, 13CDH, 14CDH, 15CDH, 16CDH, 17CDH, 18CDH, 19CDH, 1ACDH, 1BCDH, and 1CCDH: TPOP Tandem Connection Maintenance

Bit	Type	Function	Default
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

This register contains the value to be inserted in the tandem connection maintenance byte (Z5) of the transmit stream.

Z50-Z57

The Z5[7:0] bits are inserted in the Z5 byte position in the transmit stream when the corresponding TDIS register bit is set low ~~or TPOHEN input is low during the tandem connection maintenance byte positions in the corresponding path overhead input stream, TPOH~~.

Registers 11D0H, 12D0H, 13D0H, 14D0H, 15D0H, 16D0H, 17D0H, 18D0H, 19D0H, 1AD0H, 1BD0H, and 1CD0H: TTAL Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	H4BYP	0
Bit 5	R/W	CLRFS	0
Bit 4	R/W	Reserved	1
Bit 3	R/W	Reserved	0
Bit 2	R/W	ESEE	0
Bit 1	R/W	PJEE	0
Bit 0	R/W	PAIS	0

This register allows the operation of the Transmit TelecomBus Aligner to be configured.

PAIS

The PAIS bit controls the insertion of path alarm indication signal in the transmit stream. When logic one is written to this bit, the SPE and the pointer bytes (H1 – H3) are set to all-ones. When a logic zero is written to this bit, the SPE and pointer bytes are processed normally. Upon de-activation of path AIS, a new data flag accompanies the first valid pointer.

PJEE

The pointer justification event interrupt enable bit (PJEE) controls the activation of the interrupt output when a pointer justification is inserted in the transmit stream. When PJEE is set high, insertion of pointer justification events in the transmit stream will activate the interrupt (INTB) output. When PJEE is set low, insertion of pointer justification events in the transmit stream will not affect INTB.

ESEE

The elastic store error interrupt enable bit (ESEE) controls the activation of the interrupt output when a FIFO underflow or overflow has been detected in the elastic store . When ESEE is set high, FIFO flow error events will affect the interrupt (INTB) output. When ESEE is set low, FIFO flow error events will not affect INTB.

Reserved

The Reserved bits must be set to their default value for proper operation of the SPECTRA-4X155.

CLRFS

The clear fixed stuff column bit (CLRFS) enables the setting of the fixed stuff columns in virtual tributary (low order tributary) mappings to zero. When a logic one is written to CLRFS, the fixed stuff column data are set to 00H. When a logic zero is written to CLRFS, the fixed stuff column data from the Add bus is placed on the transmit stream unchanged. The location of the fixed stuff columns in the SPE (VC) is dependent on the whether the TPPS containing the TTAL is processing concatenated payload.

H4BYP

The tributary multi-frame bypass bit (H4BYP) controls whether the TTAL block overwrites the H4 byte in the path overhead with an internally generated sequence. When H4BYP is set high, the H4 byte carried in the Add bus is placed in the transmit stream unchanged. When H4BYP is set low, the H4 byte is replaced by the sequence ‘Hfc, ‘Hfd, ‘Hfe, and ‘Hff. The phase of the four frames in the multi-frame is synchronized by the V1 pulse in AC1J1V1 input.

Registers 11D1H, 12D1H, 13D1H, 14D1H, 15D1H, 16D1H, 17D1H, 18D1H, 19D1H, 1AD1H, 1BD1H, and 1CD1H: TTAL Interrupt Status and Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	ESD[1]	1
Bit 4	R/W	ESD[0]	0
Bit 3	R	ESEI	X
Bit 2	R	PPJI	X
Bit 1	R	NPJI	X
Bit 0	R/W	Reserved	0

This register allows the control of the transmit stream and sensing of interrupt status.

The interrupt bits (and the interrupt) are cleared when this register is read.

Reserved

The Reserved bit must be set low for correct operation of the SPECTRA 4x155.

NPJI

The transmit stream negative pointer justification interrupt status bit (NPJI) is set high when the TTAL inserts a negative pointer justification event in the transmit stream.

PPJI

The transmit stream positive pointer justification interrupt status bit (PPJI) is set high when the TTAL inserts a positive pointer justification event in the transmit stream.

ESEI

The Drop bus elastic store error interrupt status bit (ESEI) is set high when the FIFO in TTAL underflows or overflows. This will cause the TTAL to reset itself. Note: It can lose the J1, and go out of AIS for a short period of time if it was in AIS state.

ESD0- ESD1

The elastic store depth control bits (ESD[1:0]) set elastic store FIFO fill thresholds i.e., the thresholds for the ES_upperT and ES_lowerT indications. The thresholds for the four ESD[1:0] codes are shown in Table 15.

Table 15 Transmit ESD[1:0] Codepoints

ESD[1:0]	Hard neg limit	Soft neg limit	Soft pos limit	Hard pos limit
00	4	0	0	4
01	5	1	1	4
10	6	4	4	6
11	7	6	6	7

Definition

Soft neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the soft region of the FIFO (In the soft region, the TTAL generates outgoing negative justification at the rate of 1 in every 16 frames).

Hard neg limit: The maximum number of incoming negative justification (after several incoming positive justifications) before entering the hard region of the FIFO (In the hard region, the TTAL generates outgoing negative justification at the rate of 1 in every 4 frames).

Soft pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the soft region of the FIFO (In the soft region, the TTAL generates outgoing positive justification at the rate of 1 in every 16 frames).

Hard pos limit: The maximum number of incoming positive justification (after several incoming negative justifications) before entering the hard region of the FIFO (In the hard region the TTAL will start generates outgoing positive justification at the rate of in 1 every 4 frames).

Registers 11D2H, 12D2H, 13D2H, 14D2H, 15D2H, 16D2H, 17D2H, 18D2H, 19D2H, 1AD2H, 1BD2H, and 1CD2H: TTAL Alarm and Diagnostic Control

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	ITUAIS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	ESAIS	0
Bit 0	R/W	DH4	0

This register controls the tributary format on the transmit stream.

DH4

The diagnose multi-frame indicator enable bit (DH4) controls the inversion of the multi-frame indicator (H4) byte in the transmit stream. This bit may be used to cause an out of multi-frame alarm in downstream circuitry when the SPE (VC) is used to carry virtual tributary (VT) or tributary unit (TU) based payloads. When a logic zero is written to this bit position, the H4 byte is unmodified. When a logic one is written to this bit position, the H4 byte is inverted.

ESAIS

The elastic store error path AIS insertion enable bit (ESAIS) controls the insertion of path AIS in the transmit stream when a FIFO underflow or overflow has been detected in the elastic store. When ESAIS is set high, detection of FIFO flow error will cause path AIS to be inserted in the transmit stream for three frames. When ESAIS is set low, path AIS is not inserted as a result of FIFO errors.

Reserved

The Reserved bit must be set to logic zero for correct operation of the SPECTRA 4x155.

ITUAIS

The insert tributary path AIS bits controls the insertion of Tributary Path AIS in the transmit stream when transmitting VT-11 (TU-11), VT-12 (TU-12), and VT-2 (TU-2) payloads. When ITUAIS is set high, columns in the transmit stream carrying tributary traffic are set to all-ones. The pointer bytes (H1, H2, and H3), the path overhead column, and the fixed stuff columns are unaffected. Normal operation resumes when the ITUAIS bit is set low. The ITUAIS bit does not work for VT-3 (TU-3) tributary payloads and the ITUAIS bit must be set low. The STM1_CONCAT register bit must be set for TU2, TU11, and TU12 payloads in a VC-4.

Registers 11E0H, 12E0H, 13E0H, 14E0H, 15E0H, 16E0H, 17E0H, 18E0H, 19E0H, 1AE0H, 1BE0H, and 1CE0H: TPIP Status and Control (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	AU-3LOPCONV	X
Bit 5	R	LOPV	X
Bit 4	R	AU-3PAISCONV	X
Bit 3	R	PAISV	X
Bit 2	R	Reserved	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

This register provides configuration and reports the status of the corresponding TPIP if the EXTD bit is set low in the TPIP Pointer MSB register.

NEWPTRE

When a logic one is written to the NEWPTRE interrupt enable bit position, the reception of a new_point indication will activate the interrupt (INT) output.

NEWPTRI

The NEWPTRI bit is set to logic one when a new_point indication is received. This bit (and the interrupt) is cleared when this register is read.

Reserved:

The Reserved bits are status bits and must be ignored when this register is read.

PAISV

The path AIS status bit (PAIS) indicates reception of path AIS alarm in the receive stream.

AU-3PAISCONV

The AU-3 concatenation path AIS status bit (AU-3PAISCONV) indicates reception of path AIS alarm in the concatenation indication in the transmit STS-1 (STM-0/AU-3) or equivalent stream.

LOPV

The loss of pointer status bit (LOPV) indicates entry to the LOP_state in the TPIP pointer interpreter state machine.

AU-3LOPCONV

The AU-3 concatenated loss of pointer status bit (AU-3LOPCONV) indicates entry to LOPCON_state for the transmit STS-1 (STM-0/AU-3) or equivalent stream in the TPIP pointer interpreter.

Registers 11E0H, 12E0H, 13E0H, 14E0H, 15E0H, 16E0H, 17E0H, 18E0H, 19E0H, 1AE0H, 1BE0H, and 1CE0H: TPIP Status and Control (EXTD=1)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	IINVCNT	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	—	Unused	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

This register provides configuration of the corresponding TPIP if the EXTD bit is set high in the TPIP Pointer MSB register.

Reserved

The Reserved read/write bits must be set low for proper operation of the SPECTRA-4X155. The Reserved read bits must be ignored when this register is read.

IINVCNT

When a logic one is written to the IINVCNT (Intuitive Invalid Pointer Counter) bit, if in the LOP state, 3 x new point will reset the inv_point count. If this bit is set to logic zero, the inv_point count will not be reset if in the LOP state and 3 x new pointers are detected.

Registers 11E1H, 12E1H, 13E1H, 14E1H, 15E1H, 16E1H, 17E1H, 18E1H, 19E1H, 1AE1H, 1BE1H, and 1CE1H: TPIP Alarm Interrupt Status (EXTD=0)

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	AU-3LOPCONI	X
Bit 5	R	LOPI	X
Bit 4	R	AU-3PAISCONI	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	PREII	X

This register allows identification and acknowledgment of path level alarm and error event interrupts when the EXTD bit is set low in the TPIP Pointer MSB register. This register is reserved and should not be used when the EXTD bit is set high. These bits (and the interrupt) are cleared when the Interrupt Status Register is read.

PREII

The PREI interrupt status bit (PREII) is set high when a path REI is detected.

BIPEI

The BIP error interrupt status bit (BIPEI) is set high when a path BIP-8 error is detected.

PRDII

The PRDII interrupt status bit is set high on assertion and removal of the corresponding path RDI status.

PAISI

The PAISI interrupt status bit is set high on assertion and removal of the corresponding path alarm indication signal status.

AU-3PAISCONI

The AU-3PAISCONI interrupt status bit is set high on assertion and removal of the corresponding AU-3 path alarm indication signal concatenation status.

LOPI

The LOPI interrupt status bit is set high on assertion and removal of the corresponding loss of pointer status.

AU-3LOPCONI

The AU-3LOPCONI interrupt status bit is set high on assertion and removal of the corresponding AU-3 loss of pointer concatenation status.

Reserved

The Reserved bits are status bits and must be ignored when this register is read.

Registers 11E2H, 12E2H, 13E2H, 14E2H, 15E2H, 16E2H, 17E2H, 18E2H, 19E2H, 1AE2H, 1BE2H, and 1CE2H: TPIP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6	R	CONCATI	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	ILLPTRI	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts. These bits (and the interrupt) are cleared when this register is read. Please refer to the pointer interpreter state diagram and notes in the Function Description of the RPOP for alarm definitions.

NDFI

The NDF enabled indication interrupt status bit (NDFI) is set high when one of the NDF enable patterns is observed in the receive stream.

PSEI, NSEI

The positive and negative justification event interrupt status bits (PSEI, NSEI) are set high when the TPIP block responds to an inc_ind or dec_ind indication, respectively, in the receive stream.

ILLPTRI

The illegal pointer interrupt status bit (ILLPTRI) is set high when an illegal pointer observed on the receive stream.

INVNDFI

The invalid NDF interrupt status bit (NDFI) is set high when an invalid NDF code is observed on the receive stream.

DISCOPAI

The discontinuous pointer change interrupt status bit (DISCOPAI) is set high when the TPIP active offset is changed due to receiving the same valid pointer for three consecutive frames (3 x eq_new_point indication).

ILLJREQI

The illegal justification request interrupt status bit (ILLJREQI) is set high when the TPIP detects a positive or negative pointer justification request (inc_req, dec_req) that occurs within three frames of a previous justification event (inc_ind, dec_ind) or an active offset change due to an NDF enable indication (NDF_enable).

CONCATI

The concatenation indication error interrupt status bit (CONCATI) is set high when the H1, H2 bytes do not match the concatenation indication ('b1001xx1111111111).

This interrupt bit should be ignored for a master slice.

Registers 11E3H, 12E3H, 13E3H, 14E3H, 15E3H, 16E3H, 17E3H, 18E3H, 19E3H, 1AE3H, 1BE3H, and 1CE3H: TPIP Alarm Interrupt Enable (EXTD=0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	AU-3LOPCONE	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	AU-3PAISCONE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	RDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	PREIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set low in the TPIP Pointer MSB register.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

PREIE

When a logic one is written to the PREIE interrupt enable bit position, the reception of one or more path REIs will activate the interrupt (INTB) output.

BIPEE

When a logic one is written to the BIPEE interrupt enable bit position, the detection of one or more path BIP-8 errors will activate the interrupt (INTB) output.

PAISE

When a logic one is written to the PAISE interrupt enable bit position, a change in the path AIS state will activate the interrupt (INTB) output.

AU-3PAISCONE

When a logic one is written to the AU-3PAISCONE interrupt enable bit position, a change in the AU-3 concatenation path AIS state will activate the interrupt (INTB) output.

LOPE

When a logic one is written to the LOPE interrupt enable bit position, a change in the loss of pointer state will activate the interrupt (INTB) output.

AU-3LOPCONE

When a logic one is written to the AU-3LOPCONE interrupt enable bit position, a change in the AU-3 concatenation loss of pointer state will activate the interrupt (INTB) output.

Registers 11E3H, 12E3H, 13E3H, 14E3H, 15E3H, 16E3H, 17E3H, 18E3H, 19E3H, 1AE3H, 1BE3H, and 1CE3H: TPIP Alarm Interrupt Enable (EXTD=1)

Bit	Type	Function	Default
Bit 7	R	LOPCONV	X
Bit 6	R	Reserved	X
Bit 5	R	PAISCONV	X
Bit 4	R	Reserved	X
Bit 3	—	Reserved	X
Bit 2	—	Reserved	X
Bit 1	—	Reserved	X
Bit 0	R/W	ERDIE	0

This register allows interrupt generation to be enabled or disabled for alarm and error events. This register can be accessed when the EXTD bit is set high in the TPIP Pointer MSB register.

ERDIE

When a 1 is written to the RDIE interrupt enable bit position, a change in the path enhanced RDI state will activate the interrupt (INT) output.

Reserved

The Reserved bits are status bits and must be ignored when this register is read.

LOPCONV

The concatenated loss of pointer value bit (LOPCONV) indicates the loss of concatenated pointer status for the STS-1 (STM-1/AU-3) equivalent stream of the STS-3c (STM1/AU4) being processed in the slave slice.

PAISCONV

The concatenated path alarm indication bit (PAISCONV) indicates the presence of all-ones instead of the concatenation indicator in the payload pointer bytes. The pointer bytes refers to the H1/H2 bytes of the STS-1 (STM-1/AU-3) equivalent stream of the STS-3c (STM1/AU4) being processed in the slave slice.

Registers 11E4H, 12E4H, 13E4H, 14E4H, 15E4H, 16E4H, 17E4H, 18E4H, 19E4H, 1AE4H, 1BE4H, and 1CE4H: TPIP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	CONCATE	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	ILLPTRE	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register allows interrupt generation to be enabled or disabled for pointer events.

NDFE

When a logic one is written to the NDFE interrupt enable bit position, the detection of an NDF_enable indication will activate the interrupt (INTB) output.

PSEE

When a logic one is written to the PSEE interrupt enable bit position, a positive pointer adjustment event will activate the interrupt (INTB) output.

NSEE

When a logic one is written to the NSEE interrupt enable bit position, a negative pointer adjustment event will activate the interrupt (INTB) output.

ILLPTRE

When a logic one is written to the ILLPTRE interrupt enable bit position, an illegal pointer will activate the interrupt (INT) output.

INVNDFE

When a logic one is written to the INVNDFE interrupt enable bit position, an invalid NDF code will activate the interrupt (INTB) output.

DISCOPAE

When a logic one is written to the DISCOPAE interrupt enable bit position, a change of pointer alignment event will activate the interrupt (INTB) output.

CONCATE

When a logic one is written to the CONCATE interrupt enable bit position, an invalid Concatenation Indicator event will activate the interrupt (INTB) output.

ILLJREQE

When a logic one is written to the ILLJREQE interrupt enable bit position, an illegal pointer justification request will activate the interrupt (INTB) output.

Registers 11E5H, 12E5H, 13E5H, 14E5H, 15E5H, 16E5H, 17E5H, 18E5H, 19E5H, 1AE5H, 1BE5H, and 1CE5H: TPIP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

The register reports the lower eight bits of the active offset.

PTR[7:0]

The PTR[7:0] bits contain the eight LSBs of the active offset value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the TPIP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

Registers 11E6H, 12E6H, 13E6H, 14E6H, 15E6H, 16E6H, 17E6H, 18E6H, 19E6H, 1AE6H, 1BE6H, and 1CE6H: TPIP Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDFPOR	0
Bit 6	R/W	EXTD	0
Bit 5	R/W	Reserved	0
Bit 4	R	CONCAT	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

This register reports the upper two bits of the active offset, the SS bits in the receive pointer.

PTR[9:8]

The PTR[9:8] bits contain the two MSBs of the current pointer value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced.

CONCAT

The CONCAT bit is set high if the H1, H2 pointer byte received matches the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

RESERVED

The Reserved bit must be set low for the correct operation of the SPECTRA 4x155.

EXTD

The EXTD bit extends the TPIP registers to facilitate additional mapping. If this bit is set to logic one the register mapping, for the TPIP Status and Control register, the TPIP Alarm Interrupt Status register and the TPIP Alarm Interrupt Enable registers are extended.

NDFPOR

The NDFPOR (new data flag pointer of range) bit controls the definition of the NDF_enable indication for entry to the LOP state under 8Xndf_enable events. When NDFPOR is set high, for the purposes of detect of loss of events only, the definition of the NDF_enable indication does not require the pointer value to be within the range of 0 to 782. When NDFPOR is set low, NDF_enable indications require the pointer to be within 0 to 782.

Registers 11E8H, 12E8H, 13E8H, 14E8H, 15E8H, 16E8H, 17E8H, 18E8H, 19E8H, 1AE8H, 1BE8H, and 1CE8H: TPIP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	BE[7]	X
Bit 6	R	BE[6]	X
Bit 5	R	BE[5]	X
Bit 4	R	BE[4]	X
Bit 3	R	BE[3]	X
Bit 2	R	BE[2]	X
Bit 1	R	BE[1]	X
Bit 0	R	BE[0]	X

Registers 11E9H, 12E9H, 13E9H, 14E9H, 15E9H, 16E9H, 17E9H, 18E9H, 19E9H, 1AE9H, 1BE9H, and 1CE9H: TPIP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	BE[15]	X
Bit 6	R	BE[14]	X
Bit 5	R	BE[13]	X
Bit 4	R	BE[12]	X
Bit 3	R	BE[11]	X
Bit 2	R	BE[10]	X
Bit 1	R	BE[9]	X
Bit 0	R	BE[8]	X

BE[15:0]

Bits BE[15:0] represent the number of path BIP errors that have been detected since the last time the path BIP-8 registers were polled by writing to the SPECTRA 4x155 Reset and Identity register. The write access transfers the internally accumulated error count to the path BIP-8 registers within 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

Registers 11ECH, 12ECH, 13ECH, 14ECH, 15ECH, 16ECH, 17ECH, 18ECH, 19ECH, 1AECH, 1BECH, and 1CECH: TPIP Tributary Multi-frame Status and Control

Bit	Type	Function	Default
Bit 7	R	LOMI	X
Bit 6	R	LOMV	X
Bit 5	R/W	LOME	0
Bit 4	R/W	Reserved	0
Bit 3	R	COMAI	X
Bit 2	R/W	COMAE	0
Bit 1	R/W	Reserved	0
Bit 0	R	Reserved	X

This register reports the status of the multi-frame framer and enables interrupts caused by framer events.

RESERVED

The Reserved read/write bits must be set low for proper operation of the SPECTRA-4X155. The Reserved read bits must be ignored when this register is read.

COMAE

The change of multi-frame alignment interrupt enable bit (COMAE) controls the generation of interrupts on when the SPECTRA 4x155 detect a change in the multi-frame phase. When LOME is set high, an interrupt is generated upon change of multi-frame alignment. When COMAE is set low, COMA has no effect on the interrupt output (INTB).

COMAI

The change of multi-frame alignment interrupt status bit (COMAI) is set high on changes in the multi-frame alignment. This bit is cleared (and the interrupt acknowledged) when this register is read.

LOME

The LOM interrupt enable bit (LOME) controls the generation of interrupts on declaration and removal of LOM indication. When LOME is set high, an interrupt is generated upon loss of multi-frame. When LOME is set low, LOM has no effect on the interrupt output (INTB).

LOMV

The loss of multi-frame status bit (LOMV) reports the current state of the multi-frame framer monitoring the receive stream. LOMV is set high when LOM is declared and is set low when multi-frame alignment has been acquired.

LOMI

The loss of multi-frame interrupt status bit (LOMI) is set high on changes in the loss of multi-frame status. This bit is cleared (and the interrupt acknowledged) when this register is read.

Registers 11EDH, 12EDH, 13EDH, 14EDH, 15EDH, 16EDH, 17EDH, 18EDH, 19EDH, 1AEDH, 1BEDH, and 1CEDH: TPIP BIP Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	DISFS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

DISFS

When set high, the DISFS bit controls the BIP-8 calculations to ignore the fixed stuffed columns in an AU-3 carrying a VC-3. When DISFS is set low, BIP-8 calculations include the fixed stuff columns in an STS-1 (STM-0/AU-3) stream. This bit must be set low when the TPPS containing the TPIP is processing an STS-3c (STM-1/AU-4) stream.

BLKBIP

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be reported and accumulated on a block basis. A single BIP error is accumulated and reported to the return transmit path overhead processor if any of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated and reported on a bit basis.

ENSS

The enable size bit (ENSS) controls whether the SS bits in the payload pointer are used to determine offset changes in the pointer interpreter state machine. When a logic one is written to this bit, an incorrect SS bit pattern (that is, ≠10) will prevent TPIP from issuing NDF_enable, inc_ind and dec_ind indications. When a logic zero is written to this bit, the SS bits received do not affect active offset change events. Regardless of the logic state of the ENSS bit, an incorrect SS bit pattern will trigger an inv_point indication.

SOS

The stuff opportunity spacing control bit (SOS) controls the spacing between consecutive pointer justification events on the receive stream. When a logic one is written to this bit, the definition of inc_ind and dec_ind indications includes the requirement that active offset changes have occurred a least three frame ago. When a logic zero is written to this bit, pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Registers 11F0H, 12F0H, 13F0H, 14F0H, 15F0H, 16F0H, 17F0H, 18F0H, 19F0H, 1AF0H, 1BF0H, and 1CF0H: APGM Generator Control #1

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	GEN_INV_PRBS	0
Bit 5	R/W	GEN_AUTO	0
Bit 4	R/W	GEN_FERR	0
Bit 3	R/W	GEN_SIGE	0
Bit 2	R/W	GEN_FSENB	0
Bit 1	R/W	GEN_REGEN	0
Bit 0	R/W	GEN_EN	0

GEN_EN

The Generator Enable (GEN_EN) bit enables the insertion of PRBS into the Transmit payload. When GEN_EN is set high, the PRBS bytes will overwrite the processed payload data. When GEN_EN is set low, the incoming payload is unaltered. This bit has not effect in Autonomous Input Mode.

GEN_REGEN

The Generator Regenerate (GEN_REGEN) bit can be used to re-initialize the generator LFSR and begin regenerating the PRBS from the known reset state. The LFSR reset state is dependent on the set sequence number. Setting this bit in a master generator will automatically force all slaves to reset at the same time. This bit will clear itself when the operation is complete. Upon a frame realignment on the Add Bus #1 (AC1J1V1_AFP[1]) the Generators must be regenerated.

GEN_FSENB

The Generator Fixed Stuff Enable (GEN_FSENB) bit determines whether the PRBS is inserted into the (STS-1/STM-0) fixed stuff bytes of the processed payload. When set to logic one, the PRBS is not inserted into the fixed stuff bytes and the bytes are output unaltered. When set to logic zero, the PRBS is inserted into the fixed stuff bytes. The Fixed stuff columns are columns 30 and 59 of the STS-1 payload.

GEN_FSENB should be disabled when using the generator in master/slave configuration to support de-multiplexed concatenated payloads.

GEN_SIGE

The Generator Signature Interrupt Enable (GEN_SIGE) bit allows an interrupt to be asserted on INT when a signature verification mismatch occurs. When GEN_SIGE is set high, a change in the signature verification state (GEN_SIGV) will trigger an interrupt. When GEN_SIGE is set low, no interrupt will be asserted.

GEN_FERR

The Generator Force Error (GEN_FERR) bit is used to force bit errors in the inserted PRBS. When logic one is written to this bit, the MSB of the PRBS byte will be inverted, inducing a single bit error. The register bit will clear itself when the operation is complete. A second forced error must not be attempted for at least 200ns after this bit has been read back to '0'.

GEN_AUTO

The Generator Autonomous Mode (GEN_AUTO) bit places the Generator in the Autonomous Input Mode. In this mode the payload frame is forced to an active offset of zero. The generated frame will have all-zeros TOH and POH bytes. The H1, H2 pointer bytes are set to indicate an active SPE/VC offset of zero and the payload will be filled with a PRBS. When a logic zero is written to this bit, the active offset is determined by the received stream.

When all 12 slices are in autonomous mode, and only then, the ATSI bits in the Add Bus Configuration register (1030H) can be used for situations where the Add bus does not provide a valid frame pulse.

GEN_INV_PRBS

The Generator Invert PRBS (GEN_INV_PRBS) bit is used to invert the calculated PRBS byte before insertion into the payload. Setting this bit to logic one enables the logic inversion of all PRBS bits before insertion into the payload. Setting this bit to logic zero does not invert the generated PRBS.

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA 4x155.

Registers 11F1H, 12F1H, 13F1H, 14F1H, 15F1H, 16F1H, 17F1H, 18F1H, 19F1H, 1AF1H, 1BF1H, and 1CF1H: APGM Generator Control #2

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

Reserved

The Reserved bits must be set low for proper operation of the SPECTRA-4X155.

Registers 11F2H, 12F2H, 13F2H, 14F2H, 15F2H, 16F2H, 17F2H, 18F2H, 19F2H, 1AF2H, 1BF2H, and 1CF2H: APGM Generator Concatenate Control

Bit	Type	Function	Default
Bit 7	—	Unused	0
Bit 6	—	Unused	0
Bit 5	R/W	GEN_SEQ[3]	1
Bit 4	R/W	GEN_SEQ[2]	1
Bit 3	R/W	GEN_SEQ[1]	1
Bit 2	R/W	GEN_SEQ[0]	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	GEN_GMODE	0

GEN_GMODE

The GEN_GMODE bit controls the operational mode of the pseudo random sequence generator as summarized in the table below. When GEN_GMODE is set to 0, the generator will generate the complete sequence for an STS-1 (STM-0/AU-3) stream. When GEN_GMODE is set to logic one, the generator will generate one third or one in three bytes of the complete sequence for an STS-1 (STM-0/AU-3) equivalent in an STS-3c (STM-1/AU-4) stream.

GEN_GMODE	Generator Gap Mode Description
0	1in1 Gap Mode. Generator inserts the complete PRBS.
1	1in3 Gap Mode. Generator generates 1 of 3 (1in3) PRBS bytes. The generator will also generate 1in2 bytes to skip over path overhead columns.

GEN_SEQ[3:0]

The Generator Sequence (GEN_SEQ[3:0]) sets the reset state of the LFSR and places the generator in the master or slave mode. The sequence number identifies the multiplexing order of the outgoing data into the concatenating stream. The sequence number also affects the signature bit calculation.

GEN_SEQ [3:0]	Mode	Signature bit	Reset Value
0000	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.	All-ones.
0001	Slave1	88th PRBS bit from current state. MSB of 11th PRBS byte.	Master+8 states
0010	Slave2	80th PRBS bit from current state. MSB of 10th PRBS byte.	Master+16 states
0011-1110	Reserved	N/A	
1111	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.	All-ones.

Registers 11F3H, 12F3H, 13F3H, 14F3H, 15F3H, 16F3H, 17F3H, 18F3H, 19F3H, 1AF3H, 1BF3H, and 1CF3H: APGM Generator Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	Unused	X
Bit 3	R	Unused	X
Bit 2	R	Unused	X
Bit 1	R	GEN_SIGI	X
Bit 0	R	GEN_SIGV	X

GEN_SIGV

The Generator Signature Status (GEN_SIGV) bit indicates if the partial PRBS being generated is correctly aligned with the partial PRBS begin generated in the master generator. When GEN_SIGV is low, the signature verification is a match, and the partial PRBS is aligned with that of the master. When GEN_SIGV is high, the signature verification is a mismatch, and the partial PRBS is not aligned with that of the master.

If non-alignment persists, a forced re-start of the sequence generation by all generators processing the concatenated stream should be initiated using the GEN_REGEN register bit in the master generator. This bit is only valid in slave generators and when out of alignment may toggle high and low. Persistent reads at low or reading the interrupt at low assures that the signature is correct.

GEN_SIGI

The Generator Signature Interrupt Status (GEN_SIGI) bit indicates a change in the signature verification state (GEN_SIGV) by a slave generator. When GEN_SIGI is set high, the slave generator has either transition from the signature match state to the signature mismatch state or vice versa. This bit is cleared when this register is read. This bit will continuously be set when in the out of alignment state since the status GEN_SIGV will toggle. This bit is only valid in slave generators.

Registers 11F8H, 12F8H, 13F8H, 14F8H, 15F8H, 16F8H, 17F8H, 18F8H, 19F8H, 1AF8H, 1BF8H, and 1CF8H: APGM Monitor Control #1

Bit	Type	Function	Default
Bit 7	R/W	MON_AUTORESYNC	1
Bit 6	R/W	MON_INV_PRBS	0
Bit 5	R/W	MON_SYNCE	X
Bit 4	R/W	MON_ERRE	0
Bit 3	R/W	MON_FSENB	0
Bit 2	R/W	MON_SIGE	0
Bit 1	R/W	MON_RESYNC	0
Bit 0	R/W	MON_EN	0

MON_EN

The Monitor Enable (MON_EN) bit enables the monitoring of a PRBS in the processed payload. When MON_EN is set high, the incoming payload is extracted and the data monitored for the PRBS. When MON_EN is set low, no monitoring on the data is done.

MON_RESYNC

The Monitor Resynchronize (MON_RESYNC) bit allows a forced resynchronization of the monitor to the incoming PRBS. When set to logic one, the monitor's will go out of synchronization and begin re-synchronizing the to the incoming PRBS payload. Setting this bit in a master monitor will automatically force all slaves to re-synchronize at the same time. This register bit will clear itself when the re-synchronizing has been triggered.

MON_FSENB

The Monitor Fixed Stuff Enable (MON_FSENB) bit determines whether a PRBS is monitored for in the fixed stuff columns (columns 30 and 59) of the processed payload. When logic one is written to this bit, the PRBS is not monitored for in the fixed stuff columns. When a logic zero is written to this bit, the PRBS is monitored for in the fixed stuff columns. MON_FSENB should be disabled when using the monitor in master/slave configuration to support de-multiplexed concatenated payloads.

MON_SIGE

The Monitor Signature Interrupt Enable (MON_SIGE) bit allows an interrupt to be asserted on INT when a signature verification mismatch occurs. When MON_SIGE is set high, a change in the signature verification state (MON_SIGV) will trigger an interrupt. When MON_SIGE is set low, no interrupt is reported. Note: This bit is ignored in a master APGM.

MON_ERRE

The Monitor Byte Error Interrupt Enable (MON_ERRE) bit allows an interrupt to be asserted on INT when a PRBS byte error has been detected in the incoming payload. When MON_ERRE is set high, a detected PRBS error in the incoming data will trigger an interrupt. When MON_ERRE is set low, no interrupt is generated.

MON_SYNCE

The Monitor Synchronize Interrupt Enable (MON_ERRE) bit allows an interrupt to be asserted on INT when change in the synchronization state of the monitor occurs. When MON_SYNCE is set high, a change in the synchronization state (MON_SYNCV) will trigger an interrupt. When MON_SYNCE is set low, no interrupt is generated.

MON_INV_PRBS

The Monitor Invert PRBS (MON_INV_PRBS) bit is used to invert the received payload data before monitoring the data for a pseudo random bit sequence (PRBS). When set to logic one, the incoming payload PRBS bits are inverted before being verified against the monitor expected PRBS. When set to logic zero, the incoming payload PRBS bits are not inverted and verified as is.

MON_AUTORESYNC

The Monitor Automatic Resynchronization (MON_AUTORESYNC) bit enables the automatic resynchronization of the monitor after detecting 16 consecutive PRBS byte errors. Setting this bit to logic one, enables the monitor to automatically fall out of synchronization after 16 consecutive errors. Once out of synchronization, the monitor will attempt to resynchronize to the incoming PRBS and verify the synchronization with 32 consecutive PRBS matches. Setting this bit to logic zero disables the automatic resynchronization

Registers 11F9H, 12F9H, 13F9H, 14F9H, 15F9H, 16F9H, 17F9H, 18F9H, 19F9H, 1AF9H, 1BF9H, and 1CF9H: APGM Monitor Control #2

Bit	Type	Function	Default
Bit 7	R/W	Unused	0
Bit 6	R/W	Unused	0
Bit 5	R/W	Unused	0
Bit 4	R/W	Unused	0
Bit 3	R/W	Unused	0
Bit 2	R/W	Unused	0
Bit 1	R/W	Unused	0
Bit 0	R/W	MON_V1_DIS	0

MON_V1_DIS

The Monitor Input V1 Pulse disable (GEN_V1_DIS) bit is used to disable the V1 masking algorithm on the input C1/J1/V1 control signal. Setting this bit to logic zero allows the monitor to ignore V1 pulses. Setting this bit to logic one disables the V1 masking and no input V1 pulse is assumed present on the input interface. When disabled, on a C1 and J1 pulse is assumed received on the input interface.

Registers 11FAH, 12FAH, 13FAH, 14FAH, 15FAH, 16FAH, 17FAH, 18FAH, 19FAH, 1AFAH, 1BFAH, 1CFAH:APGM Monitor Concatenate Control

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	R/W	MON_SEQ[3]	1
Bit 4	R/W	MON_SEQ[2]	1
Bit 3	R/W	MON_SEQ[1]	1
Bit 2	R/W	MON_SEQ[0]	1
Bit 1	R/W	MON_GMODE[1]	1
Bit 0	R/W	MON_GMODE[0]	1

MON_GMODE

The MON_GMODE bit controls the operational mode of the pseudo random sequence monitor as summarized in the table below. When MON_GMODE[1:0] is set to ”00”, the monitor expects the complete sequence for an STS-1 (STM-0/AU-3) stream. When MON_GMODE[1:0] is set to ”01”, the monitor expects one third or one in three bytes of the complete sequence in an STS-1 (STM-0/AU-3) equivalent of an STS-3c (STM-1/AU-4) stream.

MON_GMODE [1:0]	Monitor Gap Mode Description
00	1in1 Gap Mode. Monitor monitors for a complete PRBS.
01	1in3 Gap Mode. Monitor will monitor for the presence of every 3rd PRBS byte. The Monitor will also monitor for every 2nd PRBS byte after the POH columns.
10	Reserved
11	Reserved

MON_SEQ[3:0]

The Monitor Sequence (MON_SEQ[3:0]) sets the Monitor in master or slave mode and is used to identify the multiplexed order of the monitored data in the concatenated payload. The sequence order affects the signature bit calculation.

MON_SEQ [3:0]	Mode	Signature bit
0000	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.
0001	Slave1	88th PRBS bit from current state. MSB of 11th PRBS byte.
0010	Slave2	80th PRBS bit from current state. MSB of 10th PRBS byte.
0011-1110	Reserved	—
1111	Master	96th PRBS bit from current state. MSB of 12th PRBS byte.

Registers 11FBH, 12FBH, 13FBH, 14FBH, 15FBH, 16FBH, 17FBH, 18FBH, 19FBH, 1AFBH, 1BFBH, 1CFBH:APGM Monitor Status

Bit	Type	Function	Default
Bit 7	R	Unused	X
Bit 6	R	Unused	X
Bit 5	R	Unused	X
Bit 4	R	MON_ERRI	X
Bit 3	R	MON_SYNCI	X
Bit 2	R	MON_SYNCV	X
Bit 1	R	MONS_SIGI	X
Bit 0	R	MONS_SIGV	X

MON_SIGV

The Monitor Signature Status (MON_SIGV) bit indicates if the partial PRBS being monitored for is correctly aligned with the partial PRBS begin monitored for by the master generator. When MON_SIGV is low, the signature verification is a match, and the calculated partial PRBS is aligned with that of the master. When MON_SIGV is high, the signature verification is a mismatch, and the calculated partial PRBS is not aligned with that of the master.

If non-alignment persists, a forced re-synchronization of all monitors processing the concatenated stream should be initiated using the MON_RESYNC register bit in the master generator. This bit is only valid in slave generators.

MON_SIGI

The Monitor Signature Interrupt Status (MON_SIGI) bit indicates a change in the signature verification state (MON_SIGV) by a slave monitor. When MON_SIGI is set high, the Monitor has either transition from the signature match state to the signature mismatch state or vice versa. This bit is cleared when this register is read. This bit is only valid in slave monitor.

MON_SYNCV

The Monitor Synchronize Status (MON_SYNCV) is set high when the monitor is out of synchronization. The monitor falls out of synchronization after detecting 16 consecutive mismatched PRBS bytes or being forced to re-synchronize. A forced re-synchronize may be due to setting the MON_RESYNC register bit or a master generator. Once out of synchronization, the Synchronized State can only be achieved after re-synchronizing to the incoming PRBS and verifying the resynchronization with 32 consecutive non-erred PRBS bytes. This bit is set low when in the Synchronized State.

MON_SYNCI

The Monitor Synchronize Interrupt Status (MON_SYNCI) bit indicates a change in the synchronization state (MON_SYNCV) of the monitor. When MON_SYNCI is set high, the monitor has transitioned from the Synchronized to Out of Synchronization State or vice versa. This bit is cleared when this register is read.

MON_ERRI

The Monitor Byte Error Interrupt Status (MON_ERRI) bit indicates that an error has been detected in the received PRBS byte while the monitor was in the Synchronized State. MON_ERRI is set high, when one or more PRBS bit errors have been detected in the received PRBS data byte. This bit is cleared when this register is read.

Registers 11FCH, 12FCH, 13FCH, 14FCH, 15FCH, 16FCH, 17FCH, 18FCH, 19FCH, 1AFCH, 1BFCH, and 1CFCH: APGM Monitor Error Count #1

Bit	Type	Function	Default
Bit 7	R	PRSE[7]	X
Bit 6	R	PRSE[6]	X
Bit 5	R	PRSE[5]	X
Bit 4	R	PRSE[4]	X
Bit 3	R	PRSE[3]	X
Bit 2	R	PRSE[2]	X
Bit 1	R	PRSE[1]	X
Bit 0	R	PRSE[0]	X

Registers 11FDH, 12FDH, 13FDH, 14FDH, 15FDH, 16FDH, 17FDH, 18FDH, 19FDH, 1AFDH, 1BFDH, 1CFDH:APGM Monitor Error Count #2

Bit	Type	Function	Default
Bit 7	R	PRSE[15]	X
Bit 6	R	PRSE[14]	X
Bit 5	R	PRSE[13]	X
Bit 4	R	PRSE[12]	X
Bit 3	R	PRSE[11]	X
Bit 2	R	PRSE[10]	X
Bit 1	R	PRSE[9]	X
Bit 0	R	PRSE[8]	X

PRSE[15:0]

The PRSE[15:0] bits represent the number of PRBS byte errors detected since the last accumulation interval. Errors are only accumulated in the synchronized state and each PRBS data byte can only have one error. The transfer of the error accumulation counter to these registers is triggered by a write to either of the GPGM Monitor Error Counters and the contents of these registers will be valid only four clock cycles after the transfer is triggered.

12 Test Features Description

The test mode registers are used for production and board testing.

During production testing, the test mode registers are used to apply test vectors. In this case, the test mode registers (as opposed to the normal mode registers) are selected when A[13] is high.

During board testing, the digital output pins and the data bus are held in a high-impedance state by simultaneously asserting (low) the CSB, RDB, and WRB inputs. All of the TSBs for the SPECTRA 4x155 are placed in test mode 0 so that device inputs may be read and device outputs may be forced through the microprocessor interface. Refer to the section "Test Mode "0" for details.

Note: The SPECTRA 4x155 supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port that can be used for board testing. All digital device inputs may be read and all digital device outputs may be forced through this JTAG test port.

Table 16 Test Mode Register Memory Map

Address	Register
0000H-1FFFH	Normal Mode Registers
2000H	Master Test Register
2001H	Master Test Slice Select
2000H-3FFFH	Reserved For Test

12.1 Master Test and Test Configuration Registers

Notes on Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2. Writeable register bits are not initialized upon reset unless otherwise noted.

Register 2000H: Master Test

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	X
Bit 5	R/W	PMCATST	X
Bit 4	R/W	PMCTST	X
Bit 3	R/W	DBCTRL	X
Bit 2	R/W	Reserved	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable SPECTRA 4x155 test features. All bits, except PMCTST and PMCATST, are reset to zero by a reset of the SPECTRA 4x155 using either the RSTB input or the Master Reset register. PMCTST and BYPASS are reset when CSB is logic one. PMCATST is reset when both CSB is high and RSTB is low. PMCTST and PMCATST can also be reset by writing a logic zero to the corresponding register bit.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the SPECTRA 4x155. While the HIZIO bit is a logic one, all output pins of the SPECTRA 4x155 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state that inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

RESERVED

The Reserved bit must always be written to zero.

DBCTRL

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and either IOTST or PMCTST are logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the SPECTRA 4x155 to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST

The PMCTST bit is used to configure the SPECTRA 4x155 for PMC-Sierra's manufacturing tests. When PMCTST is set to logic one, the SPECTRA 4x155 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST

The PMCATST bit is used to configure the analog portion of the SPECTRA 4x155 for PMC-Sierra's manufacturing tests.

Register Address 2001H: Master Test Slice Select

Bit	Type	Function	Default
Bit 7	—	Unused	X
Bit 6	—	Unused	X
Bit 5	—	Unused	X
Bit 4	—	Unused	X
Bit 3	R/W	TSTADDSEL[3]	0
Bit 2	R/W	TSTADDSEL[2]	0
Bit 1	R/W	TSTADDSEL[1]	0
Bit 0	R/W	TSTADDSEL[0]	0

TSTADDSEL[3:0]

The test address select (TSTADDSEL[3:0) bits control the addressing range of the CBI when accessing registers and TSBs in the transmit/receive transport blocks and the RPPSs blocks and TPPSs blocks when the PMCTST or the IOTST bit in the SPECTRA 4x155 Master Test register is set high. The code-points of TSTADDSEL[3:0] are summarized in Table 17 and Table 18.

When TSTADDSEL[3:0] is set to 0H, the selection among the registers and TSBs is directly controlled by the address bus A[13:0]. When TSTADDSEL[3:0] is set to 1H – CH, register and TSB selection is a combination of the address bus and the TSTADDSEL[3:0] values. The TSTADDSEL[3:0] value will then replace the value of the A[11:8] bits of the address bus. The TSTADDSEL[3:0] bits are cleared by setting CSB to logic one or writing all-zeros in the register.

Table 17 TSTADDSEL[3:0] Codepoints When Addressing Transport Channels.

TSTADDSEL[3:0]	Receive Channel #	Transmit Channel #
0H	—	—
1H	1	1
2H	2	2
3H	3	3
4H	4	4
5H-FH	Reserved	Reserved

Table 18 TSTADDSEL[3:0] Codepoints When Address RPPS/TPPS Slices

TSTADDSEL[3:0]	RPPS #	TPPS #
0H	—	—
1H	1	1
2H	2	2
3H	3	3

TSTADDSEL[3:0]	RPPS #	TPPS #
4H	4	4
5H	5	5
6H	6	6
7H	7	7
8H	8	8
9H	9	9
AH	10	10
BH	11	11
CH	12	12
DH-FH	Reserved	Reserved

12.2 JTAG Test Port

The SPECTRA 4x155 JTAG Test Access Port (TAP) allows access to the TAP controller and the four TAP registers: instruction, bypass, device identification, and boundary scan. Using the TAP, the device input logic levels can be read, the device outputs can be forced, the device can be identified, and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 19 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 20 Identification Register

Length	32 bits
Version number	0H
Part Number	5316H
Manufacturer's identification code	0CDH
Device identification	053160CDH

Table 21 Boundary Scan Register

Name	Register Bit	Cell Type	Name	Register Bit	Cell Type
hiz	238	IN_CELL	ac1j1v1_afp[2]	119	IN_CELL

Name	Register Bit	Cell Type	Name	Register Bit	Cell Type
pad_rsld1_oenb	237	IN_CELL	ad[8]	118	IN_CELL
pad_tsld1_oenb	236	IN_CELL	dd[3]	117	OUT_CELL
pad_rsld2_oenb	235	IN_CELL	ad[9]	116	IN_CELL
pad_tsld2_oenb	234	IN_CELL	dd[4]	115	OUT_CELL
pad_rsld3_oenb	233	IN_CELL	dd[5]	114	OUT_CELL
pad_tsld3_oenb	232	IN_CELL	dd[6]	113	OUT_CELL
pad_rsld4_oenb	231	IN_CELL	dpl[1]	112	OUT_CELL
pad_tsld4_oenb	230	IN_CELL	dd[7]	111	OUT_CELL
rtohfp[1]	229	OUT_CELL	dc1j1v1[1]	110	OUT_CELL
rtohclk[1	228	OUT_CELL	dd[0]	109	OUT_CELL
rtoh[1]	227	OUT_CELL	dd[1]	108	OUT_CELL
ttohclk[1]	226	OUT_CELL	ad[5]	107	IN_CELL
ttohfp[1]	225	OUT_CELL	dd[2]	106	OUT_CELL
ttohen[1]	224	IN_CELL	ad[6]	105	IN_CELL
ttoh[1]	223	IN_CELL	ad[7]	104	IN_CELL
rtohfp[2]	222	OUT_CELL	adp[1]	103	IN_CELL
rtohclk[2]	221	OUT_CELL	ad[1]	102	IN_CELL
rtoh[2]	220	OUT_CELL	ad[2]	101	IN_CELL
ttohclk[2]	219	OUT_CELL	ack	100	IN_CELL
ttohfp[2]	218	OUT_CELL	ad[3]	99	IN_CELL
ttohen[2]	217	IN_CELL	apl[1]	98	IN_CELL
ttoh[2]	216	IN_CELL	ad[4]	97	IN_CELL
rtohfp[3]	215	OUT_CELL	ac1j1v1_afp[1]	96	IN_CELL
rtohclk[3]	214	OUT_CELL	ad[0]	95	IN_CELL
rtoh[3]	213	OUT_CELL	pad_d_oenb	94	IN_CELL
ttohclk[3]	212	OUT_CELL	dpaisck	93	IN_CELL
ttohfp[3]	211	OUT_CELL	dpaisfp	92	IN_CELL
ttohen[3]	210	IN_CELL	dpais	91	IN_CELL
ttoh[3]	209	IN_CELL	tpaisck	90	IN_CELL
rtohfp[4]	208	OUT_CELL	tpaisfp	89	IN_CELL
rtohclk[4]	207	OUT_CELL	tpais	88	IN_CELL
rtoh[4]	206	OUT_CELL	rpohclk	87	OUT_CELL
ttohclk[4]	205	OUT_CELL	rpohfp	86	OUT_CELL
ttohfp[4]	204	OUT_CELL	rpoh	85	OUT_CELL
ttohen[4]	203	IN_CELL	rpohen	84	OUT_CELL
ttoh[4]	202	IN_CELL	Reserved1	83	OUT_CELL
rsldclk[1]	201	OUT_CELL	Reserved2	82	OUT_CELL
rsld[1]	200	OUT_CELL	Reserved5	81	OUT_CELL
tsldclk[1]	199	OUT_CELL	Reserved4	80	IN_CELL

Name	Register Bit	Cell Type	Name	Register Bit	Cell Type
tsld[1]	198	IN_CELL	Reserved3	79	IN_CELL
rsldclk[2]	197	OUT_CELL	rtcen	78	IN_CELL
rsld[2]	196	OUT_CELL	rtcoh	77	IN_CELL
tsldclk[2]	195	OUT_CELL	tafp	76	IN_CELL
tsld[2]	194	IN_CELL	tack	75	IN_CELL
rsldclk[3]	193	OUT_CELL	tad	74	IN_CELL
rsld[3]	192	OUT_CELL	rad	73	OUT_CELL
tsldclk[3]	191	OUT_CELL	lof[1]	72	OUT_CELL
tsld[3]	190	IN_CELL	lof[2]	71	OUT_CELL
rsldclk[4]	189	OUT_CELL	lof[3]	70	OUT_CELL
rsld[4]	188	OUT_CELL	lof[4]	69	OUT_CELL
tsldclk[4]	187	OUT_CELL	b3e	68	OUT_CELL
tsld[4]	186	IN_CELL	ralm	67	OUT_CELL
dck	185	IN_CELL	d[7]	66	IO_CELL
dfp	184	IN_CELL	d[6]	65	IO_CELL
ddp[4]	183	OUT_CELL	d[5]	64	IO_CELL
dd[31]	182	OUT_CELL	d[4]	63	IO_CELL
dd[30]	181	OUT_CELL	d[3]	62	IO_CELL
dd[28]	180	OUT_CELL	d[2]	61	IO_CELL
dd[29]	179	OUT_CELL	d[1]	60	IO_CELL
dd[27]	178	OUT_CELL	d[0]	59	IO_CELL
dd[26]	177	OUT_CELL	intb	58	OUT_CELL
dd[25]	176	OUT_CELL	a[13]	57	IN_CELL
dc1j1v1[4]	175	OUT_CELL	a[11]	56	IN_CELL
dd[24]	174	OUT_CELL	a[12]	55	IN_CELL
dpl[4]	173	OUT_CELL	a[10]	54	IN_CELL
adp[4]	172	IN_CELL	a[9]	53	IN_CELL
ad[31]	171	IN_CELL	a[8]	52	IN_CELL
ad[30]	170	IN_CELL	a[7]	51	IN_CELL
ad[29]	169	IN_CELL	a[6]	50	IN_CELL
ad[28]	168	IN_CELL	a[5]	49	IN_CELL
ad[26]	167	IN_CELL	a[4]	48	IN_CELL
ad[27]	166	IN_CELL	a[3]	47	IN_CELL
ad[25]	165	IN_CELL	a[1]	46	IN_CELL
ad[24]	164	IN_CELL	a[2]	45	IN_CELL
ac1j1v1_afp[4]	163	IN_CELL	a[0]	44	IN_CELL
apl[4]	162	IN_CELL	csb	43	IN_CELL
ddp[3]	161	OUT_CELL	ale	42	IN_CELL
dd[23]	160	OUT_CELL	rdb_e	41	IN_CELL

Name	Register Bit	Cell Type	Name	Register Bit	Cell Type
dd[22]	159	OUT_CELL	mbeb	40	IN_CELL
dd[21]	158	OUT_CELL	wrb_rwb	39	IN_CELL
dd[20]	157	OUT_CELL	rstb	38	IN_CELL
dd[19]	156	OUT_CELL	salm[1]	37	OUT_CELL
dd[18]	155	OUT_CELL	salm[2]	36	OUT_CELL
dd[17]	154	OUT_CELL	salm[3]	35	OUT_CELL
dd[16]	153	OUT_CELL	salm[4]	34	OUT_CELL
dc1j1v1[3]	152	OUT_CELL	los_rrcpfp[1]	33	OUT_CELL
dpl[3]	151	OUT_CELL	lrdi_rrcpclk[1]	32	OUT_CELL
adp[3]	150	IN_CELL	lais_rrcpdat[1]	31	OUT_CELL
ad[23]	149	IN_CELL	los_rrcpfp[2]	30	OUT_CELL
ad[22]	148	IN_CELL	lrdi_rrcpclk[2]	29	OUT_CELL
ad[21]	147	IN_CELL	lais_rrcpdat[2]	28	OUT_CELL
ad[20]	146	IN_CELL	los_rrcpfp[3]	27	OUT_CELL
ad[19]	145	IN_CELL	lrdi_rrcpclk[3]	26	OUT_CELL
ad[18]	144	IN_CELL	lais_rrcpdat[3]	25	OUT_CELL
ad[17]	143	IN_CELL	los_rrcpfp[4]	24	OUT_CELL
ad[16]	142	IN_CELL	lrdi_rrcpclk[4]	23	OUT_CELL
ac1j1v1_afp[3]	141	IN_CELL	lais_rrcpdat[4]	22	OUT_CELL
apl[3]	140	IN_CELL	rlais_trcpclk[1]	21	IN_CELL
ddp[2]	139	OUT_CELL	tlrdi_trcpfp[1]	20	IN_CELL
dd[11]	138	OUT_CELL	tlais_trcpdat[1]	19	IN_CELL
dd[12]	137	OUT_CELL	rlais_trcpclk[2]	18	IN_CELL
dd[13]	136	OUT_CELL	tlrdi_trcpfp[2]	17	IN_CELL
dd[14]	135	OUT_CELL	tlais_trcpdat[2]	16	IN_CELL
dd[15]	134	OUT_CELL	rlais_trcpclk[3]	15	IN_CELL
dpl[2]	133	OUT_CELL	tlrdi_trcpfp[3]	14	IN_CELL
dc1j1v1[2]	132	OUT_CELL	tlais_trcpdat[3]	13	IN_CELL
dd[8]	131	OUT_CELL	rlais_trcpclk[4]	12	IN_CELL
dd[9]	130	OUT_CELL	tlrdi_trcpfp[4]	11	IN_CELL
dd[10]	129	OUT_CELL	tlais_trcpdat[4]	10	IN_CELL
ad[13]	128	IN_CELL	rclk[1]	9	OUT_CELL
ad[14]	127	IN_CELL	rclk[2]	8	OUT_CELL
ad[15]	126	IN_CELL	rclk[3]	7	OUT_CELL
Adp[2]	125	IN_CELL	rclk[4]	6	OUT_CELL
ad[10]	124	IN_CELL	tclk	5	OUT_CELL
ad[11]	123	IN_CELL	pgmrclk	4	OUT_CELL
ad[12]	122	IN_CELL	pgmtclk	3	OUT_CELL
ddp[1]	121	OUT_CELL	refclk	2	IN_CELL

Name	Register Bit	Cell Type	Name	Register Bit	Cell Type
apl[2]	120	IN_CELL	peclv	1	IN_CELL

Notes

1. Pad_b_oenb is the active low output enable for D[7:0]. When set high, INTB will be set to high impedance.
2. HIZ is the active low output enable for all OUT_CELL types except D[7:0] and INTB.
3. Pad_rsld1_oenb is the active low output enable for RSLD1 and RSLDCLK1.
4. Pad_rsld2_oenb is the active low output enable for RSLD2 and RSLDCLK2.
5. Pad_rsld3_oenb is the active low output enable for RSLD3 and RSLDCLK3.
6. Pad_rsld4_oenb is the active low output enable for RSLD4 and RSLDCLK4.
7. Pad_tsld1_oenb is the active low output enable for TSLDCLK1.
8. Pad_tsld2_oenb is the active low output enable for TSLDCLK2.
9. Pad_tsld3_oenb is the active low output enable for TSLDCLK3.
10. Pad_tsld4_oenb is the active low output enable for TSLDCLK4.
11. Peclv is the first bit of the boundary scan chain (first output of TDO). When set high, INTB will be high impedance.

12.2.1 Boundary Scan Cells

In Figure 10, Figure 11, Figure 12, and Figure 13, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer shown in the center of each figure selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table, Table 21

Figure 10 Input Observation Cell (IN_CELL)

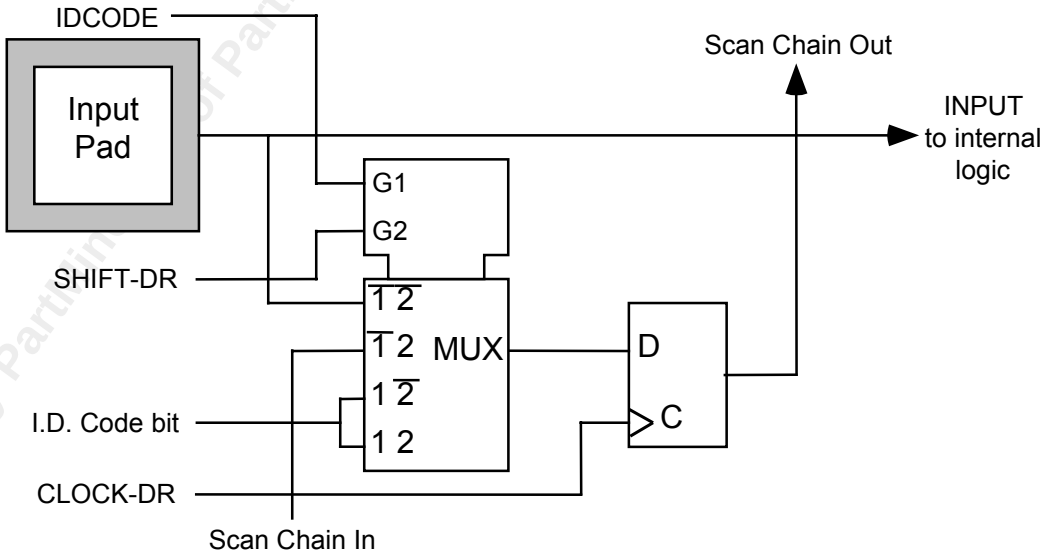


Figure 11 Output Cell (OUT_CELL)

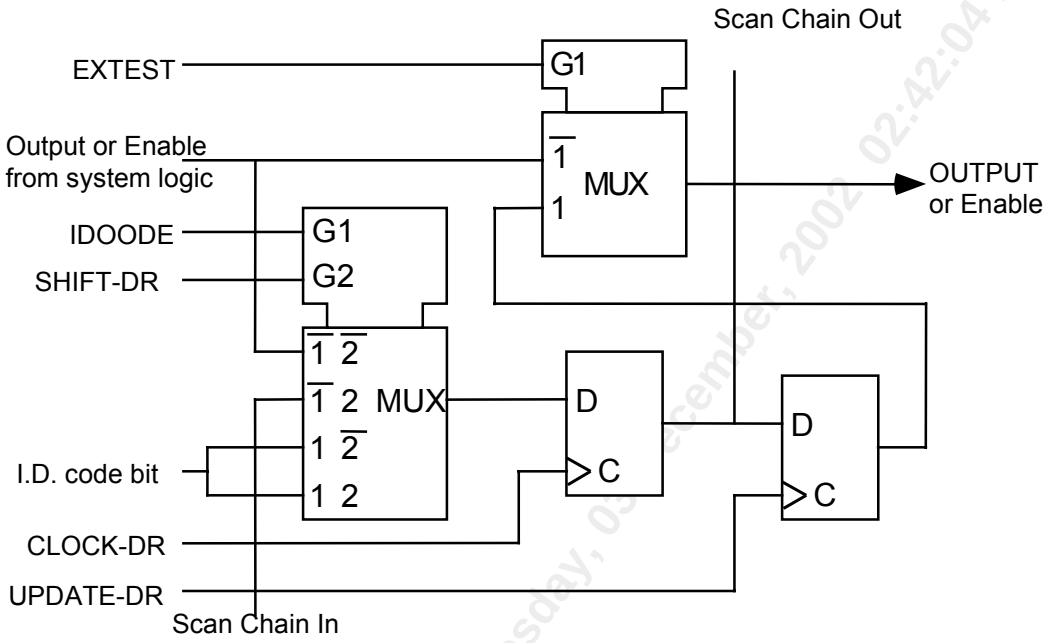


Figure 12 Bi-directional Cell (IO_CELL)

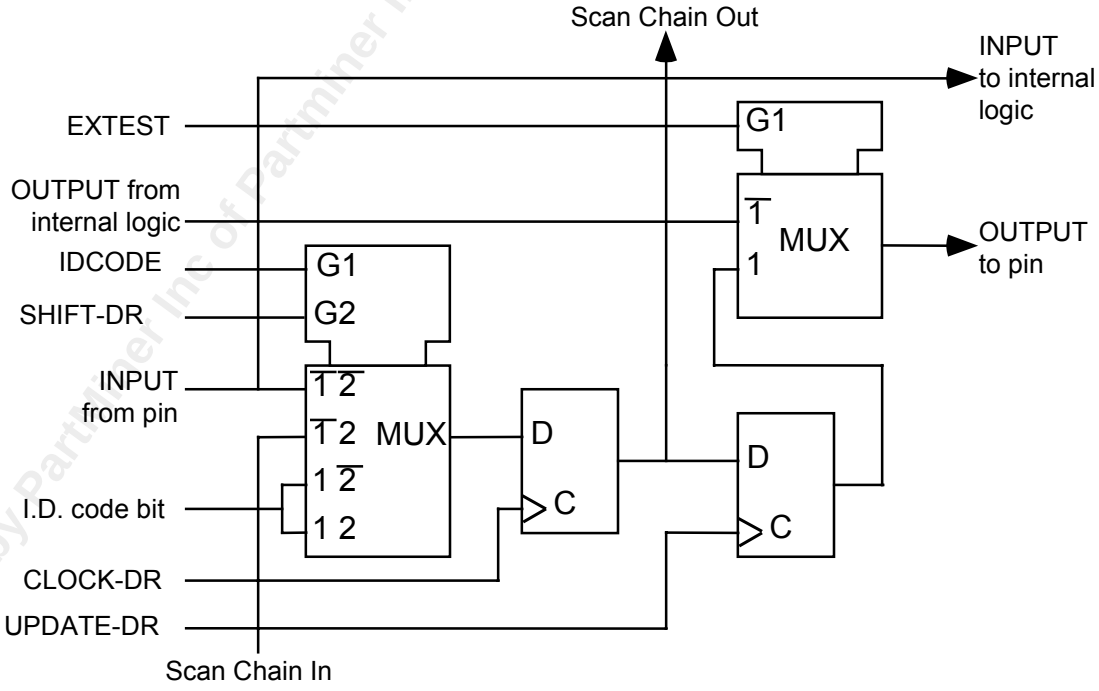
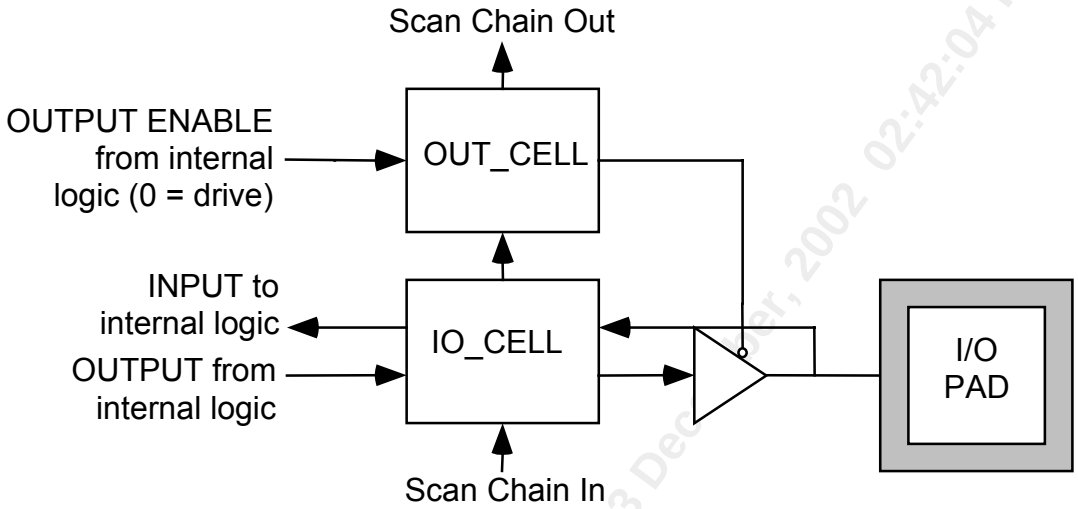


Figure 13 Layout of Output Enable and Bi-directional Cells



13 Operation

The SPECTRA 4x155 supports a rich set of line, path, and system configuration options. This section details these configuration options, PCB design recommendations, operating details for the JTAG boundary scan feature, and interface details for system side devices.

13.1 Software Initialization Sequence

If no other registers are programmed, the device will start in the following mode. All slice will be in master mode, i.e. twelve STS-1. The ADD and DROP bus will be running in the 19.44 MHz interface mode. The DROP bus will be supplying C1, J1 pulses along with a valid payload indicator. The ADD bus will be expecting a C1 and J1 pulses along with a payload indicating signal. Pointer interpretation on the ADD bus will be disabled.

Only one access is needed for proper operation of the device after power-up or global reset, the DROP bus DLL must be disabled. The DLL is not needed in 19.44 MHz mode.

13.1.1 RTAL & TTAL Elastic Store FIFO Initialization Procedure

To ensure that the Elastic Store FIFO in the RTAL or TTAL blocks come out of a hardware or software reset in proper working state, the following procedure should be included in the device initialization routine:

1. Program the DOPJ[1:0] bits to '11' in the RTAL Interrupt Status and Control register 1n59h (n from 1 to C). Program reserved[7:6] bits to ‘11’ in the TTAL Interrupt Status and Control register 1nD1h (n from 1 to C).

2. Wait at least 7 µs.

3. Program the DOPJ[1:0] bits to '00' in the RTAL Interrupt Status and Control registers; 1n59h (n from 1 to C). Program reserved[7:6] bits to ‘00’ in the TTAL Interrupt Status and Control registers; 1nD1h (n from 1 to C).

4. Wait at least 7 µs.

5. Read the ESEI bit in the RTAL and TTAL Interrupt Status and Control registers; RTAL 1n59h (n from 1 to C) and TTAL Interrupt Status and Control registers; 1nD1h (n from 1 to C) to clear previous false alarm, if exists.

6. Wait at least 14 µs.

7. Read the ESEI bit in the RTAL and TTAL Interrupt Status and Control registers; RTAL 1n59h (n from 1 to C) and TTAL Interrupt Status and Control registers; 1nD1h (n from 1 to C). Repeat steps 1 through 7, if ESEI is 1, otherwise exit.

8. Note: For STS-3c/AU-4 mode, you just need to do the work-around for master slices only. This would be the first STS-1/AU path for each STS-3c/AU-4 as follows:

9. TTAL: 11D1h to 14D1h

10. RTAL: 1159h to 1459h

Please note that if ESEI remains high continuously after the above initialization procedure, check that there are no board-level problems with the Telecom bus signals generated externally to SPECTRA 4x155. If the external system is generating Telecom bus inputs for SPECTRA 4x155 that are incorrect, the ESEI bit in the RTAL or TTAL will be set high continuously and data will be corrupted. When these symptoms are the result of incorrect input signals from the external system, resetting the internal FIFO will not solve the problem.

Users, who see these symptoms very frequently, particularly while a board is being debugged, should first verify that all Telecom bus input signals meet the specified timing requirements. This includes confirming that the ACK and DCK clocks are the proper frequency and that the AC1J1V1, APL, and DFP input signals are correct according to the specifications in the data sheet.

13.2 SONET/SDH Overhead Byte Processing

13.2.1 Transport Overhead Bytes

Under normal operating conditions, the SPECTRA 4x155 processes the complete transport overhead present in an STS-3/3c/STM-1 stream. All overhead bytes are extracted onto the RTOH port and can be inserted into the transmit stream via the TTOH port.

The TTOC block has higher priority over any other block for TOH insertion. Within the TTOC, the TTOC block applies the following priorities with respect to the TOH insertion functions it has.

TTOC Line Overhead Priority (highest priority first)

- UNUSED_EN register bit has precedence above all, to insert all ones or all zeros into the unused line overhead bytes.
- NAT_EN register bit has precedence above all except UNUSED_EN, to insert all ones or all zeros into the section growth (Z0) and line orderwire byte (E2) of STS-1's #2 to #3.
- Line overhead bytes supplied via TTOH, with TTOHEN set high during bit 7 of the serial byte on TTOH will have priority over the TSLD inputs and the ZOINS and Z1/S1 registers.
- Passing through input overhead bytes not altered by any of the above.

TTOC Section Overhead Priority (highest priority first)

- The Z0INS register bit has precedence above all for the Z0 bytes.
- NAT_EN register bit has precedence above all except ZOINS, to insert all ones or all zeros into the section growth (Z0) and line orderwire byte (E2) of STS-1's #2 to #3.
- NAT_EN register bit has precedence above all to insert all ones or all zeros into the section user channel byte (F1) of STS-1's #2 to #3. The F1 byte of STS-1 #1 is not included in the NAT_EN definition.

- UNUSED_EN register bit has precedence above all to insert all ones or all zeros into the unused section overhead bytes.
- TREN register bit has precedence over the TTOH and TTOHEN for the insertion of the section trace (J0) overhead byte.
- TAPS_SEL register bit has precedence over the TTOH and TTOHEN for the insertion of the APS (K1/K2) overhead bytes.
- Section overhead bytes supplied via TTOH, with TTOHEN set high during bit 7 of the serial byte on TTOH will have priority over the TSLD input.
- TSLD when carrying the section DCC will have priority over TSLD_VAL register bit.
- Passing through input overhead bytes not altered by any of the above.

Table 22 contains the list of SONET/SDH transport overhead bytes and the various features of the SPECTRA 4x155 which can be used to modify or extract the bytes in the transmit or receive stream respectively.

Table 22 Transport Overhead Bytes

A1, A2:	The frame alignment bytes (A1, A2) locate the SONET/SDH frame in the serial stream. These bytes are also used to byte align the serial received data. Caution must be used when replacing these bytes in the transmit stream, as it may cause framing errors at the receiving end.
C1/J0	The C1 or J0 byte is defined as the section trace byte for SONET/SDH. The frame synchronous scrambler does not scramble the J0 byte. The received section trace message is processed by the SSTB block and also available on the RTOH port. The transmit section trace message can be inserted via the SSTB, the TTOH port or the TSOP block.
Z0:	The Z0 bytes are currently defined as the section growth bytes for SONET/SDH. The frame synchronous scrambler does not scramble Z0 bytes. The transmit section growth bytes can be inserted in the following priority: the TTOC block, the TTOH port or optionally in the TSOP block. The received section growth bytes are extracted and available on the RTOH port.
B1:	The section bit interleaved parity byte provides a section error monitoring function. In the transmit direction, the SPECTRA 4x155 calculates the B1 byte over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling. An error mask can be applied to the transmit B1 via the TTOH port. TTOH will provide the error mask and not the B1 byte to insert into the transmit stream. In the receive direction, the SPECTRA 4x155 calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in the error event counter of the RSOP.
D1-D3:	The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications. In the transmit direction, the section DCC byte is inserted from a dedicated 192 kbit/s input, TSLD. Section DCC can also be inserted via the TTOH port controlled by the TTOC block with TTOH having a higher priority. In the receive direction, the section DCC is extracted on a dedicated 192 kbit/s output, RSLD. Section DCC is also extracted via onto the RTOH port via the RTOC block.
H1, H2:	The pointer value bytes locate the path overhead column in the SONET/SDH frame. In the transmit direction, the SPECTRA 4x155 TPOP block inserts a valid pointer with pointer adjustments to accommodate plesiochronous timing offsets between the references. The concatenation indication must be programmed in the slave slices via the TPOP registers. An error mask can be applied to the transmit H1/H2 via the TTOH port. TTOH will provide the error mask and not the H1/H2 bytes to insert into the transmit stream. In the receive direction, the pointer is interpreted by the RPOP to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1, H2 contain an all ones pattern.
H3:	The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.
B2:	The line bit interleaved parity bytes provide a line error monitoring function. In the transmit direction, the SPECTRA 4x155 TLOP block calculates the B2 values. The calculated code is then placed in the next frame. An error mask can be applied to the transmit B2 via the TTOH port. TTOH will provide the error mask and not the B2 byte to insert into the transmit stream. In the receive direction, the SPECTRA 4x155 RLOP block calculates the B2 code over the current frame and compares this calculation with the B2 code receive in the following frame. Receive B2 errors are accumulated in an error event counter.

K1, K2:	The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'. In the transmit direction, the K1 and K2 bytes (or part of K2) can be inserted via the TLRDI or TLAIS pins, SENDLAIS or SENDLRDI bits on the TRCP, automatic RDI insertion due to received alarms, the TTOH and TAD ports, or via register control in the TSOP and TLOP blocks. The transmitted K1/K2 bytes are also made available on the RAD port. The K1 and K2 insertion priorities are the following 1) LAIS insertion via TLAIS or TRCP. 2) LRDI insertion via TLRDI, TRCP or consequential action due to received alarms. 3) TAD port insertion via TAPS_SEL register bit in TTOC 4) TTOH port via TTOHEN high on MSB of K1 and/or K2 5) TLOP block with the TLOP Transmit K1 and K2 registers. RDI-L will only affect the K2[8:6] bits while AIS-L will force all line and SPE bytes to all ones. In the receive direction, the SPECTRA 4x155 RASE block provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is examined by the RLOP block which determines the presence of the line AIS, or the line RDI maintenance signals. A filtered version of the K1/K2 bytes is also made available on the RRCP port.
D4-D12:	The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications. In the transmit direction, the line DCC byte can be inserted from a dedicated 576 kbit/s input, TSLD. Line DCC can also be inserted via the TTOH port controlled by the TTOC block. TTOH has priority over TSLD. In the receive direction, the line DCC can be extracted on a dedicated 576 kbit/s output, RSLD. Line DCC is also extracted via onto the RTOH port via the RTOC block.
S1:	The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identify the synchronization source of the SONET/SDH signal. Bits 1 through 4 are currently undefined. In the transmit direction, the SPECTRA 4x155 TTOC and TLOP blocks provide specific register control for the synchronization status byte. The TTOH port can also be used to insert the entire S1 byte. In the receive direction, the SPECTRA 4x155 RASE block provides register access to the synchronization status byte. The RTOH provides access to the received S1 byte.
Z1:	The Z1 bytes are allocated for future growth. In the transmit direction, the SPECTRA 4x155 TTOC and TLOP blocks provide register control for the growth bytes. TTOC always has priority over the TLOP. TTOH can also be used to set the Z1 byte. In the receive direction, the SPECTRA 4x155 provides access to all growth bytes via the RTOH port.
M1:	The M1 byte provides for line remote error indications. In the transmit direction, the SPECTRA 4x155 the M1 byte is internally generated. The number of B2 errors detected in the previous interval is insert. The insertion may be overwritten via the TTOH or Transmit Ring control port. The TTOH has priority over the TRCP. In the receive direction, a legal M1 byte value is added to the line REI (FEBE) event counter in the RSOP block.

Z2:	The Z2 bytes are future growth. In the transmit direction, Z2 can be inserted with the TTOH port or programmed to be processed by the TTOC. In the receive direction, Z2 bytes are extracted and made available on the RTOH port.

13.2.2 Path Overhead Bytes

All receive path overhead bytes are extracted and presented onto the RPOH port. ~~All transmit overhead bytes can be inserted via the TPOH port with exception of the B3 which can be masked via the supplied byte on TPOH. TPOH_DIS register bit in the TPPS must be enabled for the TPOH port has effect.~~

Table 23 Path Overhead Bytes

J1:	The Path Trace byte is used to repetitively transmit a 64-byte or 16-byte message. When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00. In the transmit direction, characters can be inserted using the TPOP Path Trace register or the SPTB block. The register is the default selection and resets to 0x00 to enable the transmission of NULL characters from a reset state. In the receive direction, the path trace message is optionally extracted into the 16 or 64 byte path trace message buffer. The SPTB block can declare trace identifier unstable or mismatch alarms.
B3:	The path bit interleaved parity byte provides a path error monitoring function. In the transmit direction, the SPECTRA 4x155 calculates the B3 bytes in the master TPOP block. The calculated code is then placed in the next frame. In the receive direction, the SPECTRA 4x155 master RPOP block calculates the B3 code and compares this calculation with the B3 byte received in the next frame. B3 errors are accumulated in an error event counter. Errors are accumulated in the master slice only. Received errors are also output on the B3E pin and the resulting REI on the RAD port. The REI can also automatically be inserted in the transmit path.
C2:	The path signal label indicator identifies the equipped payload type. In the transmit direction, the SPECTRA 4x155 inserts the C2 value using the TPOP Path Signal Label register. In the receive direction, the code is available in the RPOP Path Signal Label register. In addition, the SPTB block also provides circuitry to detect path signal label mismatch and unstable alarms.
F2	The Path User channel is allocated for user communication purposes between path terminating equipment. In the transmit direction, the SPECTRA 4x155 inserts the F2 value using the TPOP Path User Channel register. In the receive direction, the F2 byte is available on the RPOH port.
G1:	The path status byte provides a path REI (FEBE) function, and a path remote defect indication function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications. In the transmit direction, the SPECTRA 4x155 provides register bits to control the path RDI states in the TPOP block. The path RDI may also be set via the TAD port. For path REI, the number of B3 errors detected in the previous interval is inserted either automatically or using a register in the TPOP block. This path REI code has 9 legal values, namely 0 to 8 errors. The TAD port may also be used to provide the REI count of a mate SPECTRA. The TAD port can retrieve up to 15 BIP error for each slice per frame (125 us). Given the timing of the RAD port, a mate SPECTRA 4x155 could output 16 errors within one frame period. If eight errors are detected in two consecutive frames and the timing makes them appear within one frame period, one count could be lost. In the receive direction, a legal path REI value is accumulated in the path REI event counter of the RPOP. In addition, the path RDI and auxiliary path RDI signal states are available in internal registers. The REI (FEBE) count is also available on the RAD port.
H4:	The multi-frame indicator byte is a payload specific byte. The byte can be set by the TTAL block in the transmit stream. In the receive stream the RPOP can process the H4 and declare LOM.

Z3-Z5:	The path growth bytes provide three unused bytes for future use. Tandem connection byte (Z5) can be inserted in the receive side towards the DROP port via the RTCOH and programming registers in the RPOP. In the transmit direction the TPOP block can be used to insert the growth bytes. In the receive direction, the growth bytes are available on the RPOH port.

13.3 Path Processing Slice Configuration Options

13.3.1 Basic Configuration

The SPECTRA 4x155 Path Processing Slice architecture enables the software, used to configure the device, to handle any combination of the four STS-3 or STS-3c SONET streams or any combination of the four STM-1/AU-3 STM-1/AU-4 SDH streams.

The Slice Configuration for SDH STM-1 Path Processing, shown in Table 24, shows examples of an STM-1 SDH stream and the configurations required for the SPECTRA 4x155 to correctly process them.

Table 24 Slice Configuration for SDH STM-1 Path Processing

CH#1 Slice#	CH#2 Slice#	CH#3 Slice#	CH#4 Slice#	Tx/Rx Order	STM-1 AU-3 Example 1	STM-1 AU-4 Example 2
1	2	3	4	1	STM-1 #1 AU-3 #1 (M)	STM-1 #1 TUG3 #1 (M)
5	6	7	8	2	STM-1 #1 AU-3 #2 (M)	STM-1 #1 TUG3 #2 (S)
9	10	11	12	3	STM-1 #1 AU-3 #3 (M)	STM-1 #1 TUG3 #3 (S)

In the first example, the STM-1 stream consists of AU-3s. To process the individual AU-3 streams in the STM-1, all TPPSs and RPPSs in the channel must be configured in the TPPS/RPPS Configuration registers as masters.

In the second example, the STM-1 stream consists of an AU-4. To process the AU-4 concatenated streams, only the first TPPS or RPPS (Slice #1, #2, #3, #4), which process TUG3 #1 in the STM-1/AU-4 streams, is configured in the corresponding TPPS/RPPS Configuration registers, as master.

An equivalent Slice Configuration example for SONET/SDH is illustrated in Table 25.

Table 25 Slice Configuration for SONET STS-3/3c Path Processing

CH#1 Slice#	CH#2 Slice#	CH#3 Slice#	CH#4 Slice#	Tx/Rx Order	STM-1 AU-3 Example 1	STM-1 AU4 Example 2
1	2	3	4	1	STM-1 #1 AU-3 #1 (M)	STM-1 #1 TUG3 #1 (M)
5	6	7	8	2	STM-1 #1 AU-3 #2 (M)	STM-1 #1 TUG3 #2 (S)
9	10	11	12	3	STM-1 #1 AU-3 #3 (M)	STM-1 #1 TUG3 #3 (S)

The valid master/slave slice configurations shown in Table 26 provide a list of all valid Path Processing Slice configurations and the corresponding STS-3 (STM-1) SONET/SDH streams being processed.

Table 26 Valid Master/Slave Slice Configurations within a Channel

	Channel #1			Channel #2			Channel #3			Channel #4		
	Path Processing Slice #											
	1	5	9	2	6	10	3	7	11	4	8	12
STS-3c	M	X_a	X_b	M	X_a	X_b	M	X_a	X_b	M	X_a	X_b
STS-3	M	M	M	M	M	M	M	M	M	M	M	M

Notes

1. Master slices are marked with the symbol “M”.
2. Slave slices are marked with the symbol “S”.
3. (X_a,X_b) represents a pair of master or slave Slices. For example, (X_a,X_b) for Slice #5 and #9 must be a pair of slave slices when Slice #1-#5-#9 are processing an STS-3c (STM-1/AU-4) stream.
4. (X_a,X_b) must be a pair of master slices when Slice #1-#5-#9 are processing an STS-3 (STM-1/AU-3) stream.
5. Channel configurations are completely independent of each other.

13.3.2 Additional Configuration for Transmit Concatenated Streams (Slave Slices)

To support the transmission of a concatenated stream, the TPOP block in the slave TPPS must be software configured to transmit a pointer in the H1 and H2 bytes identical to the concatenation indication (H1=93H, H2=FFH). This is achieved by writing 93H and FFH into the TPOP Payload Pointer MSB and TPOP Payload Pointer LSB registers, respectively. The FTPTR and the NDF bits in the TPOP Pointer Control register must then be set high to activate the new pointer insertion in the transmit stream. The TDIS bit in the SPECTRA 4x155 TPPS Path Transmit Control register must also be set high to allow the payload bytes which correspond to the “path overhead” bytes of the STS-1 (STM-0/AU-3) equivalent stream from the Add bus to be transmitted with no modification.

13.3.3 Concatenated and Non-concatenated Stream Detection

Each RPPS and TPPS processes an STS-1 (STM-0/AU-3) or equivalent stream in an STS-3/3c (STM-1/AU-3/AU-4) receive (Add bus) stream. It is capable of detecting error-free and errored pointers as well as error-free and errored concatenation indications in the H1 and H2 pointer bytes concurrently regardless of whether it is operating as a master or a slave. Errored pointers are indicated with the LOP status and errored concatenation indications are reported as an AU-3 Loss-Of-Pointer-Concatenation (AU-3LOPCON) in the RPOP (TPIP) Status and Control register.

Under normal operating conditions, the LOP status in a master slice is set low while the AU-3LOPCON is set high. The opposite is true for a slave slice; the LOP status is set high while the AU-3LOPCON status is set low. By monitoring LOP and AU-3LOPCON, it is possible to detect for mismatches between the configuration of the receive (Add bus) stream and the provisioning of the SPECTRA 4x155.

For Add bus concatenated/non-concatenated streams detection to function, valid H1 and H2 must be provided in the Add bus SPE data stream.

13.3.4 PRBS Generator/Monitor Configuration for Concatenated streams

For an STS-3 (STM-1/AU-3) Add or Drop bus stream, the (APGM/DPGM) PRBS Generator and Monitor, in each TPPS/RPPS handling an STS-1 (STM-0/AU-3), can be independently configured and enabled without affecting the PRBS generation or monitoring performed by other TPPS/RPPSs. However, for concatenated STS-3c (STM-1/AU-4) streams, a group re-start of the PRBS generation is required after all the PRBS Generators within the TPPS/RPPS group have been configured and enabled by setting the GEN_REGEN bit in the (APGM/DPGM) Generator Control register of the master Path Processing Slice. The software group re-start will align all the PRBS Generators to produce a complete and valid sequence for the concatenated stream. Alarm such as LOP or path AIS may cause misalignment between PRBS Generators in the PPS group and may persist after the alarm has been removed. Misalignment may also be caused by a frame re-alignment on the Add Bus #1 or Drop bus via DFP.

Misalignment is indicated by the signature status (GEN_SIGNV) bit in the (APGM/DPGM) Generator/Monitor Status/Interrupt register of a slave Path Processing Slice. A software group re-start is required to recover from this condition.

The PRBS Monitors in a TPPS/RPPS group processing a concatenated stream operate independently of each other. If the monitored PRBS sequence is formed by misaligned sub-sequences caused by misaligned Generators or incorrect muxing order, the PRBS Monitors in the slave Path Processing Slices will indicate that they have locked on to the corresponding sub-sequences. However, the misalignment will be indicated by the signature status (MON_SIGNV) bit in the (APGM/DPGM) Generator/Monitor Status/Interrupt register of a slave Path Processing Slice.

13.4 Time Slot Interchange (Grooming) Configuration Options

~~The TelecomBus STS-1 (STM-0/AU-3) Time-slots (streams) table~~ Table 27 lists all the Telecom Add/Drop bus streams or time-slots for the two different TelecomBus configurations. The Input/Output order of the STS-1 (STM-0/AU-3) streams or time-slots is provided for each TelecomBus configuration.

Table 27 Telecom Bus STS-1 (STM-0/AU-3) Time-slots (Streams)

"STS-1/AU-3" TelecomBus Time-Slots (Streams)	4 x 19.44 MHz Buses		1x 77.76 MHz Bus	
	I/O Order	Data Bus	I/O Order	Data Bus
STM-1 #1 AU-3 #1	1	AD[7:0] DD[7:0]	1	AD[7:0] DD[7:0]
STM-1 #1 AU-3 #2	2		5	
STM-1 #1 AU-3 #3	3		9	
STM-1 #2 AU-3 #1	1	AD[15:8] DD[15:8]	2	
STM-1 #2 AU-3 #2	2		6	
STM-1 #2 AU-3 #3	3		10	
STM-1 #3 AU-3 #1	1	AD[23:16] DD[23:16]	3	
STM-1 #3 AU-3 #2	2		7	
STM-1 #3 AU-3 #3	3		11	
STM-1 #4 AU-3 #1	1	AD[31:24] DD[31:24]	4	
STM-1 #4 AU-3 #2	2		8	
STM-1 #4 AU-3 #3	3		12	

The grooming of STS (AU) streams at the Telecom Drop bus(es) is achieved by selecting an STS-1 (STM-0/AU-3) or equivalent receive stream for each Drop bus time-slot other than its default. Any of the four channels receive stream can be selected for Drop bus time-slot STM-1 #i AU-3 #j using the STM1SEL[1:0] and AU-3SEL[1:0] bits in the corresponding Drop Bus STM-1 #i AU-3 #j Select register. The selected STM number corresponds to the device channel. Normally, each STS-1 (STM-0/AU-3) receive stream is selected only for one Drop bus time-slot. Drop bus multicast is achieved when the same STS-1 (STM-0/AU-3) receive stream is selected for multiple Drop bus time-slots.

Similarly, grooming of STS (AU) streams at the Telecom Add bus(es) is achieved by selecting an STS-1 (STM-0/AU-3) or equivalent Add bus stream (for example, a time-slot or column in an STS-12/STM-4 frame) for each transmit time-slot other than its default. Any Add bus stream can be selected for transmit time-slot STM-1 #i AU-3 #j using the STM1SEL[1:0] and AU-3SEL[1:0] bits in the corresponding SPECTRA 4x155 Add Bus STM-1 #i AU-3 #j Select register. The selected STM number corresponds to the device channel. Normally, each Add bus STS-1 (STM-0/AU-3) stream is selected only for a single transmit time-slot. Add bus multicast is achieved when the same STS-1 (STM-0/AU-3) Add bus stream is selected for multiple transmit time-slots.

The default settings in the SPECTRA 4x155 Add/Drop Bus STM-1 #i AU-3 #j Select registers disable all grooming functions.

13.5 System Interface Configuration Options

13.5.1 Single 77.76 MHz Byte TelecomBus Mode

The Single 77.76 MHz Byte TelecomBus Mode is selected by setting the ATMODE bit in the Add Bus Configuration register to low (for Add bus) and the DTMODE bit in the Drop Bus Configuration register to low (for Drop bus). When operating in this mode, system data is delivered to the SPECTRA 4x155 via an eight bit Add bus (AD[7:0]) and is sourced by the SPECTRA 4x155 via an eight bit Drop bus (DD[7:0]). For the Add bus, the SPECTRA 4x155 requires either a composite C1, J1, V1 input or optionally a C1 or AFP signal coupled with a valid H1, H2 pointer.

The Add and Drop bus timing domains can be asynchronous to each other as well as to the transmit and receive line side interfaces. The SPECTRA 4x155 compensates for timing differences with pointer justifications.

13.5.2 Four 19.44 MHz Byte TelecomBus Mode

The Four 19.44 MHz Byte TelecomBus Mode is selected by setting the ATMODE bit in the SPECTRA 4x155 Add Bus Configuration register to high (for Add bus) and the DTMODE bit in the Drop Bus Configuration register to high (for Drop bus). When operating in this mode, system data is delivered to the SPECTRA 4x155 through four eight bit Add buses (AD[7:0], AD[15:8], AD[23:16], AD[31:24]) and is sourced by the SPECTRA 4x155 via four eight bit Drop buses (DD[7:0], DD[15:8], DD[23:16], DD[31:24]). For the Add buses, the SPECTRA 4x155 requires either a composite C1, J1, V1 input or optionally a C1 or AFP signal coupled with a valid H1, H2 pointer.

Both the Add bus and the Drop bus timing domains can be asynchronous to each other as well as to the transmit and receive line side interfaces. The SPECTRA 4x155 compensates for timing differences with pointer justifications.

13.6 Bit Error Rate Monitor (BERM)

The SPECTRA 4x155 provides two BERM blocks per channel. One can be dedicated to monitoring the Signal Degrade (SD) error rates and the other dedicated to monitoring the Signal Fail (SF) error rates.

The BERM block counts and monitor line BIP errors over programmable periods of time (window size). At the associated thresholds, it declares an alarm or clears it if the alarm is already set. A different threshold and accumulation period must be used for declaring and clearing alarms regardless of whether the two operations are set to the same BER threshold. The following table lists the recommended content of the BERM registers for different error rates (BER). Both BERMs in the TSB are equivalent and are programmed similarly. In a normal application, they will be set to monitor different BERs.

When the SF/SD CMODE bit is set to logic one, the clearing monitoring is recommended to be performed using a window size that is eight times longer than the declaration window size. When the SF/SD CMODE bit is set to logic zero, it is recommended that clearing monitoring is performed using a window size equal to the declaration window size. In all cases the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. Table 28 indicates the declare BER and evaluation period only.

The Saturation threshold is not listed in the table, and should be programmed with the value 0xFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts.

Table 28 Recommended BERM settings

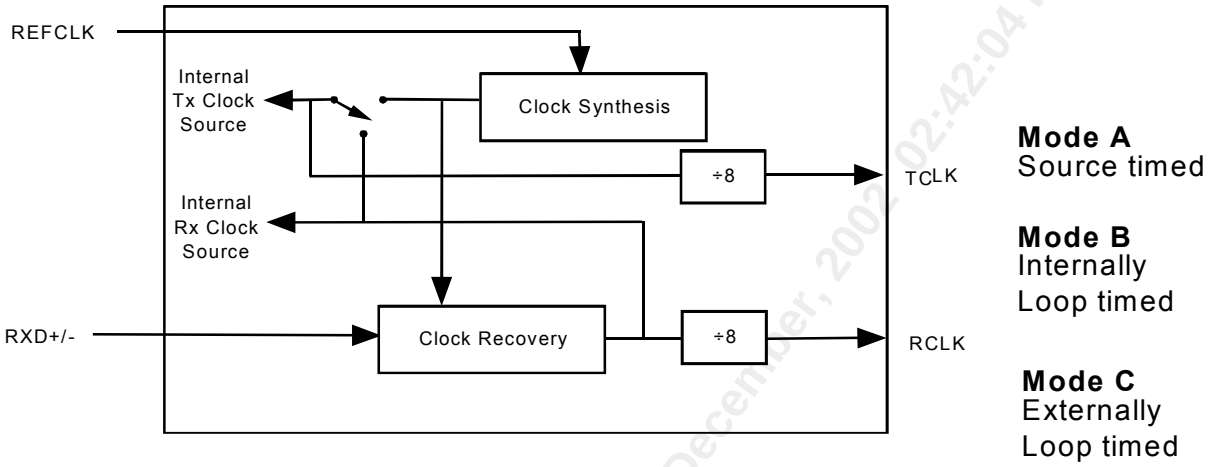
Declare BER	Eval Per (s)	SF/SD SMODE	SF/SD CMODE	SF/SD SAP	SF/SD DTH	SF/SDCTH
10^{-3}	0.008	0	0	0x000008	0x245	0x083
10^{-4}	0.013	0	1	0x00000D	0x0A3	0x0B4
10^{-5}	0.100	0	1	0x000064	0x084	0x08E
10^{-6}	1.000	0	1	0x0003E8	0x085	0x08E
10^{-7}	10.000	0	1	0x002710	0x085	0x08E
10^{-8}	83.000	0	1	0x014438	0x06D	0x077
10^{-9}	667.000	0	1	0x0A2D78	0x055	0x061

Note: Table 28 is based on the Telcordia GR-253 specification. Please refer to the SONET/SDH/SDH Bit error Threshold Monitoring application note for more details as well as the recommended programming configuration meeting the ITU G.783 specification.

13.7 Clocking Options

The SPECTRA 4x155 supports several clocking modes. Figure 14 is an abstraction of the clocking topology.

Figure 14 Conceptual Clocking Structure



Mode A is provided for all public user network interfaces (UNIs) and for private UNIs and private network node interfaces (NNIs) that are not synchronized to the recovered clock.

The transmit clock in a public UNI must conform to SONET Network Element (NE) requirements specified in Telcordia GR-253-CORE. These requirements include jitter generation, short term clock stability, phase transients during synchronization failure, and holdover. The 19.44 MHz clock source is typically a VCO (or temperature compensated VCXO) locked to a primary reference source for public UNI applications. The accuracy of this clock source should be within ±20 ppm of 19.44 MHz to comply with the SONET/SDH network element free-run accuracy requirements.

The transmit clock in a private UNI or a private NNI may be locked to an external reference or may be free-run. The simplest implementation requires an oscillator free-running at 19.44 MHz.

Mode A is selected by clearing the LOOPT bit of the Channel Control register. REFCLK is multiplied by eight to become the 155.51 MHz transmit clock. REFCLK must be jitter free. Note: The source REFCLK is also internally used as the clock recovery reference.

Mode B is provided for private UNIs and private NNIs that require synchronization to the recovered clock. Mode B is selected by setting the LOOPT bit of the Master Control register. Normally, the transmit clock is locked to the receive data. In the event of a LOS condition, the transmit clock is synthesized from REFCLK.

Mode C is the external loop timing mode that makes use of the external PLL. This mode can be achieved when LOOPT is set to logic zero. This mode allows an interface to meet Telcordia's wander transfer and holdover stability requirements.

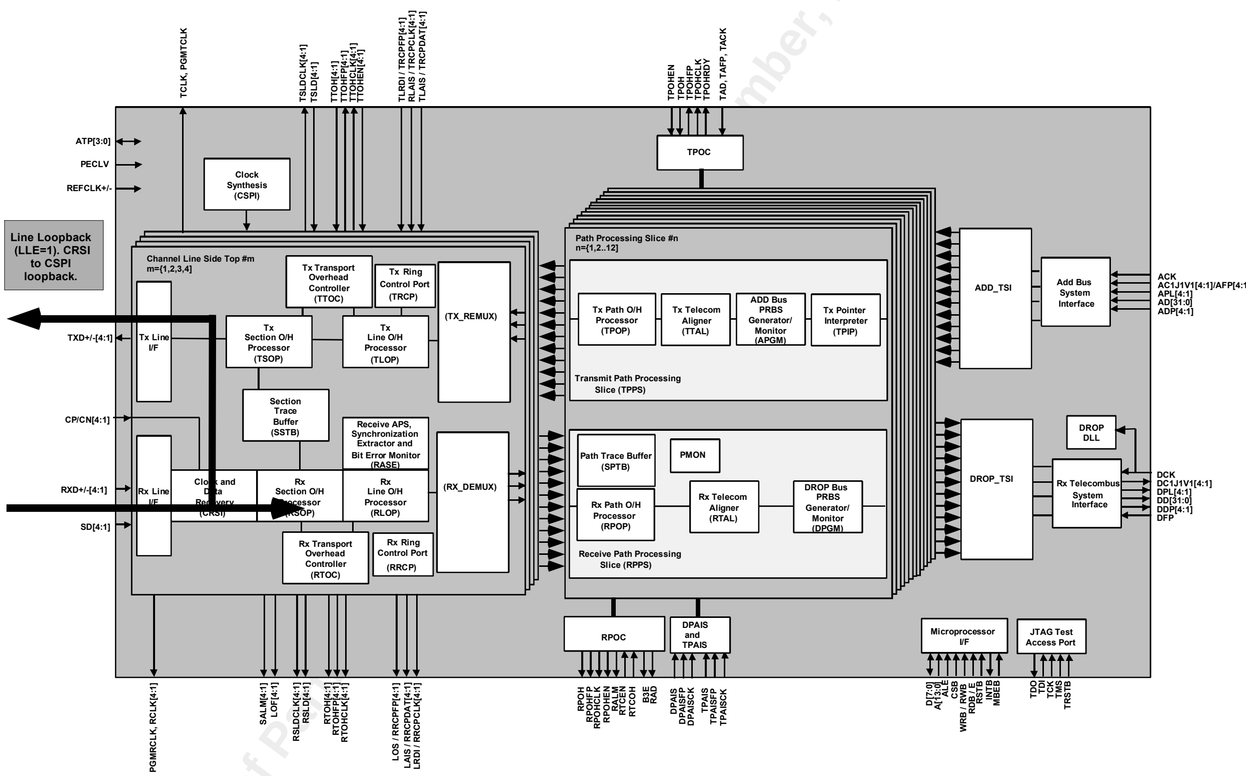
13.8 Loop Back Modes

The SPECTRA 4x155 supports four loop back functions: line loop back, system-side line loop back, parallel diagnostic loop back and serial diagnostic loop back.

13.8.1 Line Loop Back

The Line Loop back is used to loop back the recovered data and clock from the clock recovery unit/serial-to-parallel converter (CRSI) to the clock recovery unit/parallel-to-serial converter (CSPI). The CRSI will recover a clock from the received serial stream and retime the serial data before looping it back to the CSPI. The looped back data is retimed and transmitted out onto TXD+/-. The Line loop back is programmable on a per channel basis. Refer to Figure 15.

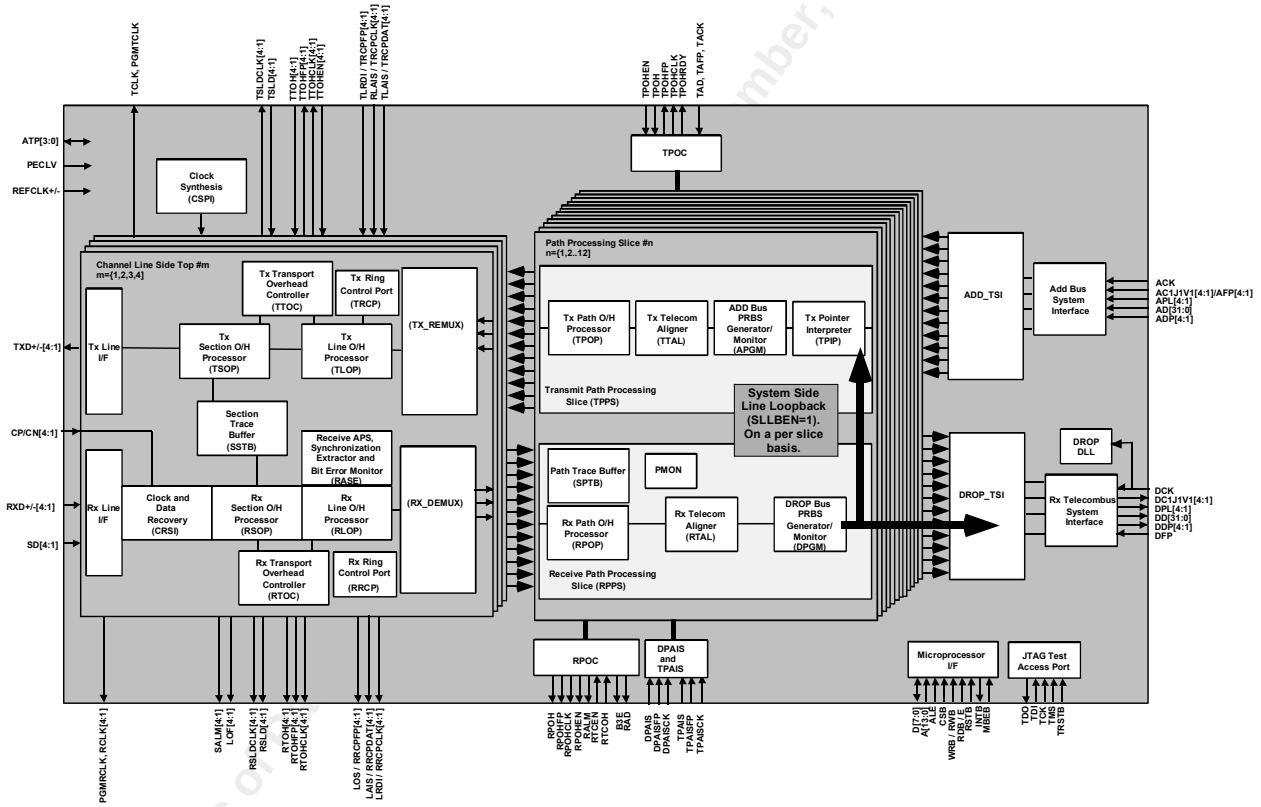
Figure 15 Line Loop Back



13.8.2 System Side Line Loop Back

The System Side Line Loop back (SLLB) loops back the line side receive data to the transmit interface after having terminated the SONET payloads. Prior to entering the Drop TSI, the receive payload is looped back on a per slice basis to the transmit path processing slice (TPPS). The received payload is looped back to the TPIP block that interprets the pointer to find the payload. Refer to Figure 16.

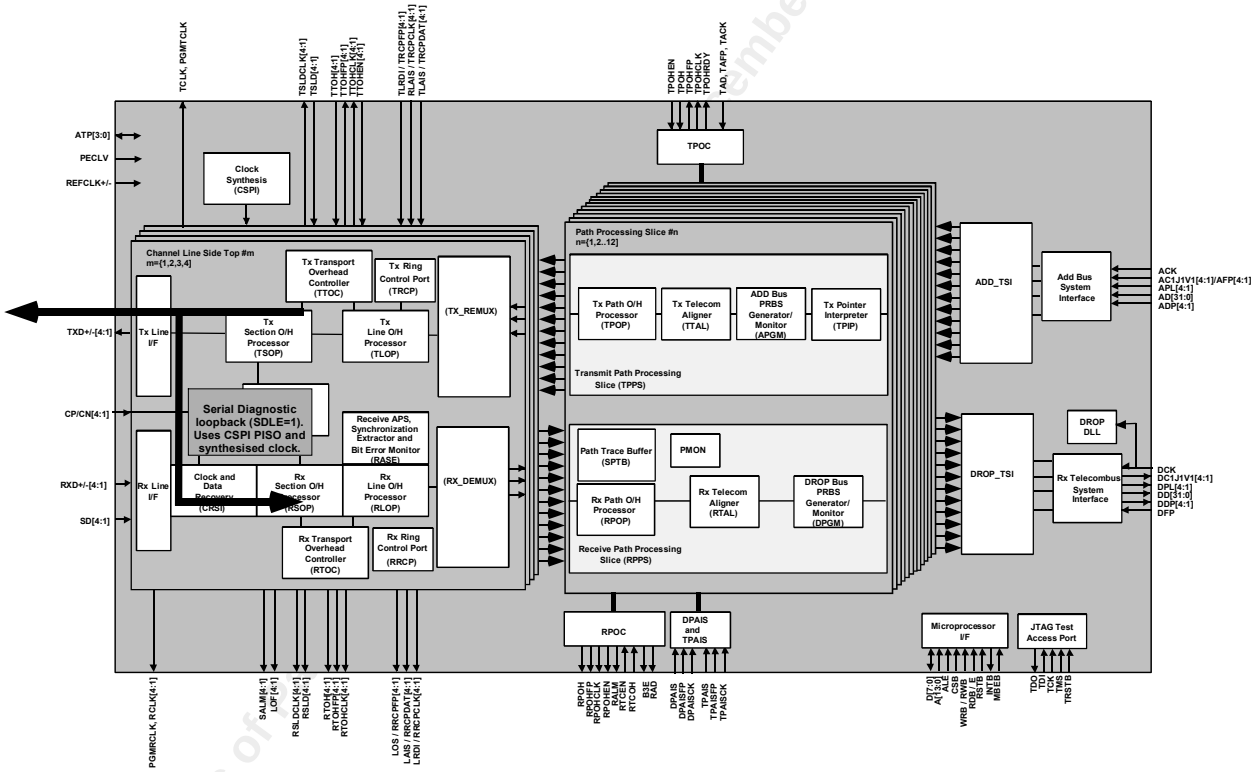
Figure 16 System Side Line Loop Back



13.8.3 Serial Diagnostic Loop Back

The Serial Diagnostic Loop back (SDLE) is a loop back at the line side of the device. The serial transmit data timed to the synthesized clock is looped back just before the TXD outputs. On the receive side, the looped back serial data replaces the RXD inputs. From this point, the looped data is processed as regular data having come from the serial receive interface. The CRSI will lock and recover a clock from the looped back data. This loop back allows a diagnostic test of the device from the system side using the analog blocks. Refer to Figure 17.

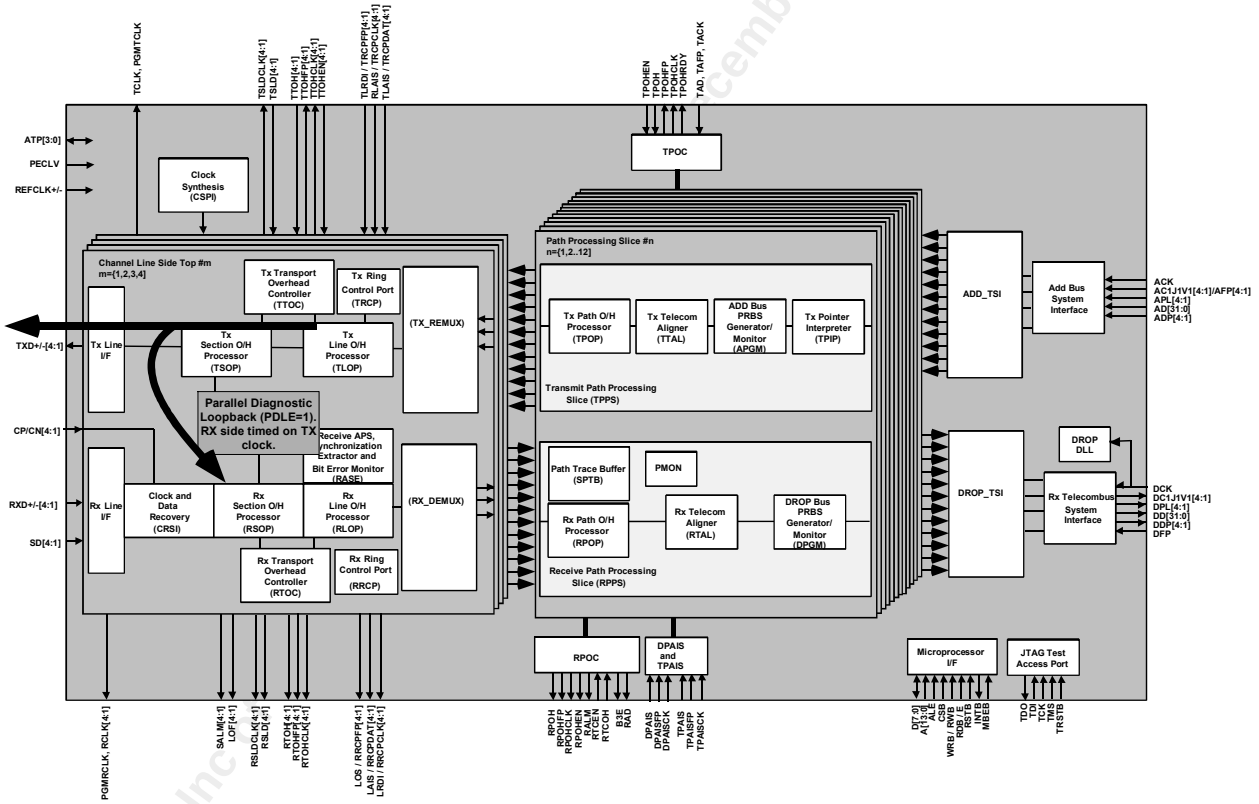
Figure 17 Serial Diagnostic Loop Back



13.8.4 Parallel Diagnostic Loop back

The Parallel Diagnostic Loop back (PDLE) is a loop back at the line side of the device from transmit to receive, before entering the CSPI. The parallel transmit data just before the CSPI is looped back to the receive side of the device replacing the parallel data from the CRSI. From this point, the looped data is processed as regular data having come from the CRSI's SIPO. The RSOP will frame to the looped back data and all regular alarms declared. This loop back allow a diagnostic test of the device from the system side without the use of the analog blocks. Refer to Figure 18.

Figure 18 Parallel Diagnostic Loop Back



13.9 Loop Back Operation

The loop back modes are activated by the SLLE, PDLE, and SDLE bits contained in the SPECTRA 4x155 Configuration register and the SLLBEN and LLBEN bits in the SPECTRA 4x155 TPPS Configuration register.

The line loop back (SLLE=1) connects the high speed receive data and clock to the high speed transmit data and clock, and can be used for line side investigations (including clock recovery and clock synthesis). While in this mode, the entire receive path is operating normally.

The serial diagnostic loop back (SDLE=1) connects the high speed transmit data and clock to the high speed receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

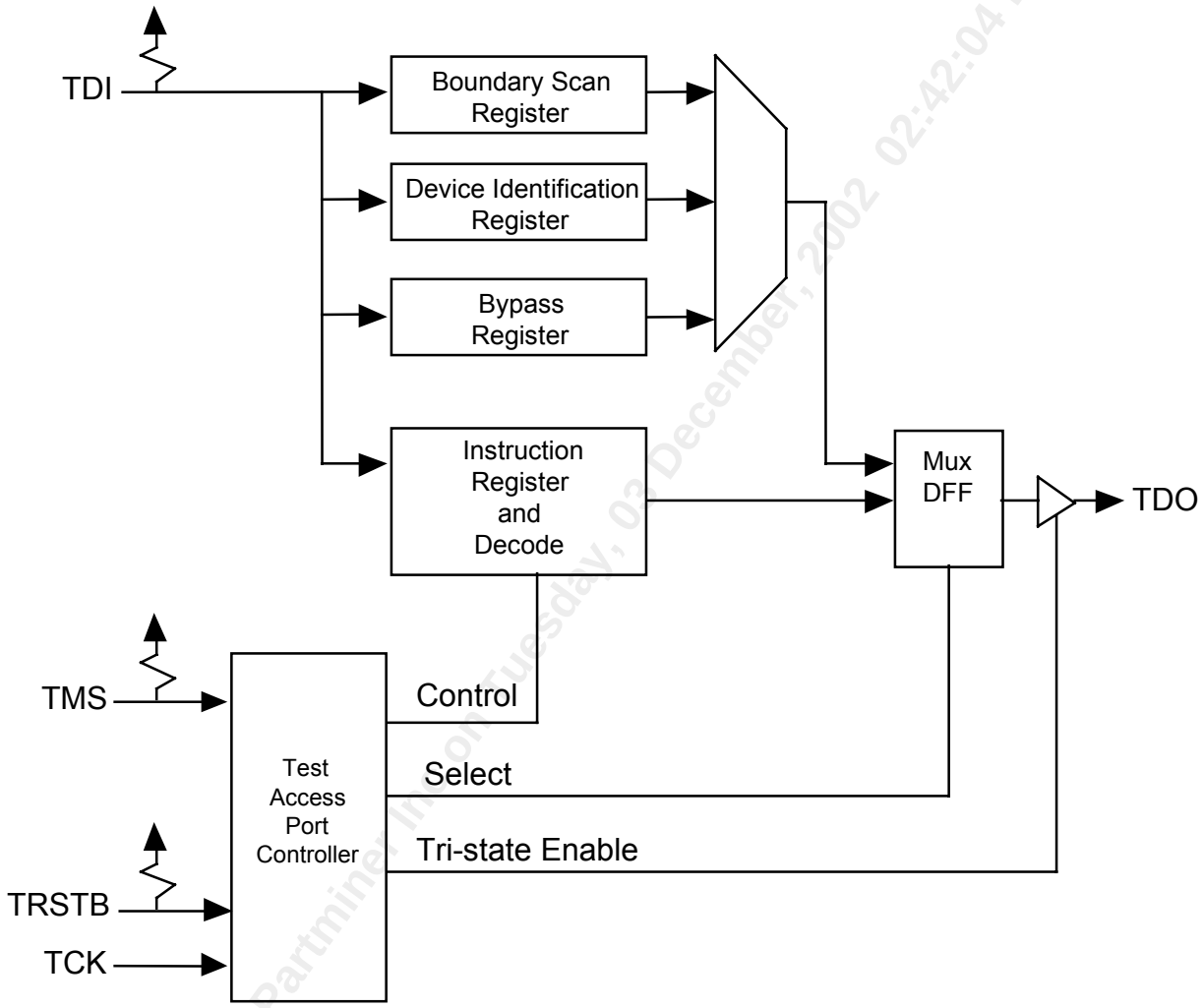
The parallel diagnostic loop back (PDLE=1) connects the byte wide transmit data and clock to the byte wide receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The system-side line loop back (SLLBEN=1) connects the STS-1 (STM-0/AU-3) or equivalent receive stream from the Receive Telecom bus Aligner (RTAL) of the associated RPPS to the Transmit Telecom bus Aligner (TTAL) of the corresponding TPPS. This mode can be used for line side investigations (including clock recovery and clock synthesis) as well as path processing investigations. While in this mode, the entire receive path is operating normally. The SPECTRA 4x155 may be configured to support the system-side line loop back of up to 12 STS-1 (STM-0/AU-3) or equivalent receive streams.

13.10 JTAG Support

The SPECTRA 4x155 supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in Figure 19.

Figure 19 Boundary Scan Architecture



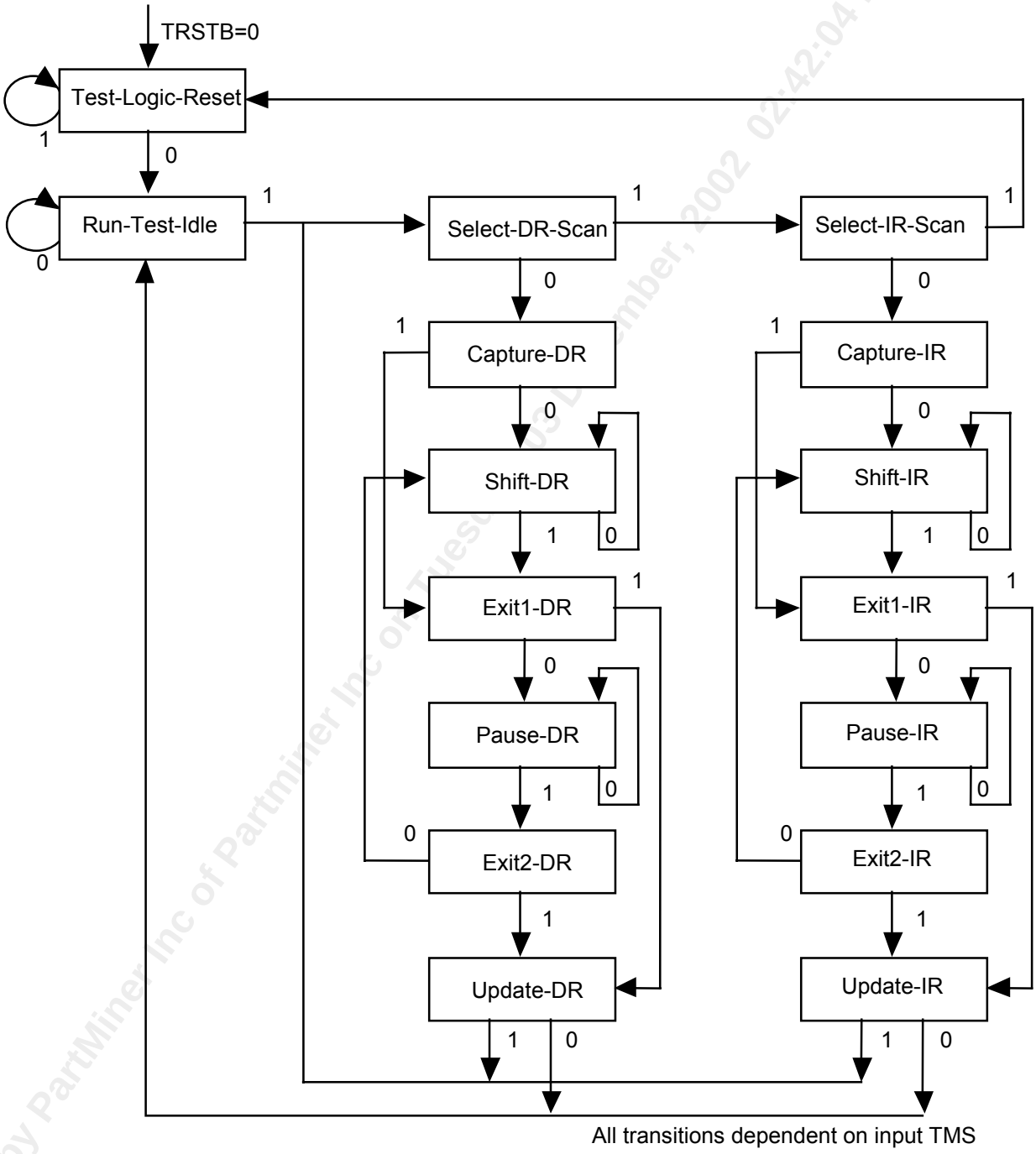
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register, and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI, to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows board inter-connectivity to be tested. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. Also, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.10.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is shown in Figure 20.

Figure 20 TAP Controller Finite State Machine



13.10.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for five TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

13.10.3 Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects an serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.11 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines must be followed in order to ensure proper operation:

1. Use a single plane for both digital and analog grounds.

2. Provide a +3.3 volt analog and digital supply with filtering between the power supply rail and the analog power pins.

3. Use simple RC filtering. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is the best approach provided care is taken to ensure the IR Drop in the resistance does not lower the supply voltage below the recommended operating voltage.

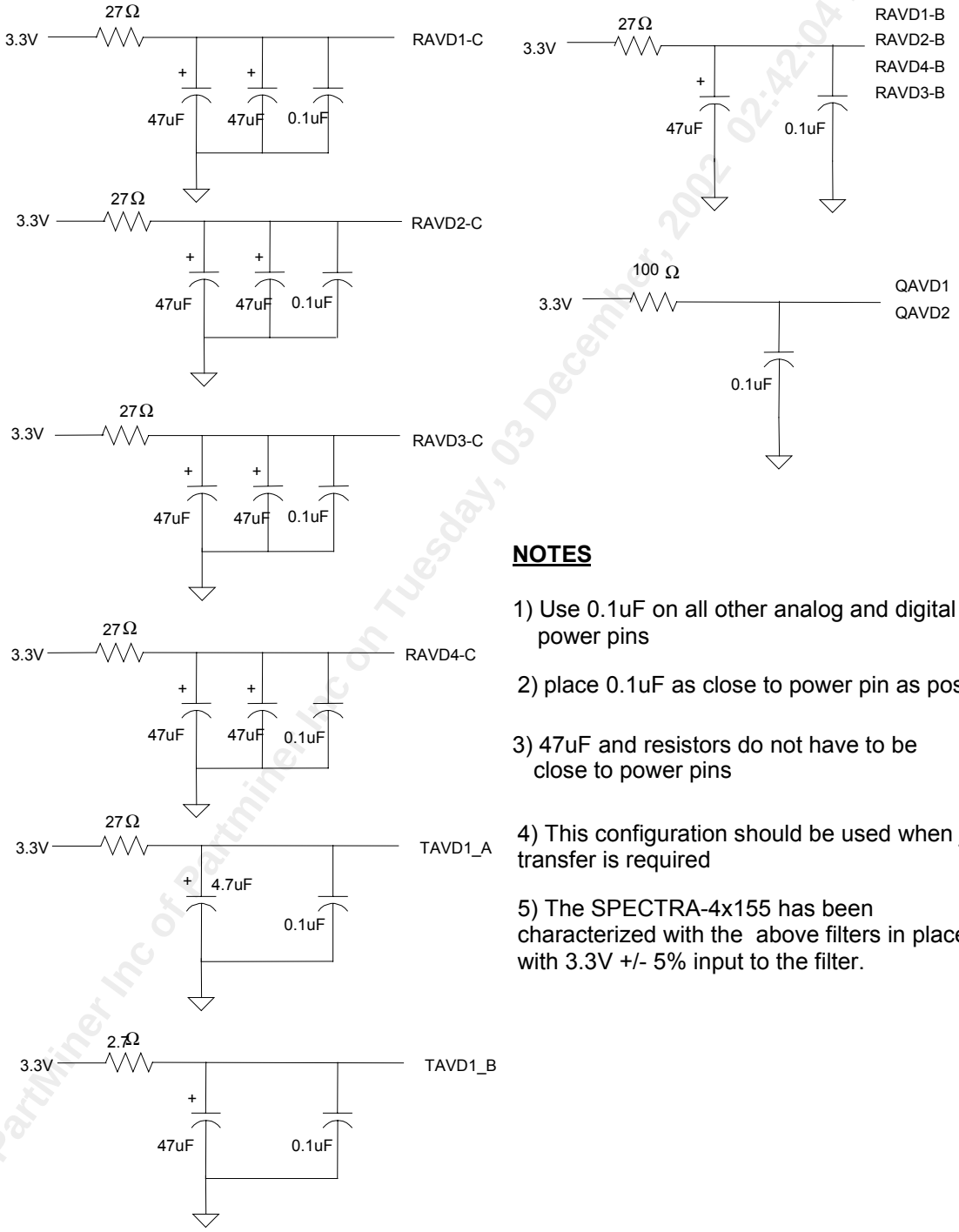
4. Use separate high-frequency decoupling capacitors as close to the package pin as possible as these are recommended for the analog power (TAVD, RAVD, QAVD) pins. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent transients from coupling into some reference circuitry. See the section on Power Supplies for more details.

5. Route the high speed serial streams (TXD1-4+/- and RXD1-4+/) with 50 µm controlled impedance circuit board traces and terminate with a matched load. This must be done. Normal CMOS-type design rules are not recommended and will reduce the performance of the device. See the section on interfacing to ECL and PECL devices for more details (Section 13.13).

13.12 Analog Power Supply Filtering

The noise environment and signal integrity are often the limiting factors of the system performance. The analog circuitry is particularly susceptible to noise. We recommend using the analog power filtering scheme shown in Figure 21.

Figure 21 Analog Power Filters with 3.3V Supply (1)



NOTES

1) Use 0.1uF on all other analog and digital power pins

2) place 0.1uF as close to power pin as possible

3) 47uF and resistors do not have to be close to power pins

4) This configuration should be used when jitter transfer is required

5) The SPECTRA-4x155 has been characterized with the above filters in place, with 3.3V +/- 5% input to the filter.

13.13 Power Supplies Sequencing

Due to the ESD protection structures in the pads, caution must be taken when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to blow these ESD protection devices or trigger latch up. Use the following recommended power supply sequencing:

1. To prevent damage to the ESD protection on the device inputs the maximum DC input current specification must be respected. Either ensure that the VDD power is applied before input pins are driven or increase the source impedance of the driver so that the maximum driver short circuit current is less than the maximum DC input current specification.

2. Supply QAVD power either after VDD or simultaneously with VDD to prevent any current flow through the ESD protection devices that exist between QAVD and VDD power supplies. To prevent forward biasing the ESD protection diode between QAVD and VDD supplies, the differential voltage measured between these power supplies must be less than 0.5 Volt.

   This recommended differential voltage is to include peak-to-peak noise on the VDD power supply as digital noise will otherwise be coupled into the analog circuitry. Current limiting can be accomplished by using an off chip three terminal voltage regulator supplied by a quiet high voltage supply.

3. Supply BIAS voltage either before VDD or simultaneously with VDD to prevent current flow through the ESD protection devices that exist between BIAS and VDD power supplies.

4. Apply analog power supplies (AVD, includes RAVDs, TAVDs but not QAVD) after QAVD. These can be applied at the same time as QAVD providing the 100 ohm resistor in series with QAVD, shown in Figure 21 is in place.

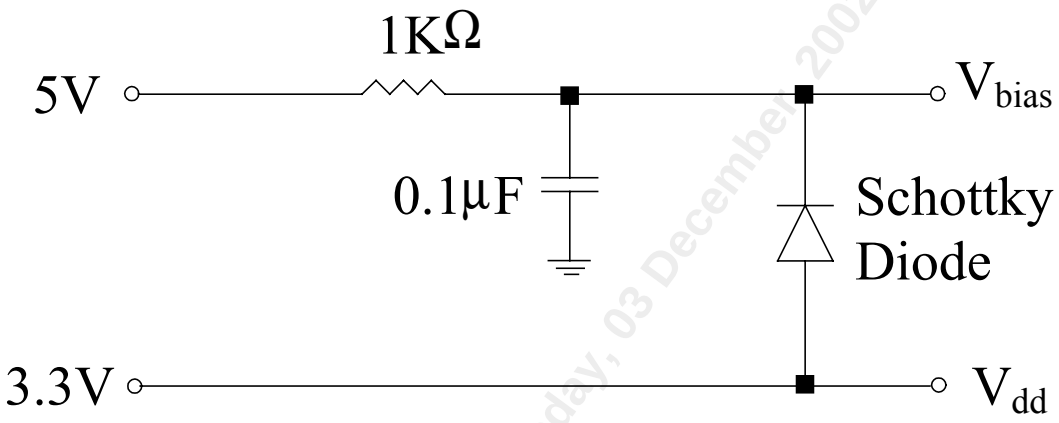
   Ensure the AVD supplies are current limited to the maximum latchup current specification (100 mA). To prevent forward biasing the ESD protection diode between AVD supplies and QAVD the differential voltage measured between these power supplies must be less than 0.5 Volt.

   This recommended differential voltage is to include peak-to-peak noise on the QAVD and AVD power supplies as digital noise will otherwise be coupled into the analog circuitry. Use an off chip three terminal voltage regulator supplied by a quiet high voltage supply to limit the current. If the VDD power supply is relatively quiet, VDD can be filtered using a ferrite bead and a high frequency decoupling capacitor to supply AVD. The relative power sequencing of the multiple AVD power supplies is not important.

5. Power down the device in the reverse sequence. Use the above current limiting technique for the analog power supplies. Small offsets in VDD/AVD discharge times will not damage the device.

Figure 22 illustrates a power sequencing circuit to avoid latch-up or damage to 3.3 Volt devices that are 5 Volt tolerant. This circuit will ensure V_{bias} is greater than V_{dd} and protect against designs which require the 3.3 Volt power supply appearing before the 5 Volt supply. The Schottky diode shown on Figure 22 is optional.

Figure 22 Power Sequencing Circuit



13.14 Interfacing to ECL or PECL Devices

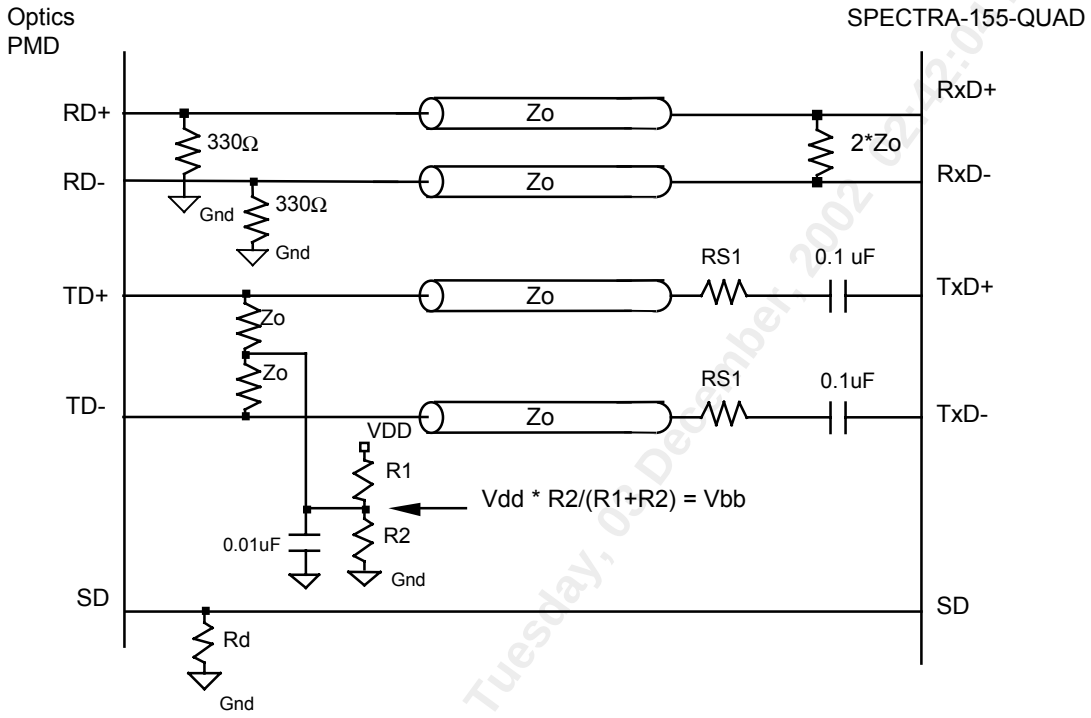
Although the TXD+/- outputs are TTL compatible, only a few passive components are required to convert the signals to ECL (or PECL) logic levels. Figure 23 illustrates the recommended configurations for both types of ECL voltage levels. The PECLV pin should be set appropriately for the selected configuration.

The capacitors, AC, couple the outputs so that the ECL inputs are free to swing around the ECL bias voltage (V_{BB}). The combination of the RS1 and Z0 resistors divides the voltage down to a nominally 800 mV swing. The Z0 resistors also terminate the signals.

The RXD+/- inputs to the SPECTRA 4x155 are DC coupled as shown. The device has a true PECL receiver so only termination resistors are required.

Ceramic coupling capacitors are recommended.

Figure 23 Interfacing to ECL or PECL Devices



Notes: Vpp is minimum input swing required by the optical PMD device.

Vbb is the switching threshold of the PMD device (typically Vdd - 1.3 volts)

Vpp is Voh - Vol (typically 800 mVolts)

Vpp = (Zo/((RS1+Rs)+Z0) * Vdd

- Vdd (SPECTRA-155-QUAD analog transmit power) 3.3V
- Zo (trace impedance) typically 50Ω
- Rs (TxD source impedance) typically 15-20Ω
- RS1: ~ 158Ω

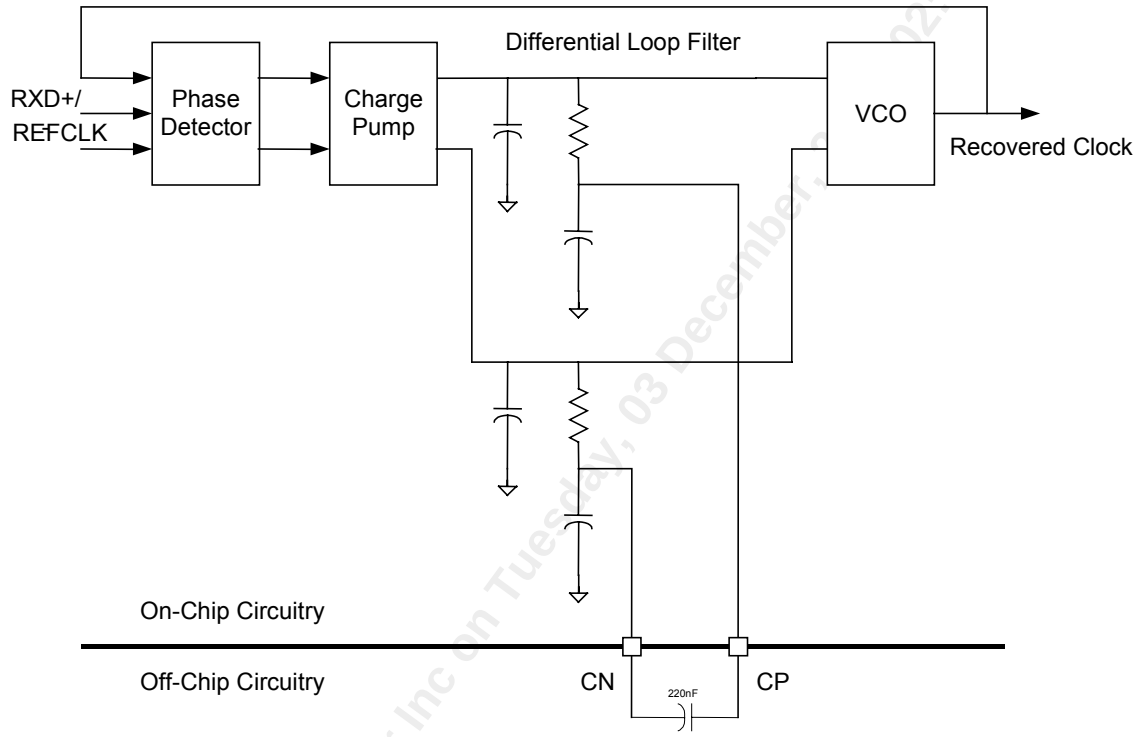
For interfacing to 5.0V ODL, R1 : 237Ω , R2 : 698Ω
Rd : 330Ω
For interfacing to 3.3V ODL, R1 : 220Ω, R2: 330Ω
Rd : 180Ω

13.15 Clock Recovery

Figure 24 is an abstraction of the clock recovery PLL illustrating the connections to external components. In order to meet jitter transfer requirements for WAN applications, the CRU requires an external 220nF X7R 10% ceramic loop capacitor. This capacitor is placed across pins C1 and C2 in close proximity to the chip pins.

The external loop filter capacitor is used as a floating capacitor, which means that neither of C1 and C2 is grounded.

Figure 24 Clock Recovery External Components



14 Functional Timing

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines. That is, polarity control bits in the SPECTRA 4x155 registers are set to their default states. It is also assumed that the STS (AU) grooming functions at the Add and Drop buses using the TSI feature are disabled.

14.1 Receive Transport Overhead Extraction

14.1.1 Receive Transport Overhead (RTOH) Functional Timing

Figure 25 Receive Tranport Overhead Extraction

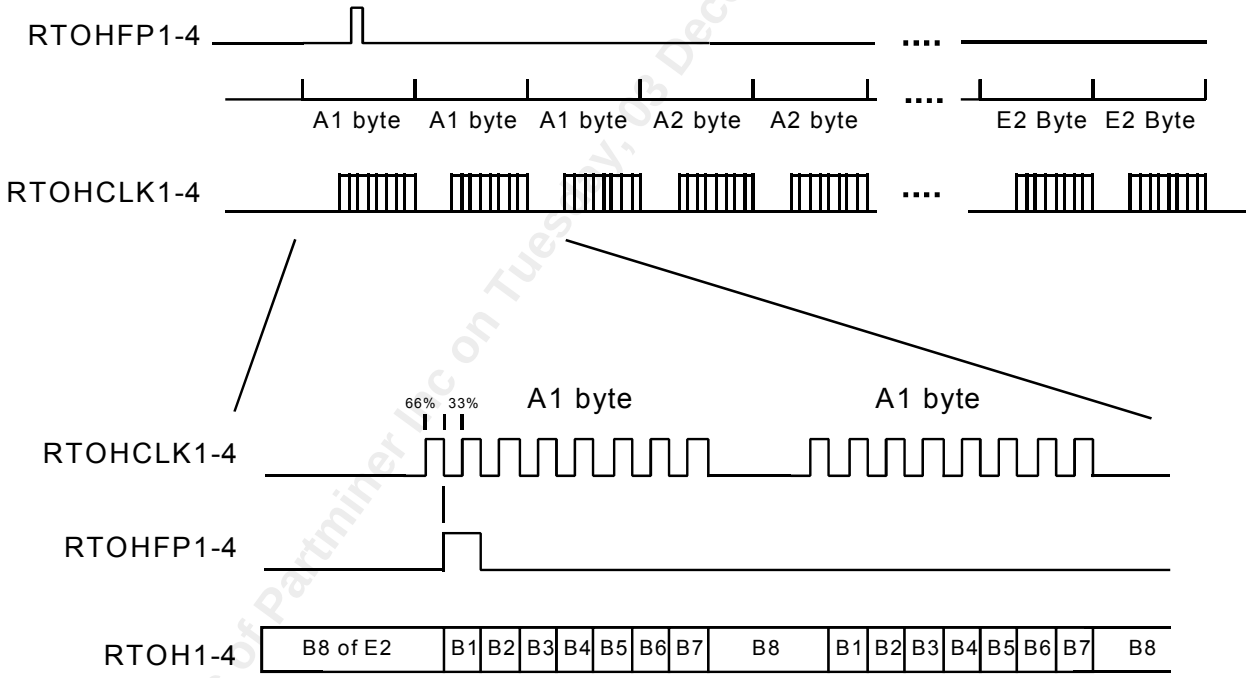


Figure 25 shows the Receive Transport Overhead (RTOH) output timing. RTOHCLK1-4 is a 5.184 MHz clock generated by gapping a 6.48 MHz, 33% high duty cycle clock. 648 bits (27x3 bytes) will be output on RTOH1-4 between the rising edges of RTOHFP1-4. RTOHCLK1-4 will have a 33% high duty cycle and RTOHFP1-4 will be set high to identify the MSB (bit 1) of the STS-1 #1 A1 byte. The RTOHCLK1-4 begins bursting out data during RTOHFP1-4 high. The Overhead bytes of the each row are bursted out followed by a prolonged gapped period in the clock. The clock begins bursting out data once again when the next row's overhead has been received. In between each overhead byte, the clock gaps for one cycle.

RTOHCLK1-4 should be used to sample the RTOH1-4 and RTOHFP1-4 output signals. All outputs are aligned with the falling edge of RTOHCLK1-4 and should be sampled on the rising edge of RTOHCLK1-4.

14.1.2 Receive Section and Line DCC Functional Timing

Figure 26 and Figure 27 show the receive section and line DCC output timings. The section/line (RSLD and RSLDCLK) functional timing for the case where RSLD1-4 is carrying the section DCC bytes (D1-D3) is shown in Figure 26. Sampling RTOHFP1-4 high identifies the MSB of the D1 byte available on the RSLD output. In the case when carrying the line DCC bytes (D4-D12), the RSLD1-4 and RSLDCLK1-4 functional timing is shown in Figure 27. Sampling RTOHFP1-4 high identifies the MSB of the D4 byte available on the RSLD output.

Enabling the LOS/LOF/LAIS or TIM alarms via the associated LINE_AISEN(2:0) or SECT_AISEN[2:0] register bits will force the RSLD1-4 output to logic one when the alarms are asserted.

Figure 26 RX Section DCC Timing

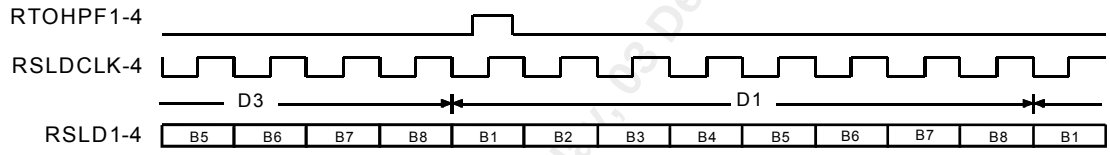
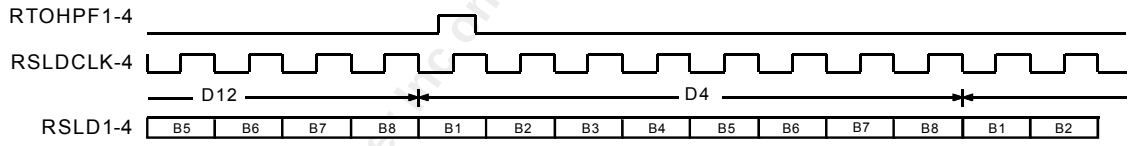


Figure 27 RX Line DCC Timing



The section/line data output (RSLD1-4) is aligned with the falling edge of the RSLDCLK1-4. The rising edge of RSLDCLK1-4 should be used to sample the RSLD1-4 data and RTOHFP1-4. When carrying the line DCC, RSLDCLK1-4 is a 576 kHz clock (see line DCC Figure 27) and when carrying the section DCC, RSLDCLK1-4 is a 192 kHz clock.

14.2 Transmit Transport Overhead Insertion

14.2.1 Transmit Transport Overhead (TTOH) Functional Timing

Figure 28 Transmit Transport Overhead Insertion

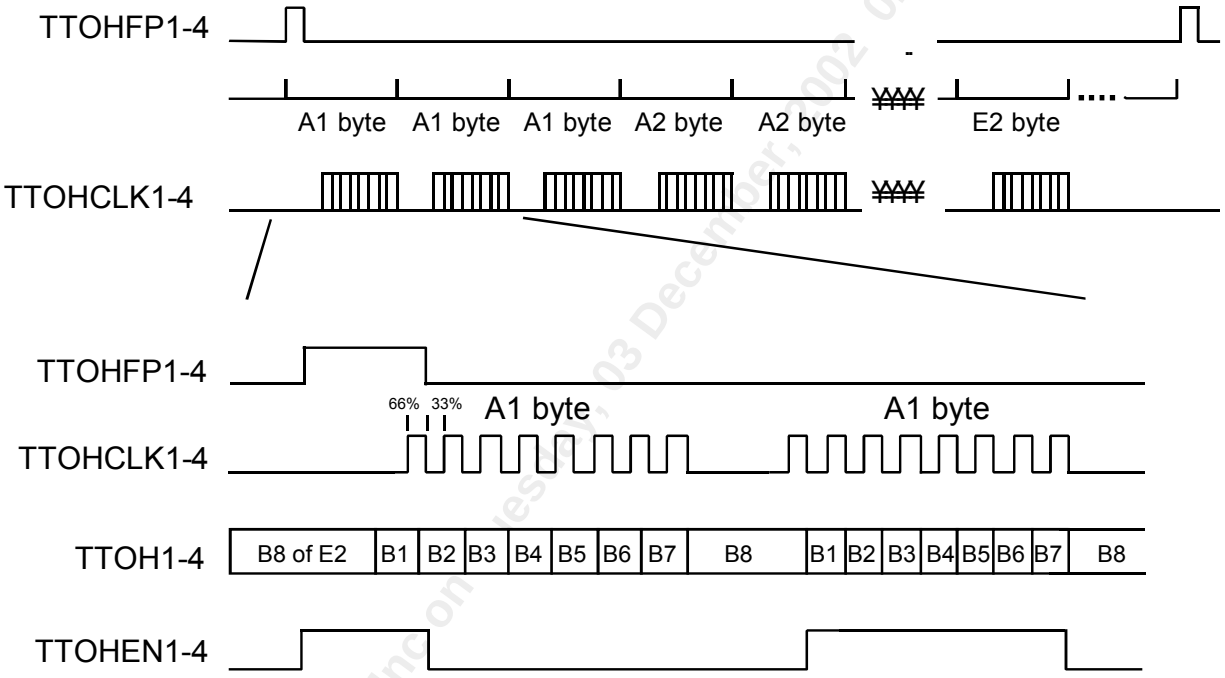


Figure 28 shows all the TTOH1-4 port signal functional timings. The TTOH1-4 ports (TTOH1-4, TTOHCLK1-4, TTOHFP1-4 and TTOHEN1-4) are used to supply the SONET/SDH transport overhead bytes for channel #1-4 of the SPECTRA 4x155. The serial TTOH data stream supplies the 81 transport overhead bytes (27 section overhead and 54 line overhead bytes) in 125 us. The TTOHCLK1-4 output provides timing for the TTOH1-4 and TTOHEN1-4 inputs. TTOHCLK1-4 is a 5.184 MHz clock generated by gapping a 6.48 MHz clock.

The TTOHCLK1-4 generates a burst of clock cycles after the TTOHFP1-4. This burst is used to receive all overhead bytes needed for insertion into the 9 overhead bytes (a row of the SONET/SDH payload). The TTOHFP1-4 output is updated on the falling edge of TTOHCLK1-4 and is used to identify the positioning of the 1st A1 byte's (STS-1 #1) most significant bit on TTOH1-4. External logic supplying the TTOH1-4 and TTOHEN1-4 must use the TTOHFP1-4 to locate when the MSB (bit #1)of the A1#1 byte should be present on TTOH1-4.

The TTOC blocks sample the TTOH1-4 and TTOHEN1-4 inputs on the rising edge of TTOHCLK1-4. TTOHEN1-4 high during the MSB (bit 1) of TOH byte on TTOH1-4, validates the byte to be inserted into the data stream. In the second half of Figure 28, the first A1 byte will be inserted into the transmit stream since the TTOHEN1-4 is sampled high at the same time that the MSB is sampled. The second A1 byte will not be inserted since the TTOHEN1-4 was not sampled high at the same time as the MSB of the second A1 byte.

An error insertion feature is provided for the H1, H2, B1, and B2 byte positions. When TTOH1-4 is held high during any of the bit positions corresponding to these bytes, the corresponding bit is inverted before being inserted in the transmit stream (TTOHEN1-4 must be sampled high during the first bit position to enable the error insertion mask).

14.2.2 Transmit Section and Line DCC Functional Timing

Figure 29 TX Section DCC Output Timing For D1-D3

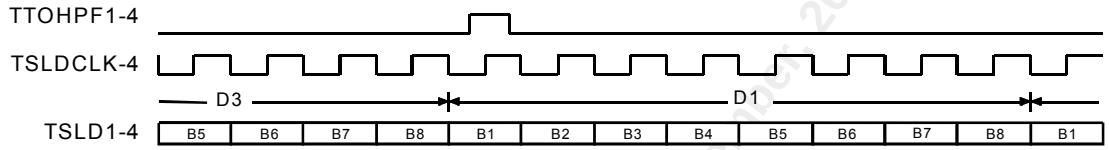


Figure 30 TX Line DCC Output Timing For D4-D12

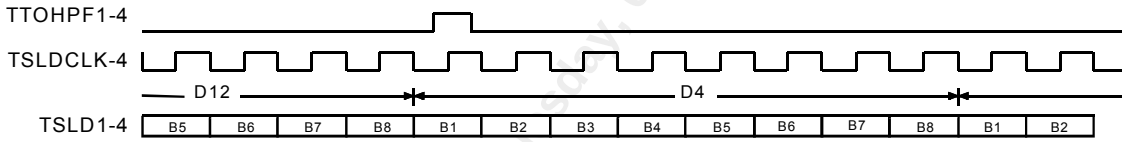


Figure 29 and Figure 30 show the functional timing for the section and line DCC port. The TTOC block generates the TSLDCLK1-4 output clock. TSLDCLK1-4 is programmable (TSLD_SEL) to provide timing for the section or line DCC over the TSLD1-4 serial input. When TSLD_SEL is a logic zero, the TSLD1-4 serial input is set to carry the section DCC (D1 to D3) bytes. In this case TSLDCLK is a 192 kHz clock. When TSLD_SEL is a logic one, the TSLD1-4 serial input is set to carry the line DCC (D4 to D12) bytes. In this case TSLDCL1-4K is a 576 kHz clock. The TSLD1-4 serial input is sampled on the rising edge of TSLDCLK1-4. When TSLD_SEL register bit is programmed low and TSLD1-4 is used to carry the line DCC bytes, the section DCC bytes can be force to all-ones or all-zeros via the TSDVAL register bit. TTOH1-4 and TTOHEN1-4 has precedence over TSDVAL.

The TTOHFP1-4 output is updated on the falling edge of TTOHCLK1-4 but the TSLDCLK1-4 clock is generated such that the rising edge of the clock is able to sample the TTOHFP1-4. Figure 29 and Figure 30 show this relation. TTOHFP1-4 is used to identify the positioning of the D1 or D4 bit 1 (MSB) on TSLD1-4. External logic supplying the TSLD1-4 must use the TTOHFP to locate when the MSB of D1 and D4 should be present on TSLD.

14.3 Receive Path Overhead Extraction

Figure 31 Receive Path Overhead Extraction/Alarm Timing

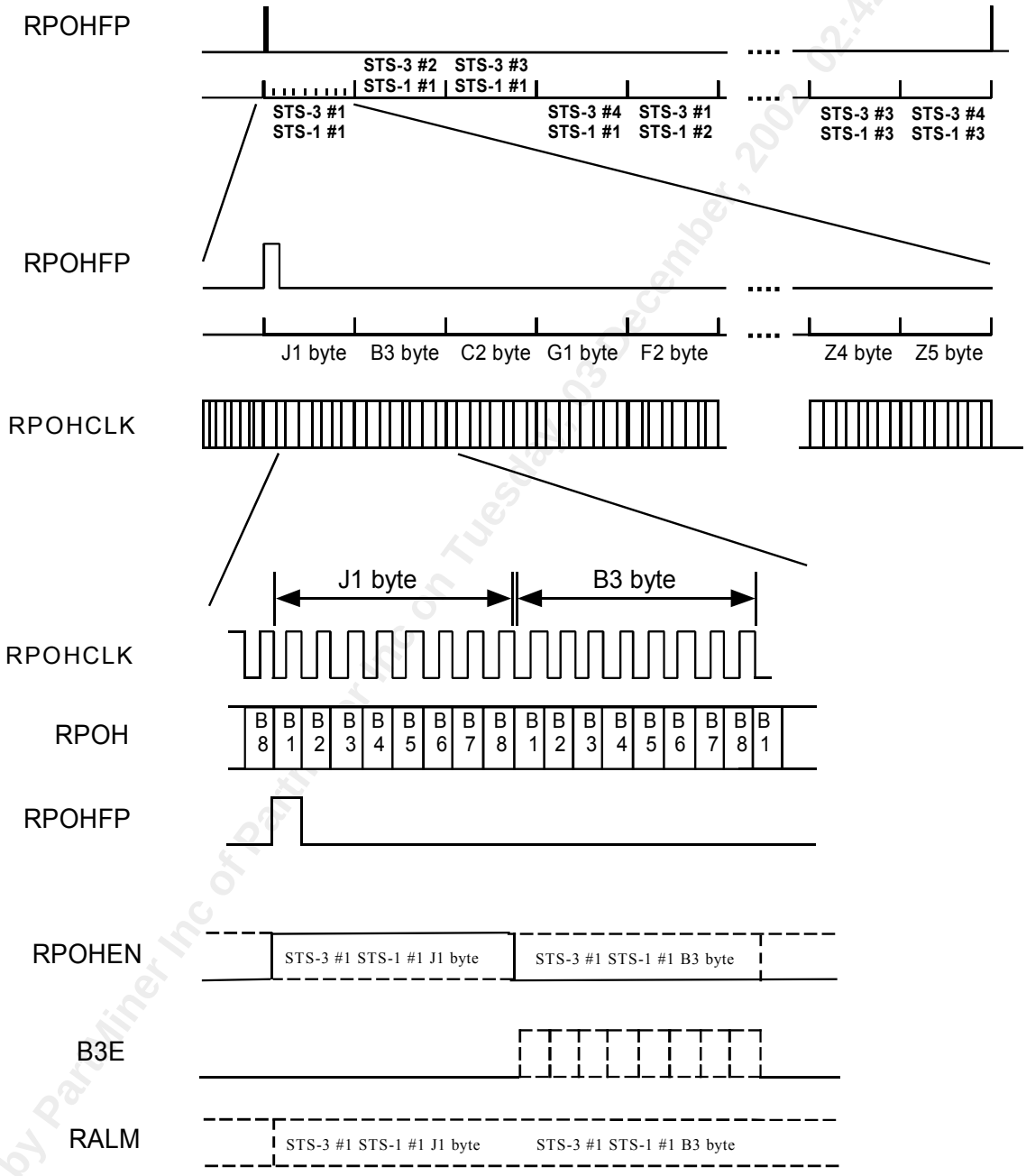


Figure 30 shows the receive path overhead extraction to a serial stream. RPOHCLK is a nominally 12.96 MHz clock and is substantially faster than the actual arrival rate of the receive path overhead bytes. This allows the use of over-sampling to multiplex the path overhead data streams from the RPOPs onto a single RPOH output. The entire path overhead (J1, B3, C2, G1, F2, H4, Z3, Z4, Z5 bytes) of each STS-1 (STM-0/AU-3) in four STS-3 (STM-1/AU-3) receive streams can be extracted, serialized and placed on RPOH over one or two RPOH frame periods. For each byte, the most significant bit (MSB) is transmitted first. RPOHFP marks the most significant bit of the first J1 byte of the STS-12 (STM-4/AU-3). This corresponds to the msb of the J1 byte of STS-3 (STM-1) #1 STS-1 (STM-0/AU-3) #1 stream. The RPOHEN indicates the validity of the path overhead bytes extracted to the RPOH. If a new path overhead byte of a particular STS-1 (STM-0/AU-3) stream is not available during the current time-slot then the RPOHEN is set low. In the above example, the J1 byte of the STS-3 (STM-1) #1 STS-1 (STM-0/AU-3) #1 stream is valid but the B3 byte is not yet available in the current RPOH frame.

The path overhead data streams of corresponding STS-1 (STM-0/AU-3) or equivalent receive streams are arranged in the order of the RPPS numbers (RPPS #1 to RPPS #12). RPPS #1 to #12 always process the SONET/SDH bytes (i.e. STS-1 (STM-0/AU-3) streams) in the received order.. With this assignment, the path overhead data streams are driven on to RPOH in the hierarchical order of STS-3 #1 STS-1 #1, STS-3 #2 STS-1 #1, STS-3 #3 STS-1 #1 - #3) STS-3 #4 STS-1 #1, and etc.

For an STS-3c (STM-1/AU-4), only the path overhead time-slots associated with the equivalent STS-1 (STM-0/AU-3) #1 (processed by a master RPPS) carry valid path overhead bytes when RPOHEN is set high. During the path overhead time-slots of the equivalent STS-1 (STM-0/AU-3) #2 and #3 processed by corresponding slave RPPSs, RPOHEN is always set low.

B3E identifies the bits within the B3 bytes containing a parity error and it is only valid during the B3 byte time-slot of an STS-1 (STM-0/AU-3) or equivalent stream when RPOHEN is set high.

RALM identifies an STS-1 (STM-0/AU-3) or equivalent stream where one or more receive alarm conditions have been detected. The receive alarm conditions which enable an assertion during the corresponding RALM time-slot are controlled by the RPPS RALM Output Control #1 and #2 registers. RALM for each STS-1 (STM-0/AU-3) or equivalent stream may be asserted at any time during the entire period (time-slot) when the corresponding path overhead bytes are serialized on RPOH regardless of the RPOHEN setting. RALM should therefore sampled during the entire time slot period to detect a low-to-high or high-to-low transition.

Figure 32 Receive Tandem Connect Maintenance Insertion Timing

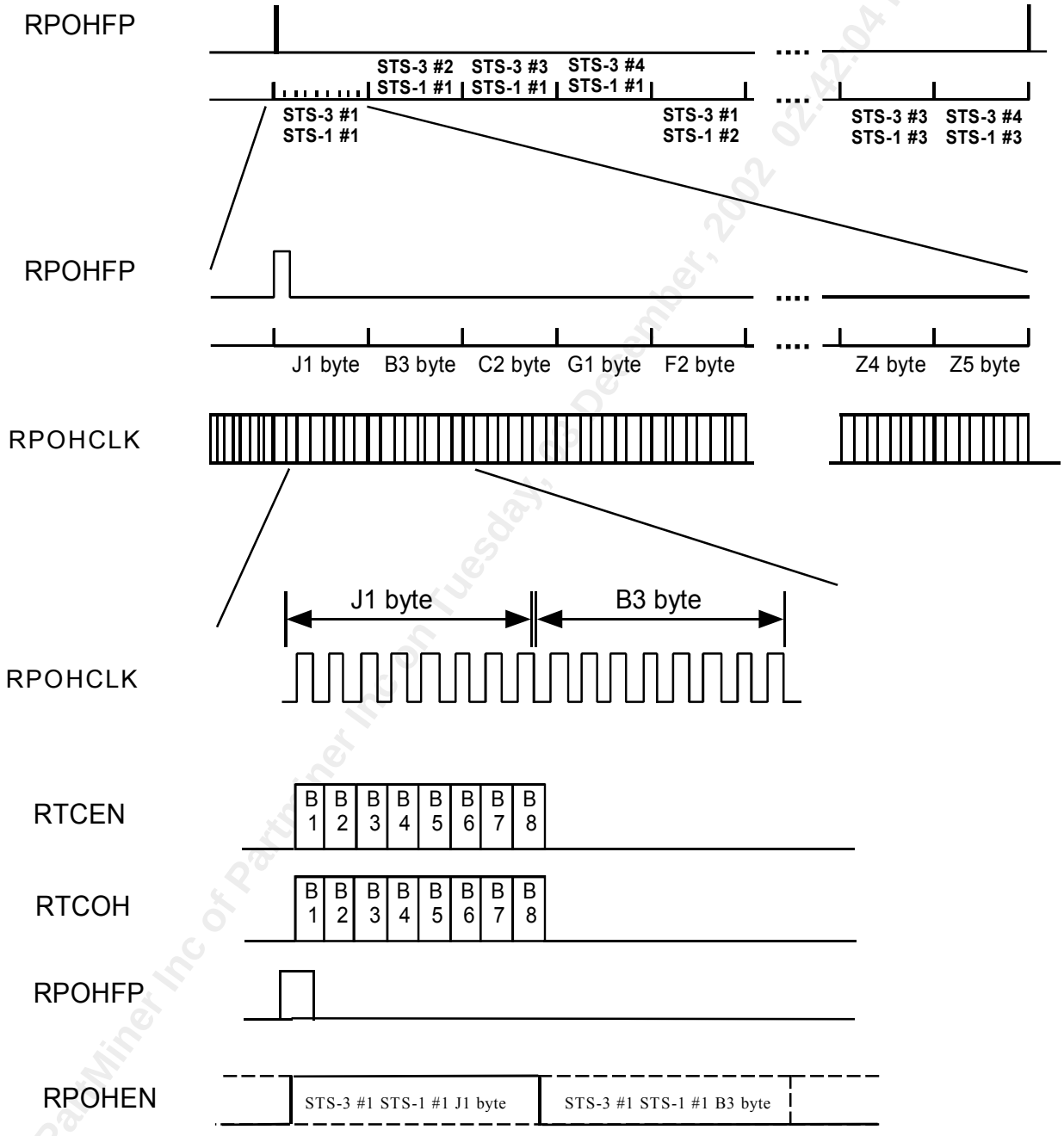
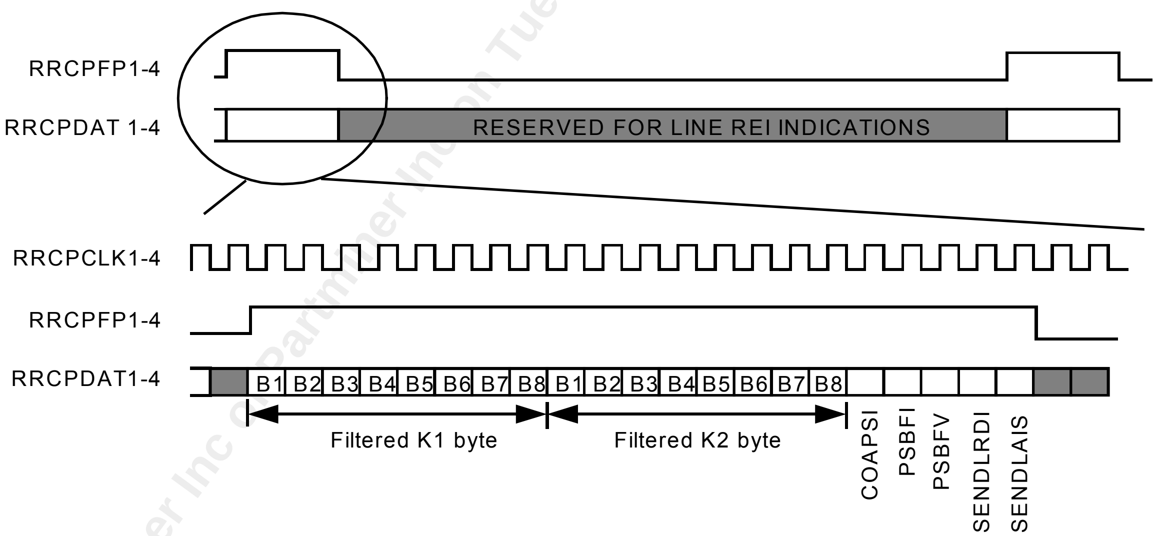


Figure 32 illustrates how the Receive Tandem Connection Maintenance Insertion interface. RTCOH carries the data to be inserted in the tandem connection maintenance byte (Z5) in the Drop bus for each STS-1 (STM-0/AU3) in the four STS-3 (STM-1/AU-3) receive streams. The first bit on RTCOH (B1) corresponds to the most significant bit of Z5. The RTCEN signal controls whether the corresponding bit in RTCOH is inserted in the Z5 byte of a particular STS-1 (STM-0/AU-3) stream. The data bit on RTCOH is inserted in the Z5 byte if the corresponding bit of RTCEN is high. The incoming error count or a logic one data link bit is placed on the Z5 byte if the corresponding bit in RTCEN is low. RTCEN has significance only during the J1 byte positions in the RPOHCLK clock sequence as shown above where RPOHEN is also set high and is ignored at all other times. Figure 32 shows that the Z5 byte for the Drop bus STS-3 (STM-1) #1 STS-1 (STM-0/AU3) #1 stream is accepted. If RPOHEN was low during a particular J1 byte time-slot then the same Z5 insertion must be repeated for the next J1 byte time-slot for the STS-1 (STM-0/AU-3) stream.

For an STS-3c (STM-1/AU-4) receive stream, only the J1 time-slot associated with the equivalent STS-1 (STM-0/AU-3) #1 can be used for Z5 insertion.

14.4 Mate SPECTRA 4x155 Interfaces

Figure 33 Receive Ring Control Port



The timing diagram for the receive ring control port, Figure 33, illustrates the operation of the receive ring control port for each of the device channels when the ring control ports are enabled (using the RCPEN bit in the SPECTRA 4x155 Ring Control register). The control port timing is provided by the RRCPCLK1-4 input. RRCPFP1-4 and RRCPDAT1-4 are updated on the falling edge of RRCPCLK1-4. RRCPFP1-4 is used to distinguish the bit positions carrying alarm status and maintenance signal control information (RRCPFP1-4 is high) from the bit positions carrying line REI indications (RRCPFP1-4 is low). RRCPFP1-4 is high for 21 bit positions once per 125 µs frame. Note: REI indications are enabled using the AUTOLREI bit in the SPECTRA 4x155 Ring Control register.

The first 16 bit positions contain the APS channel byte values after filtering (the K1 and K2 values have been identical for at least three consecutive frames). The 17th bit position, COAPSI, is high for one frame when a new APS channel byte value (after filtering) is received. The 18th and 19th bit positions contain the current protection switch byte failure alarm status. PSBFI is high for one frame when a change in the protection switch byte failure alarm state is detected. PSBFV contains the real-time active high state value of the protection switch byte failure alarm. The 20th and 21st bit positions control the insertion of the line AIS and line RDI maintenance signals in a mate device. The SENDLRDI bit position is controlled by the logical OR of the section/line alarms as enabled by the Line RDI Control Register, or by the SLRDI bit in the Ring Control register. The SENDLAIS bit position is controlled by the SLAIS bit in the Ring Control register.

While RRCPFP is low, RRCPDAT is high for one RRCPCLK cycle for each received REI indication.

Figure 34 Receive Path Alarm Port Timing

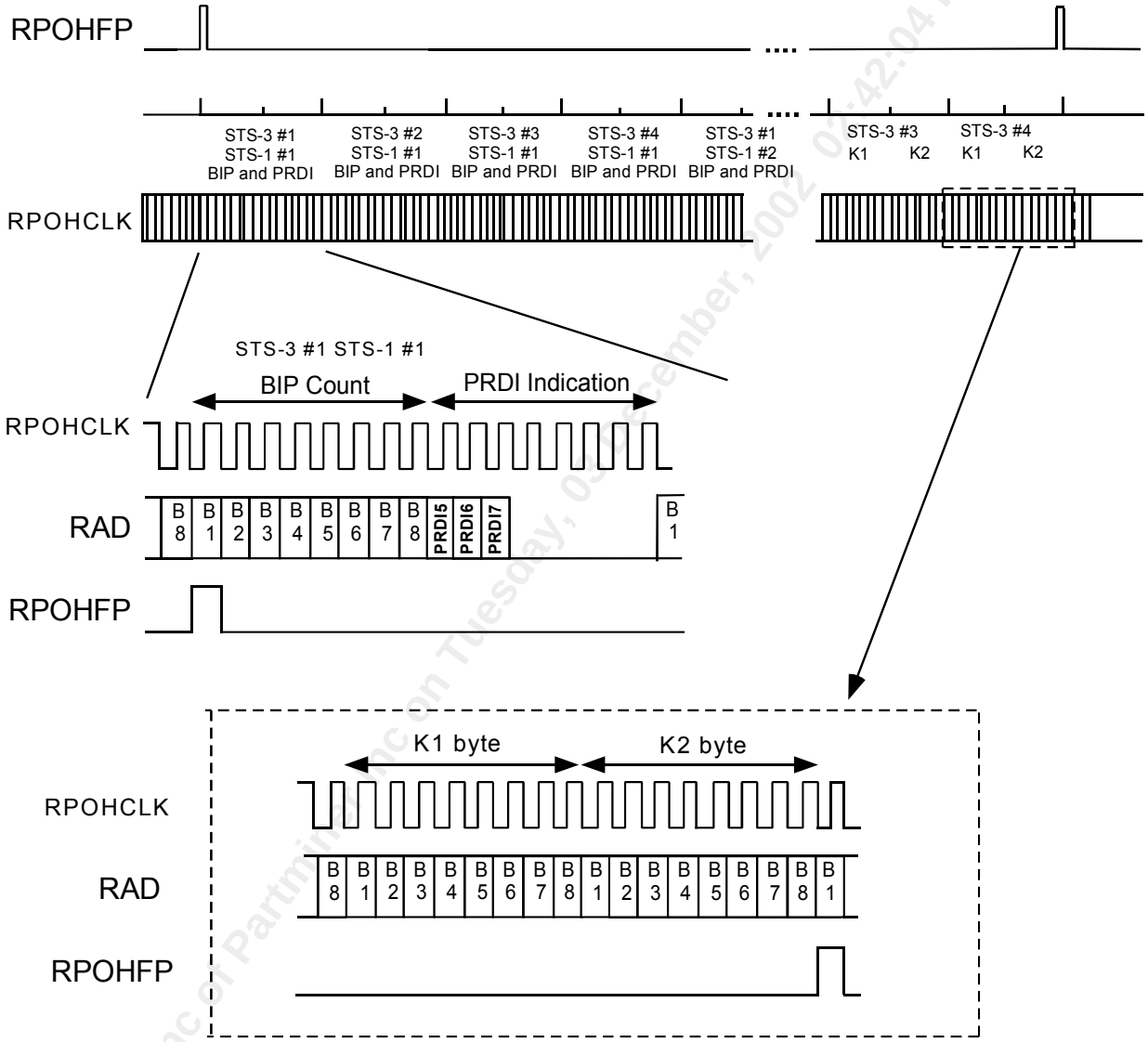
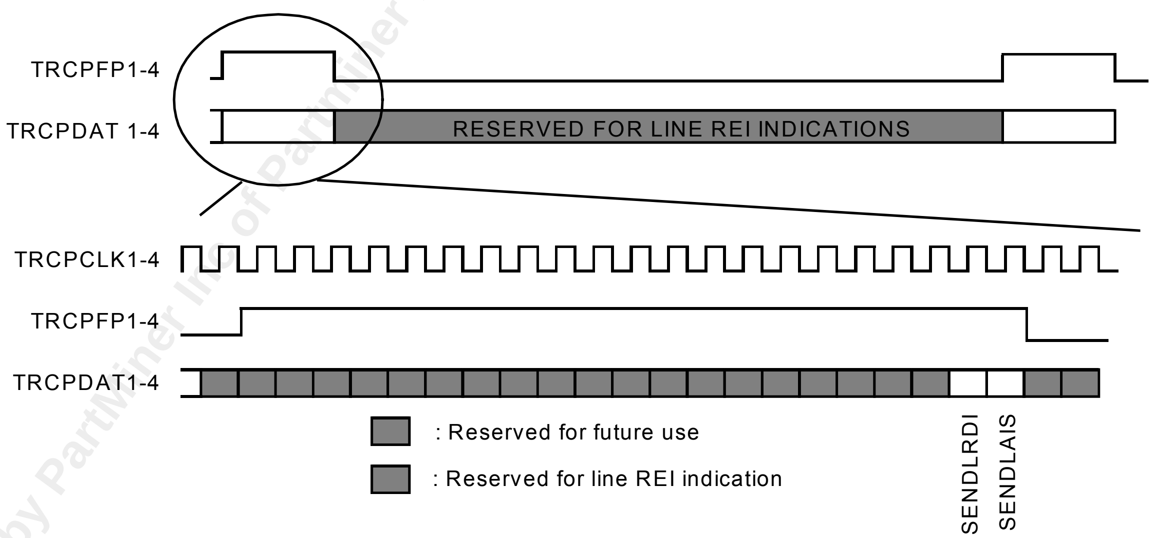


Figure 34 shows the format of the receive path alarm port. The path BIP-8 error counts and the PRDI codes from all STS-1 (STM-0/AU-3) in the four STS-3 (STM-1/AU-3) receive stream are serialized in the receive alarm data output (RAD) and clocked out by RPOHCLK. Output data is updated on the falling edge of RPOHCLK. The eight BIP count bit positions for each STS-1 (STM-0/AU-3) are left justified. If there are eight BIP errors in the corresponding STS-1 (STM-0/AU-3) stream, all bit positions are set high. If there are fewer BIP errors, only the first N positions corresponding to the number of detected errors are set high, the remainder are set low. The PRDI code bits are set when receive alarm conditions are asserted for the corresponding STS-1 (STM-0/AU-3) stream. Note: BIP error indications are enabled using the AUTOPREI bit in the SPECTRA 4x155 RPPS Path REI/RDI Control #1 register. The PRDI5 indications are enabled using bits in the RPPS Path REI/RDI Control registers. The PRDI6 and PRDI7 bits are enabled using bits in the RPPS Path Enhanced RDI Control registers.

When not generating AIS-L on the transmit stream, the transmit APS K1 and K2 bytes of all four channels are also serialized on the RAD during the last eight byte position in the output bit stream. The transmit K1 and K2 bytes can be sourced from the TTOH1-4 input or via the TLOP Transmit K1/K2 registers in order of precedence. Under AIS-L generation on the transmit stream, the K1 and K2 bytes extracted are those which would have been transmitted if it were not for the forcing of AIS-L. AIS-L may be forced on the transmit stream via the TLAIS pin, the transmit ring control port (TRCP) or the TSOP Control Register 0m80h.

For an STS-3c (STM-1/AU-4) receive stream, only the BIP Count and PRDI code time-slots associated with the equivalent STS-1 (STM-0/AU-3) #1 carry valid information. The BIP Count and PRDI code time-slots of the equivalent STS-1 (STM-0/AU-3) #2 and #3 should be ignored.

Figure 35 Transmit Ring Control Port



The timing diagram for the transmit ring control port, Figure 36, illustrates the operation of the transmit ring control port for each of the device channels when the ring control ports are enabled (using the RCPEN bit in the Ring Control Register). The control port timing is provided by the TRCPCLK1-4 input. TRCPFP1-4 and TRCPDAT1-4 are sampled on the rising edge of TRCPCLK1-4. TRCPFP1-4 is used to distinguish the bit positions carrying maintenance signal control information (TRCPFP1-4 is high) from the bit positions carrying line REI indications (TRCPFP is low). TRCPFP1-4 is high for 21 bit positions once per frame 125 µs). Currently, only the last two bit positions are used. These bit positions control the insertion of line RDI and line AIS maintenance signals as illustrated. The remaining 19 bit positions are reserved for future feature enhancements.

Figure 36 Transmit Alarm Port Timing

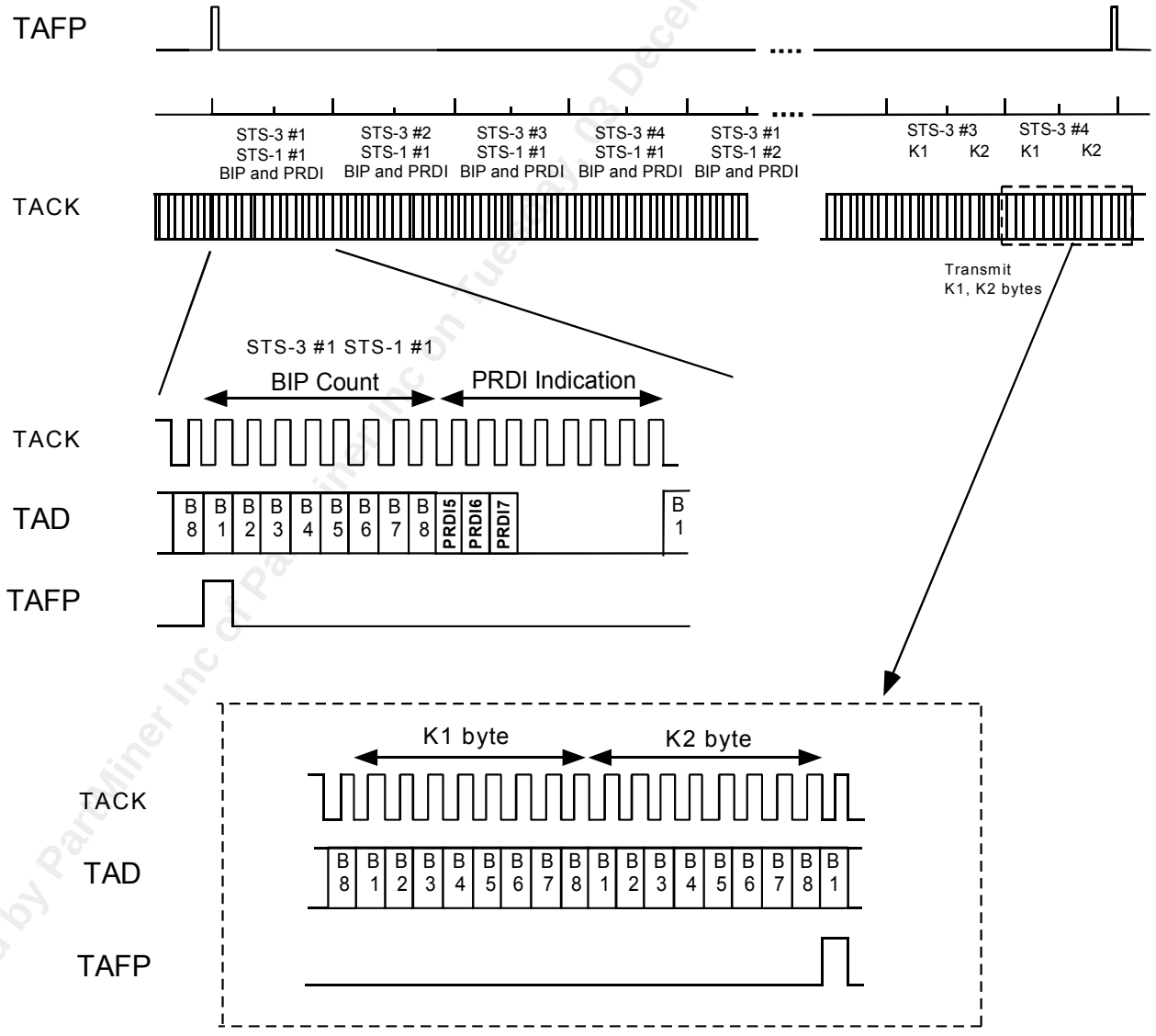


Figure 36 shows the format of the transmit path alarm port. The path BIP-8 error counts and PRDI codes for all STS-1 (STM-0/AU-3) in all four STS-3 (STM-1/AU-3) transmit streams are serialized in the transmit alarm data input (TAD) and clocked in by TACK. The eight BIP count bit positions for each STS-1 (STM-0/AU-3) are left justified. If there are eight BIP errors in the corresponding STS-1 (STM-0/AU-3) stream, all bit positions are set high. If there are fewer BIP errors, only the first N positions corresponding to the number of detected errors are set high, the remainder are set low. The PRDI code bits (PRDI5, PRDI6, PRDI7) are set accordingly when the corresponding STS-1 (STM-0/AU-3) stream in the peer receive section inserts an RDI condition to be relayed back to the far end. The transmit APS K1 and K2 bytes of all four channels can also be sourced from TAD stream during the last height byte position in the input bit stream. Input data is sampled on the rising edge of TACK.

For an STS-3c (STM-1/AU-4) transmit stream, only the BIP Count and PRDI code time-slots associated with the equivalent STS-1 (STM-0/AU-3) #1 can be used. The TAD input must be set low during the BIP Count and PRDI code time-slots of the equivalent STS-1 (STM-0/AU-3) #2 and #3.

The TAD port can accumulate up to 15 BIP errors. Given the timings of the RAD port, a mate SPECTRA 4x155 could output 16 errors within one frame period. If eight errors are detected in two consecutive frames and the timing makes them appear within one frame period, the 16th count could be lost.

14.5 Telecom Bus System Side

14.5.1 Drop Bus

Figure 37 STS-3 (STM-1/AU-3) 19.44 MHz Byte Drop Bus Timing

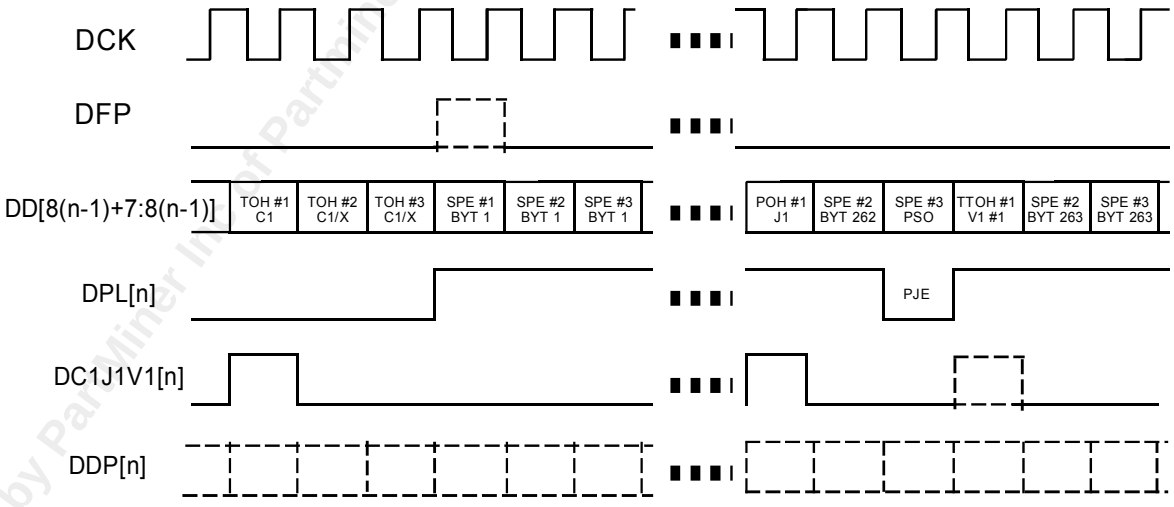


Figure 38 shows the STS-3 (STM-1/AU-3) 19.44 MHz byte Drop bus timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom Drop buses. DCK is a 19.44 MHz clock. The frame pulse DFP marks the first SPE byte in the STS-3 (STM-1/AU-3) frame on DD[7:0] (DD[31:24], DD[23:16], DD[15:8]). It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL[1] (DPL[4], DPL[3], DPL[2]) output which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-1 (STM-0/AU-3) #3. A stuff byte is place in the positive stuff opportunity byte position and DPL[1] (DPL[4:2]) is set low to indicate that data is not available. The Drop bus composite timing signal DC1J1V1[1] (DC1J1V1[4], DC1J1V1[3], DC1J1V1[2]) is set high when DPL[1] (DPL[4:2]) is set low to mark the C1 byte. DC1J1V1[1] (DC1J1V1[4:2]) is set high when DPL[1] (DPL[4:2]) is also set high to mark the J1 byte in each of the three STS-1 (STM-0/AU-3) streams. Optionally, DC1J1V1[1] (DC1J1V1[4:2]) is set high once every multi-frame to mark the first frame of the Drop bus tributary multi-frame in each STS-1 (STM-0/AU-3) stream. The alignment of the transport frame and the SPE of STS-1 (STM-0/AU-3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom Drop buses may be different. The Drop bus parity output DDP[1] (DDP[4], DDP[3], DDP[2]) reports the parity of DD[7:0] (DD[31:24], DD[23:16], DD[15:8]) and optionally includes DPL[1] (DPL[4:2]) and DC1J1V1[1] (DC1J1V1[4:2]).

Figure 38 STS-3c (STM-1/AU-4) 19.44 MHz Byte Drop Bus Timing

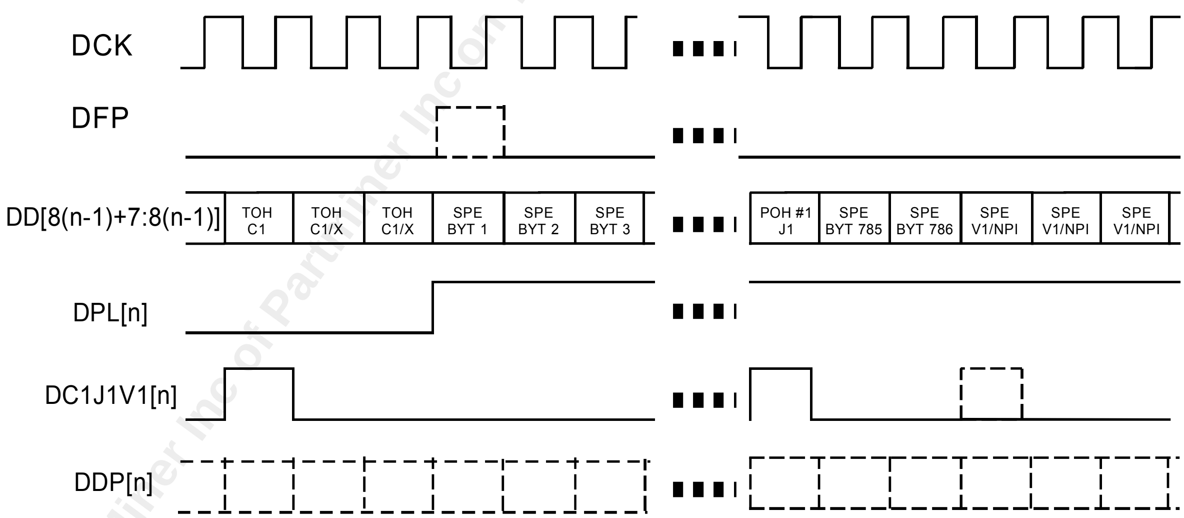


Figure 38 shows the STS-3c (STM-1/AU-4) 19.44 MHz byte Drop bus timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom Drop buses. DCK is a 19.44 MHz clock. The frame pulse DFP marks the first SPE byte on DD[7:0] (DD[31:24], DD[23:16], DD[15:8]). It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL[1] (DPL[4], DPL[3], DPL[2]) output which is set low to mark transport overhead bytes and set high to mark payload bytes. The Drop bus composite timing signal DC1J1V1[1] (DC1J1V1[4], DC1J1V1[3], DC1J1V1[2]) is set high when DPL[1] (DPL[4:2]) is set low to mark the C1 byte. DC1J1V1[1] (DC1J1V1[4:2]) is set high when DPL[1] (DPL[4:2]) is also set high to mark the J1 byte of the STS-3c (STM-1/AU-4) stream. Optionally, DC1J1V1[1] (DC1J1V1[4:2]) is set high once every multi-frame to mark the first frame of the Drop bus tributary multi-frame. When processing an STS-3c (STM-1/AU-4) stream, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multi-frame. The alignment of the transport frame and the SPE of STS-3c (STM-1/AU-4) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom Drop buses may be different. The Drop bus parity output DDP[1] (DDP[4], DDP[3], DDP[2]) reports the parity of DD[7:0] (DD[31:24], DD[23:16], DD[15:8]) and optionally includes DPL[1] (DPL[4:2]) and DC1J1V1[1] (DC1J1V1[4:2]).

Figure 39 STS-12 (STM-4/AU-3) 77.76 MHz Byte Drop Bus Timing

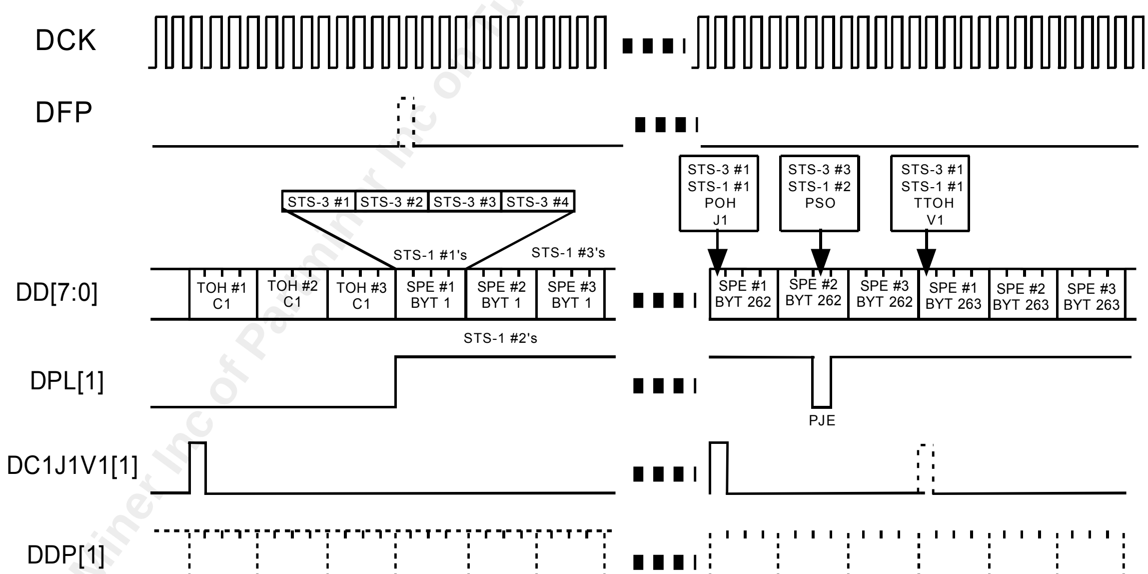


Figure 39 shows the STS-12 (STM-4/AU-3) 77.76 MHz byte Drop bus timing. DCK is a 77.76 MHz clock. The frame pulse DFP marks the first SPE byte in the STS-12 (STM-4/AU-3) frame on DD[7:0]. This is also the first SPE byte of STS-3 (STM-1) #1 STS-1 (STM-0/AU-3) #1 stream. It is not necessary for DFP to be present at every frame. An internal counter fly-wheels based on the most recent DFP received. Transport overhead and payload bytes are distinguished by the DPL[1] output which is set low to mark transport overhead bytes and set high to mark payload bytes. A positive justification event is shown for STS-3 (STM-1) #3 STS-1 (STM-0/AU-3) #2. A stuff byte is place in the positive stuff opportunity byte position and DPL[1] is set low to indicate that data is not available. The Drop bus composite timing signal DC1J1V1[1] is set high when DPL[1] is set low to mark the first C1 byte of the STS-12 (STM-4/AU-3) frame. DC1J1V1[1] is set high when DPL[1] is also set high to mark the J1 byte in each of the STS-1 (STM-0/AU-3) streams. Optionally, DC1J1V1[1] is set high once every multi-frame to mark the first frame of the Drop bus tributary multi-frame in each STS-1 (STM-0/AU-3) stream. The alignment of the transport frame and the SPE of STS-3 (STM-1) #1 STS-1 (STM-0/AU-3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The Drop bus parity output DDP[1] reports the parity of DD[7:0] and optionally includes DPL[1] and DC1J1V1[1].

14.5.2 Add Bus

Figure 40 STS-3 (STM-1/AU-3) 19.44 MHz Byte Add Bus Timing

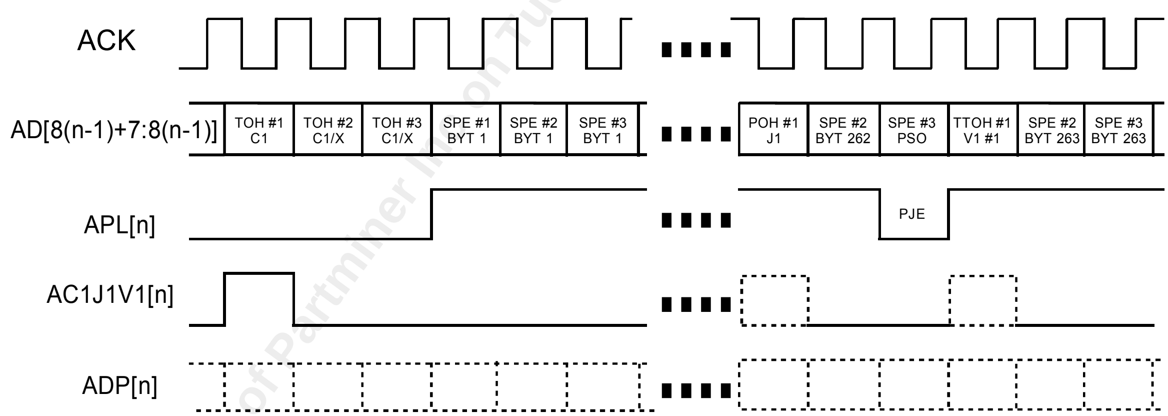


Figure 40 shows the STS-3 (STM-1/AU-3) 19.44 MHz byte Add bus timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom Add buses. ACK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the APL[1] (APL[4], APL[3], APL[2]) input which is set low to mark transport overhead bytes and set high to mark payload bytes on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]). A positive justification event is shown for STS-1 (STM-0/AU-3) #3. A stuff byte is place in the positive stuff opportunity byte and APL[1] (APL[4], APL[3], APL[2]) is set low to indicate that data is not available. The Add bus composite timing signal AC1J1V1[1] (AC1J1V1[4], AC1J1V1[3], AC1J1V1[2]) is set high when APL[1] (APL[4:2]) is set low to mark the C1 byte. Optionally, AC1J1V1[1] (AC1J1V1[4:2]) is set high when APL[1] (APL[4:2]) is also set high to mark the J1 byte in each of the three STS-1 (STM-0/AU-3) streams. Optionally, AC1J1V1[1] (AC1J1V1[4:2]) is set high once every multi-frame to mark the first frame of the Add bus tributary multi-frame in each STS-1 (STM-0/AU-3) stream. The alignment of the transport frame and the SPE of STS-1 (STM-0/AU-3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom Add buses may be different. The Add bus parity input ADP[1] (ADP[4], ADP[3], ADP[2]) carries the parity of AD[7:0] (AD[31:24], AD[23:16], AD[15:8]) and optionally includes APL[1] (APL[4:2]) and AC1J1V1[1] (AC1J1V1[4:2]).

Figure 41 STS-3 (STM-1/AU-3) 19.44 MHz Byte Add Bus (AFP) Timing

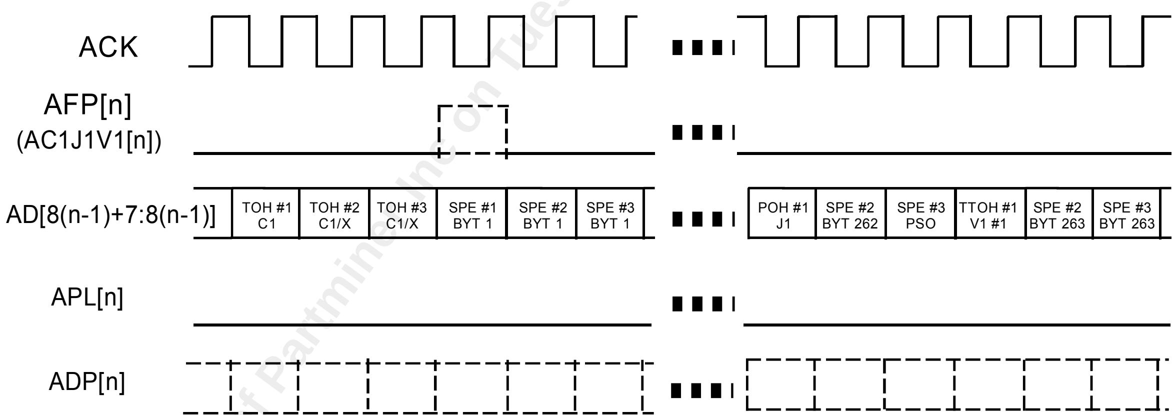


Figure 41 shows the STS-3 (STM-1/AU-3) 19.44 MHz byte Add bus (AFP) timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom Add buses. ACK is a 19.44 MHz clock. The frame pulse AFP[1] (AFP[4], AFP[3], AFP[2]) marks the first SPE byte in the STS-3 (STM-1/AU-3) frame on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]). It is not necessary for AFP[n] to be present at every frame. An internal counter fly-wheels based on the most recent AFP[n] received. In this system interface mode, valid H1, H2 pointer bytes must be provided on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]) and the APL[1] (APL[4:2]) input signal must be strapped low. Transport overhead and payload bytes are distinguished by interpreting the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame and pointer justification events are also determined via the H1 and H2 pointer bytes. Optionally, the first frame of the Add bus tributary multi-frame in each STS-1 (STM-0/AU-3) stream is determined by interpreting the H4 byte in the corresponding path overhead. The alignment of the transport frame and the SPE of STS-1 (STM-0/AU-3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom Add buses may be different. The Add bus parity input ADP[1] (ADP[4], ADP[3], ADP[2]) carries the parity of AD[7:0] (AD[31:24], AD[23:16], AD[15:8]).

Figure 42 STS-3c (STM-1/AU-4) 19.44 MHz Byte Add Bus Timing

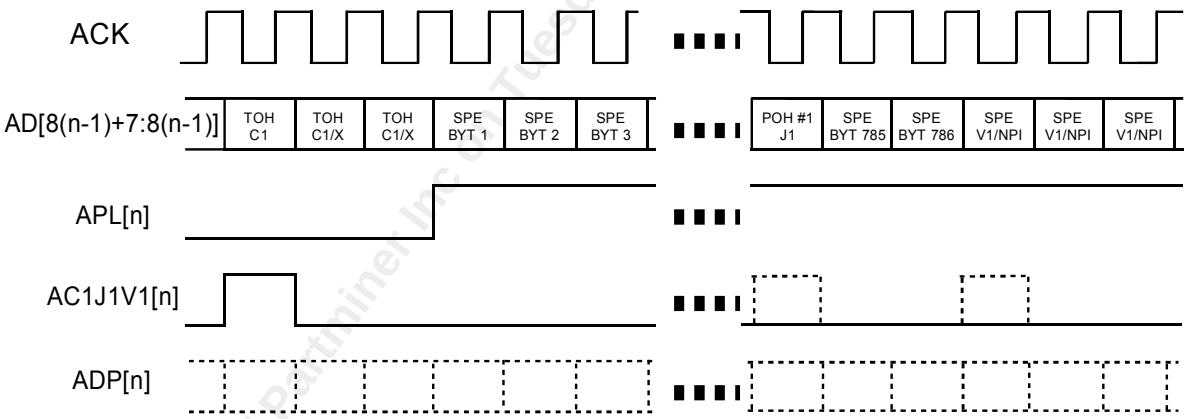


Figure 42 shows the STS-3c (STM-1/AU-4) 19.44 MHz byte Add bus timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom Add buses. ACK is a 19.44 MHz clock. Transport overhead and payload bytes are distinguished by the APL[1] (APL[4], APL[3], APL[2]) input which is set low to mark transport overhead bytes and set high to mark payload bytes on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]). The Add bus composite timing signal AC1J1V1[1] (AC1J1V1[4], AC1J1V1[3], AC1J1V1[2]) is set high when APL[1] (APL[4:2]) is set low to mark the C1 byte. Optionally, AC1J1V1[1] (AC1J1V1[4:2]) is set high when APL[1] (APL[4:2]) is also set high to mark the J1 byte. Optionally, AC1J1V1[1] (AC1J1V1[4:2]) is set high once every multi-frame to mark the first frame of the Add bus tributary multi-frame. When processing an STS-3c (STM-1/AU-4) stream, the V1 pulse marks the more significant byte of the Null Pointer Indication (NPI) of the first frame in each tributary multi-frame. The alignment of the transport frame and the SPE of STS-3c (STM-1/AU-4) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom Add buses may be different. The Add bus parity input ADP[1] (ADP[4], ADP[3], ADP[2]) carries the parity of AD[7:0] (AD[31:24], AD[23:16], AD[15:8]) and optionally includes APL[1] (APL[4:2]) and AC1J1V1[1] (AC1J1V1[4:2]).

Figure 43 STS-3c (STM-1/AU-4) 19.44 MHz Byte Add Bus (AFP) Timing

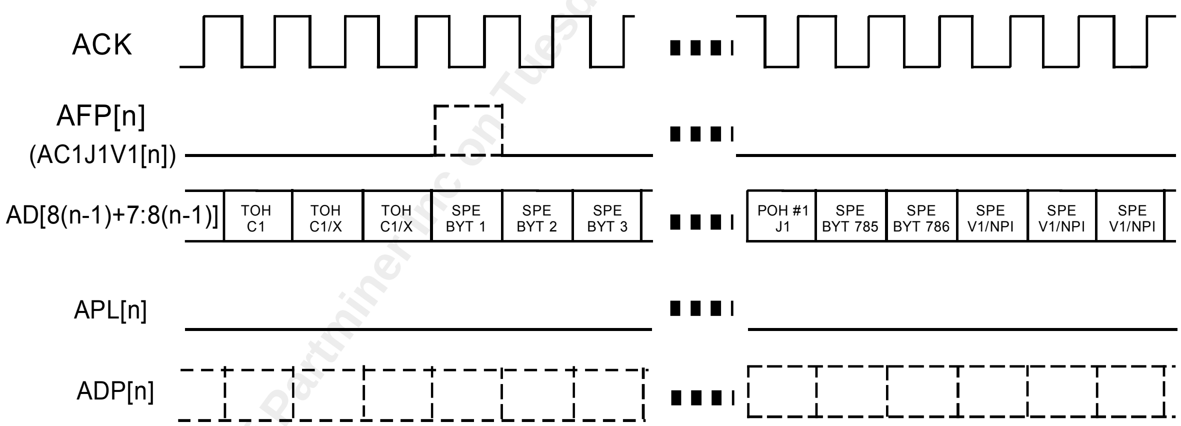


Figure 43 shows the STS-3c (STM-1/AU-4) 19.44 MHz byte Add bus (AFP) timing where n is {1, 2, 3, 4}. This timing applies to all four 19.44 MHz Byte Telecom Add buses. ACK is a 19.44 MHz clock. The frame pulse AFP[1] (AFP[4], AFP[3], AFP[2]) marks the first SPE byte in the STS-3c (STM-1/AU-4) frame on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]). It is not necessary for AFP[n] to be present at every frame. An internal counter fly-wheels based on the most recent AFP[n] received. In this system interface mode, valid H1, H2 pointer bytes must be provided on AD[7:0] (AD[31:24], AD[23:16], AD[15:8]) and the APL[1] (APL[4:2]) input signal must be strapped low. Transport overhead and payload bytes are distinguished by interpreting the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame and pointer justification events are also determined via the H1 and H2 pointer bytes. Optionally, the V1 byte in the first frame of the Add bus tributary multi-frame is determined by interpreting the H4 byte in the corresponding path overhead. The alignment of the transport frame and the SPE of STS-3c (STM-1/AU-4) stream shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. Also, the SPE alignments of the four 19.44 MHz Byte Telecom Add buses may be different. The Add bus parity input ADP[1] (ADP[4], ADP[3], ADP[2]) carries the parity of AD[7:0] (AD[31:24], AD[23:16], AD[15:8]).

Figure 44 STS-12 (STM-12/AU-3) 77.76 MHz Byte Add Bus Timing

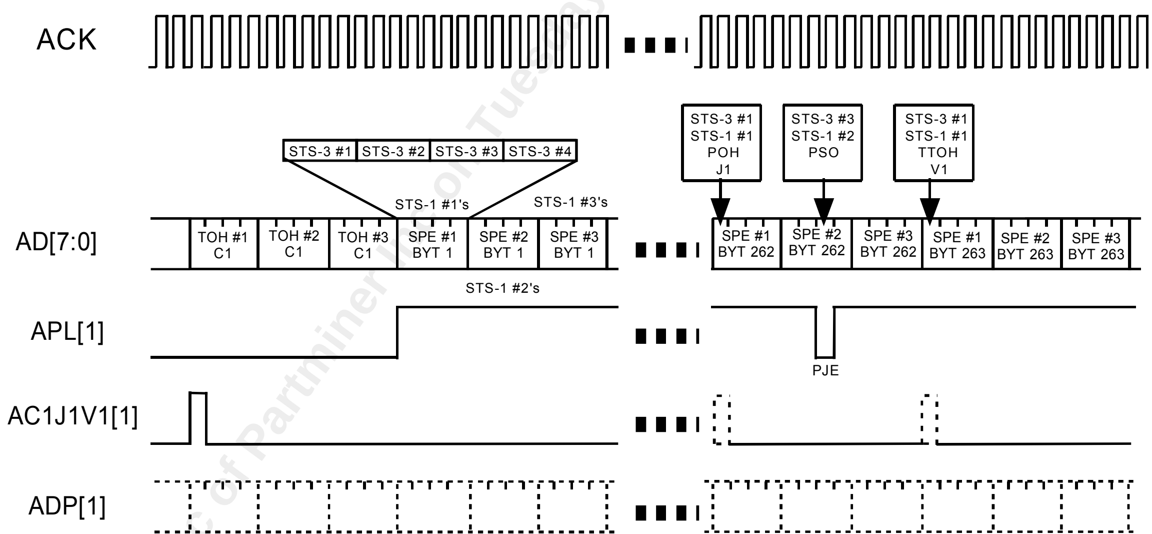


Figure 44 shows the STS-12 (STM-4/AU-3) 77.76 MHz byte Add bus timing. ACK is a 77.76 MHz clock. Transport overhead and payload bytes are distinguished by the APL[1] input which is set low to mark transport overhead bytes and set high to mark payload bytes on AD[7:0]. A positive justification event is shown for STS-3 (STM-1) #3 STS-1 (STM-0/AU-3) #2. A stuff byte is place in the positive stuff opportunity byte and APL[1] is set low to indicate that data is not available. The Add bus composite timing signal AC1J1V1[1] is set high when APL[1] is set low to mark the first C1 byte. Optionally, AC1J1V1[1] is set high when APL[1] is also set high to mark the J1 byte in each of the STS-1 (STM-0/AU-3) streams. Optionally, AC1J1V1[1] is set high once every multi-frame to mark the V1 byte of first frame of the Add bus tributary multi-frame in each STS-1 (STM-0/AU-3) stream. The alignment of the transport frame and the SPE of STS-3 #1 STS-1 (STM-0/AU-3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The Add bus parity input ADP[1] carries the parity of AD[7:0] and optionally includes APL[1] and AC1J1V1[1].

Figure 45 STS-12 (STM-12/AU-3) 77.76 MHz Byte Add Bus (AFP) Timing

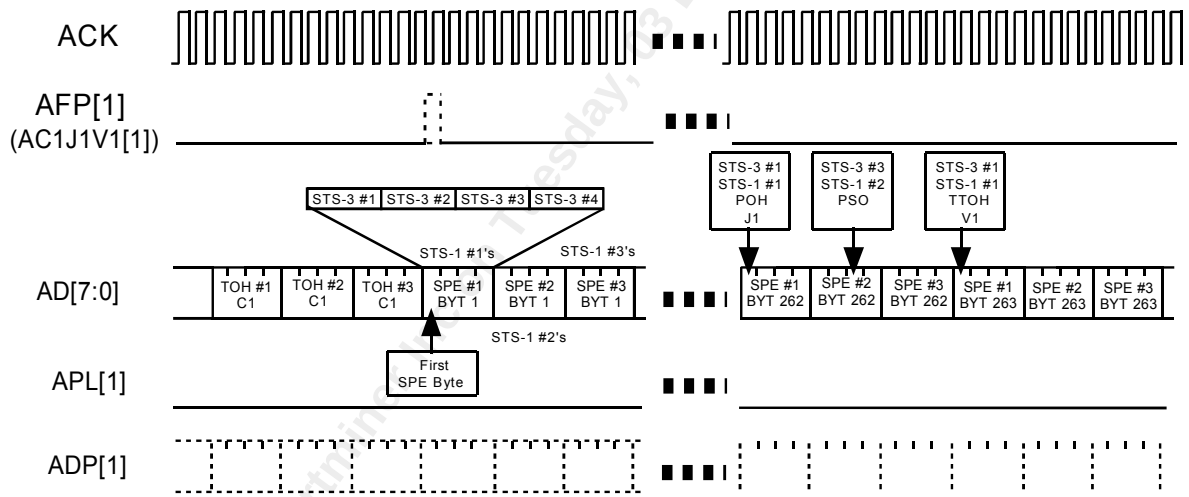


Figure 45 shows the STS-12 (STM-4/AU-3) 77.76 MHz byte Add bus (AFP) timing. ACK is a 77.76 MHz clock. The frame pulse AFP[1] marks the first SPE byte in the STS-12 (STM-4/AU-3/AU-4) frame on AD[7:0]. It is not necessary for AFP[1] to be present at every frame. An internal counter fly-wheels based on the most recent AFP[1] received. In this system interface mode, valid H1, H2 pointer bytes must be provided on AD[7:0] for each STS-1 (STM-0/AU-3) or equivalent stream and the APL[1] input must be strapped low. Transport overhead and payload bytes are distinguished by interpreting the H1 and H2 pointer bytes. The phase relation of the SPE (VC) to the transport frame and pointer justification events are also determined via the H1 and H2 pointer bytes. Optionally, the V1 byte in the first frame of the Add bus tributary multi-frame for each STS-1 (STM-0/AU-3) or equivalent stream is determined by interpreting the H4 byte in the corresponding path overhead. The alignment of the transport frame and the SPE of STS-3 #1 STS-1 (STM-0/AU-3) #1 shown corresponds to an active offset of 0 and is for illustration only. Other alignments are possible. The Add bus parity input ADP[1] carries the parity of AD[7:0].

14.6 System Side Path AIS Control Port

Figure 46 System Drop Side Path AIS Control Port Timing

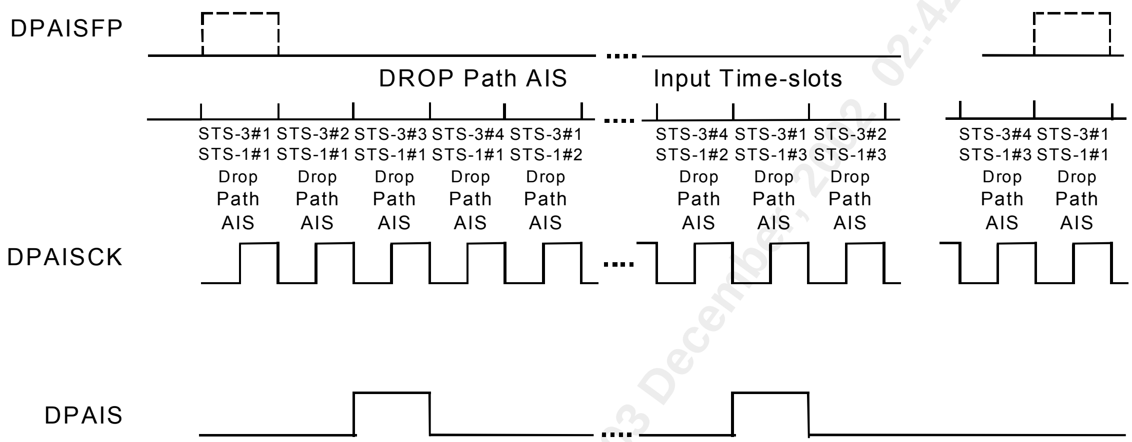


Figure 46 shows the System Drop Side Path AIS Control Port timing. The frame pulse DPAISFP marks the first STS-1 (STM-0/AU-3) or equivalent Drop bus path AIS assertion control signal on the DPAIS input. It is not necessary for DPAISFP to be present at every frame. An internal counter fly-wheels based on the most recent DPAISFP received. The DPAISFP and DPAIS inputs are sampled on the rising edge of DPAISCK. The path AIS assertion control signals are multiplexed according to the hierarchical order of STS-3 #1 (STS-1 #1 - #3), STS-3 #2 (STS-1 #1 - #3), STS-3 #3 (STS-1 #1 - #3) and STS-3 #4 (STS-1 #1 - #3) for the 12 STS-1 (STM-0/AU-3) or equivalent receive streams. The above figure shows Drop bus path AIS assertion for the STS-3 (STM-1) #1 STS-1 (STM-0/AU-3) #1 and STS-3 (STM-1) #3 STS-1 (STM-0/AU-3) #3 receive streams. The DPAIS must be set high during the above time-slots in consecutive DPAIS frames for continuous path AIS assertion. Each slice samples the corresponding DPAIS signal once per frame. Path AIS assertion of a stream is removed when the corresponding DPAIS time-slot is set low.

The time-slot assignment on DPAIS is unrelated to the configuration of the STS (STM) groups in the receive streams. For a concatenated stream, only the time-slots associated with the equivalent STS-1 (STM-0/AU-3) #1 can be used. DPAIS must be set low during the time-slots for the remaining STS-1 (STM-0/AU-3) equivalent streams in the concatenated stream.

Figure 47 System Add Side Path AIS Control Port Timing

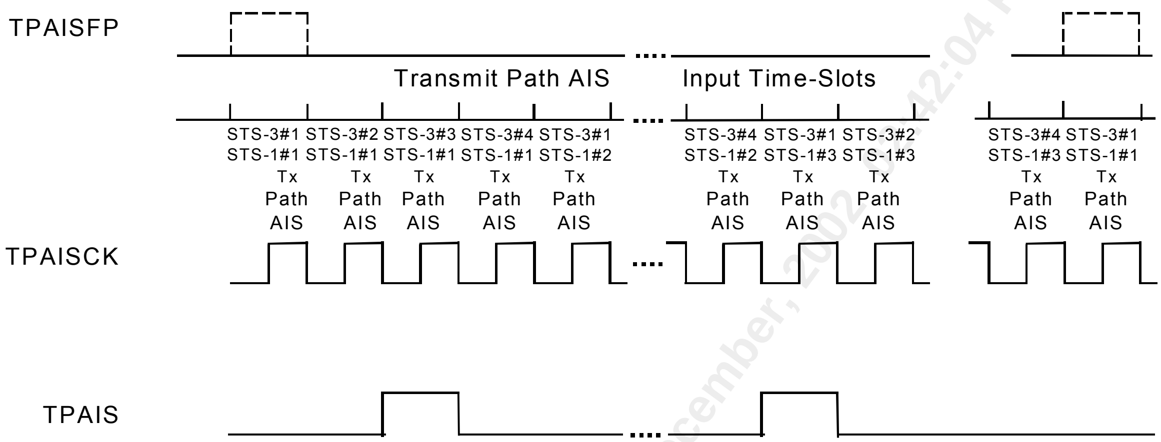


Figure 47 shows the System Add Side Path AIS Control Port timing. The frame pulse TPAISFP marks the first STS-1 (STM-0/AU-3) or equivalent transmit stream path AIS assertion control signal on the TPAIS input. It is not necessary for TPAISFP to be present at every frame. An internal counter fly-wheels based on the most recent TPAISFP received. The TPAISFP and TPAIS inputs are sampled on the rising edge of TPAISCK. The path AIS assertion control signals are multiplexed according to the hierarchical order of STS-3 #1 (STS-1 #1 - #3), STS-3 #2 (STS-1 #1 - #3), STS-3 #3 (STS-1 #1 - #3) and STS-3 #4 (STS-1 #1 - #3) for the 12 STS-1 (STM-0/AU-3) or equivalent transmit streams. The above figure shows transmit path AIS assertion for the STS-3 (STM-1) #1 STS-1 (STM-0/AU-3) #1 and STS-3 (STM-1) #3 STS-1 (STM-0/AU-3) #3 streams. The TPAIS must be set high during the above time-slots in consecutive TPAIS frames for continuous path AIS assertion. Each slice samples the corresponding DPAIS signal once per frame. Path AIS assertion of a stream is removed when the corresponding TPAIS time-slot is set low.

The time-slot assignment on TPAIS is unrelated to the configuration of the STS (STM) groups in the transmit stream. For a concatenated stream, only the time-slots associated with the equivalent STS-1 (STM-0/AU-3) #1 can be used. TPAIS must be set low during the time-slots for the remaining STS-1 (STM-0/AU-3) equivalent streams in the concatenated stream.

15 Absolute Maximum Ratings

Maximum ratings are the worst-case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 29 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
Supply Voltage	-0.3V to +4.6V
Bias Voltage (V_{BIAS})	(V_{DD} - .3) to +5.5V
Voltage on PECL Pin	-0.3V to V_{BIAS}+0.3V
Voltage on Any Digital Pin	-0.3V to ~~V_{VDD}~~V_{BIAS}+0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

16 D.C. Characteristics

T_A = -40°C to +85°C, V_{DD} = 3.3V ± 5%, V_{AVD} = 3.3V ± 5%, V_{DD} < BIAS < 5.5V
(Typical Conditions: ~~T_C~~ T_A = 25°C, V_{DD} = 3.3V, V_{AVD} = 3.3V , V_{BIAS} = 5V)

Table 30 D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	3.14	3.3	3.47	Volts	—
BIAS	5V Tolerant Bias	VDD	5.0	5.5	Volts	—
V_{IL}	Input Low Voltage	0	—	0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0	—		Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		—	0.4	Volts	Guaranteed output Low voltage at VDD=3.14V and I_{OL}=maximum rated for pad. [4]
V_{OH}	Output or Bi-directional High Voltage	2.4	—	—	Volts	Guaranteed output High voltage at VDD=3.14V and I_{OH}=maximum rated current for pad. [4]
V_{T+}	Reset Input High Voltage	2.0	—	—	Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage		—	0.8	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage	—	0.4		Volts	Applies to RSTB and TRSTB only.
VPECLI+	Input PECL High Voltage	V_{PECL} - 1.165	V_{PECL} - 0.955	V_{PECL} - 0.880	Volts	Applies to PECL inputs RXD[4:1]+/-, SD[4:1].
VPECLI-	Input PECL Low Voltage	V_{PECL} - 1.810	V_{PECL} - 1.700	V_{PECL} - 1.475	Volts	Applies to PECL inputs RXD[4:1]+/-, SD[4:1].
I_{ILPU}	Input Low Current	-100		-4	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10		10	µA	V_{IH} = V_{DD}. Notes 1 and 3.
I_{IL}	Input Low Current	-10		+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10		+10	µA	V_{IH} = V_{DD}. Notes 2 and 3.
$I_{IL\ PECL}$	Input Low Current	-10	0	+100	µA	PECL inputs only. Note 3
$I_{IH\ PECL}$	Input High Current	-100	0	+10	µA	PECL inputs only. Note 3
C_{IN}	Input Capacitance	—	5	—	pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance	—	5	—	pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance	—	5	—	pF	t_A=25°C, f = 1 MHz
IDDOP	Operating Current	—	730	~~950~~860	mA	VDD = 3.47V, Vbias = 5.5 V, 25C, Outputs Unloaded

Notes

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor

3. Negative current flows into the device (sinking), positive current flows out of the device (sourcing).
4. Refer to the footnotes at the bottom of the Pin Description table, section 9 for the DC current rating of each device output.

17 Microprocessor Interface Timing Characteristics

(~~T~~C-TA = -40°C to +85°C, V_{DD} = 3.3V ± 5%, V_{AVD} = 3.3V ± 5%)

Table 31 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
TS_{AR}	Address to Valid Read Set-up Time	10	—	ns
TH_{AR}	Address to Valid Read Hold Time	5	—	ns
TS_{ALR}	Address to Latch Set-up Time	10	—	ns
TH_{ALR}	Address to Latch Hold Time	10	—	ns
TV_{L}	Valid Latch Pulse Width	5	—	ns
TS_{LR}	Latch to Read Set-up	0	—	ns
TH_{LR}	Latch to Read Hold	5	—	ns
TS_{RWB}	RWB to Read Set-up	10	—	ns
TH_{RWB}	RWB to Read Hold	5	—	ns
TP_{RD}	Valid Read to Valid Data Propagation Delay	—	70	ns
TZ_{RD}	Valid Read Negated to Output Tri-state	—	20	ns
TZ_{INTH}	Valid Read Negated to Output Tri-state	—	50	ns

Figure 48 Microprocessor Interface Read Access Timing (Intel Mode)

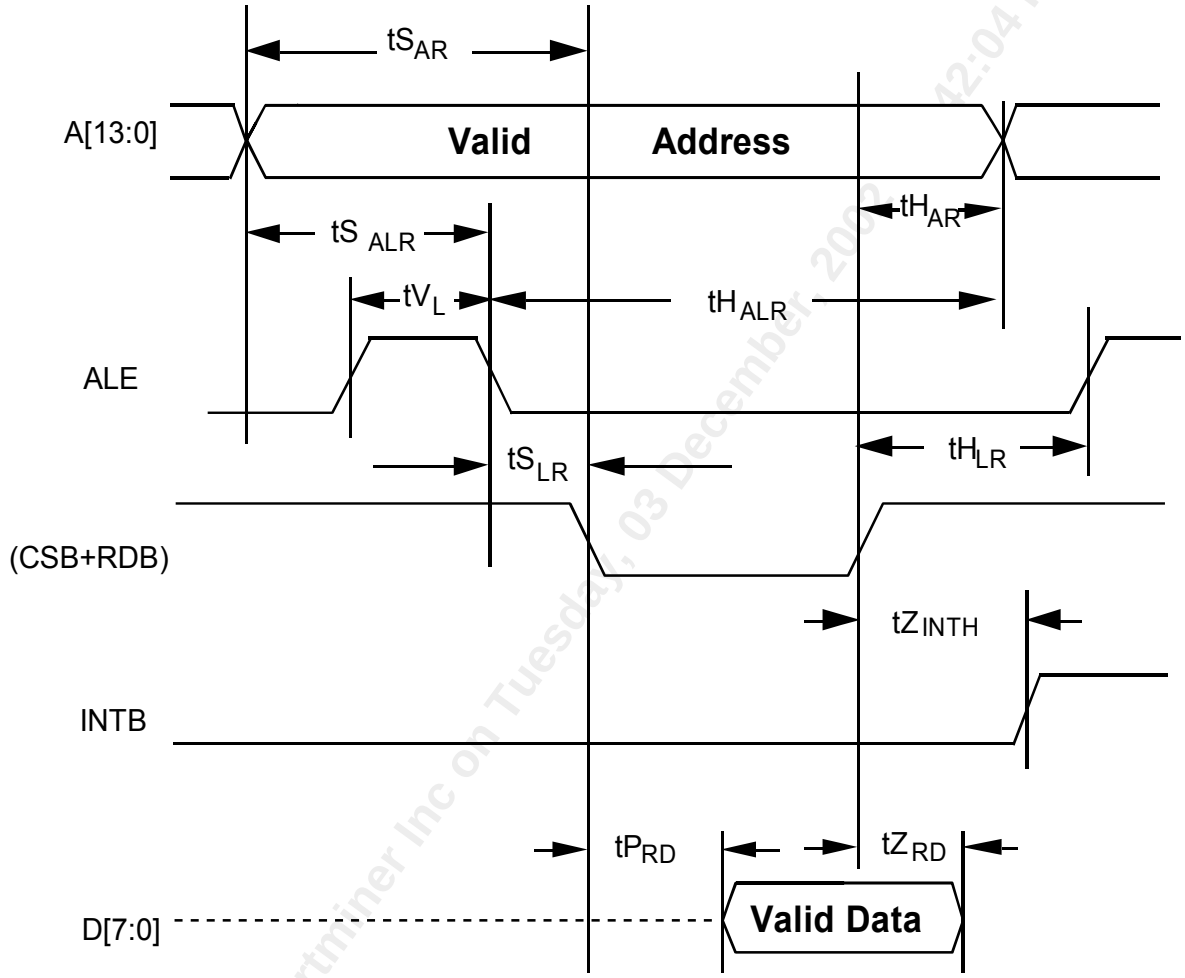
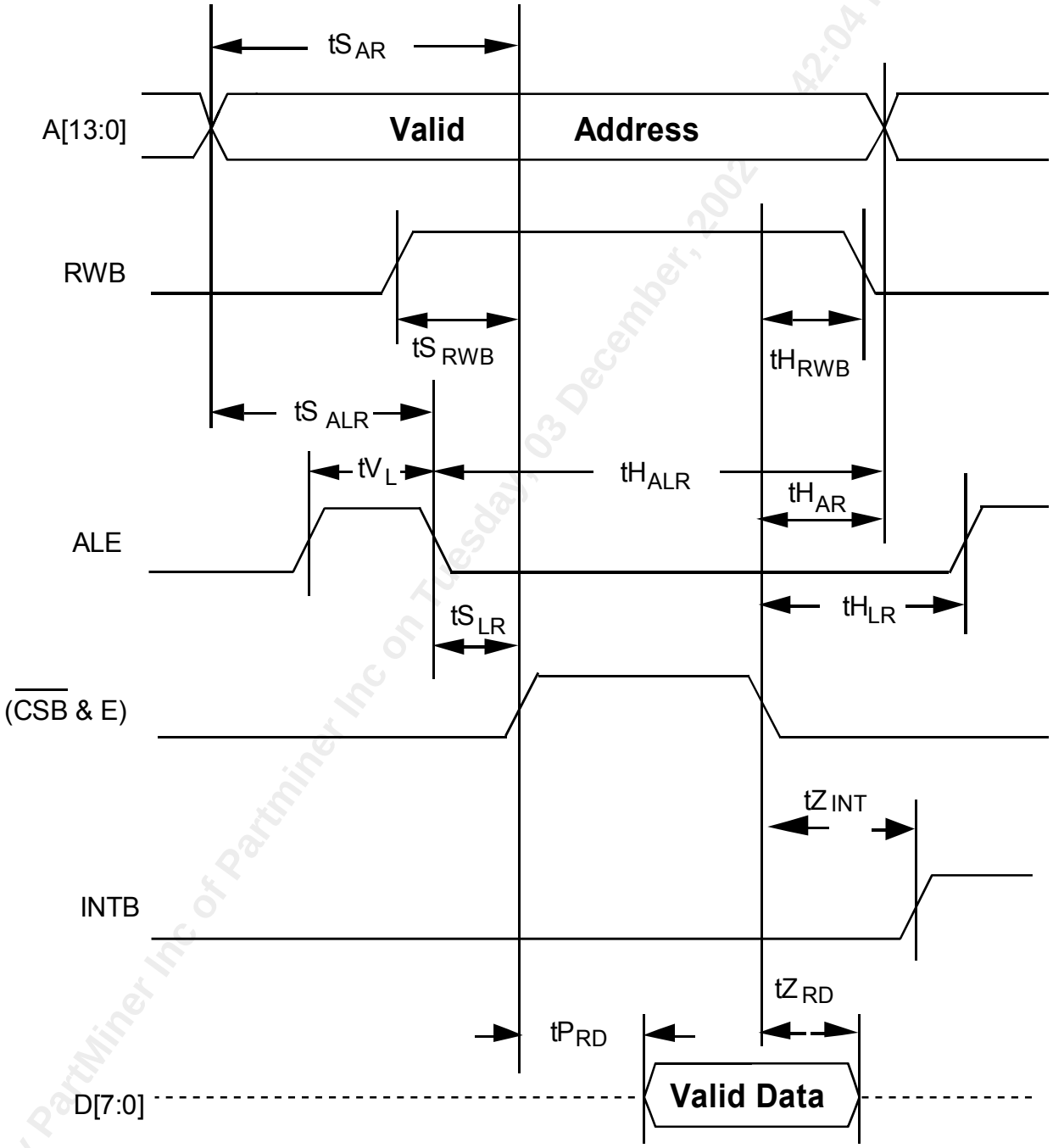


Figure 49 Microprocessor Interface Read Access Timing (Motorola Mode)



Notes

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

3. In Intel mode, a valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In Motorola mode, a valid read cycle is defined as a logical AND of the E signal, the RWB signal and the inverted CSB signal.
5. Microprocessor Interface timing applies to normal mode register accesses only.
6. In non-multiplexed Address/data bus architectures, ALE should be held high, parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR} are not applicable.
7. Parameter tH_{AR} and tS_{AR} are not applicable if Address latching is used.
8. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
9. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Table 32 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
TS_{AW}	Address to Valid Write Set-up Time	10	—	ns
TS_{DW}	Data to Valid Write Set-up Time	20	—	ns
TS_{ALW}	Address to Latch Set-up Time	10	—	ns
TH_{ALW}	Address to Latch Hold Time	10	—	ns
TV_L	Valid Latch Pulse Width	5	—	ns
TS_{LW}	Latch to Write Set-up	0	—	ns
TH_{LW}	Latch to Write Hold	5	—	ns
TS_{RWB}	RWB to Write Set-up	10	—	ns
TH_{RWB}	RWB to Write Hold	5	—	ns
TH_{DW}	Data to Valid Write Hold Time	5	—	ns
TH_{AW}	Address to Valid Write Hold Time	5	—	ns
TV_{WR}	Valid Write Pulse Width	40	—	Ns
TZ_{INTH}	Valid Write Negated to Output Tri-state	—	50	ns

Figure 50 Microprocessor Interface Write Access Timing (Intel Mode)

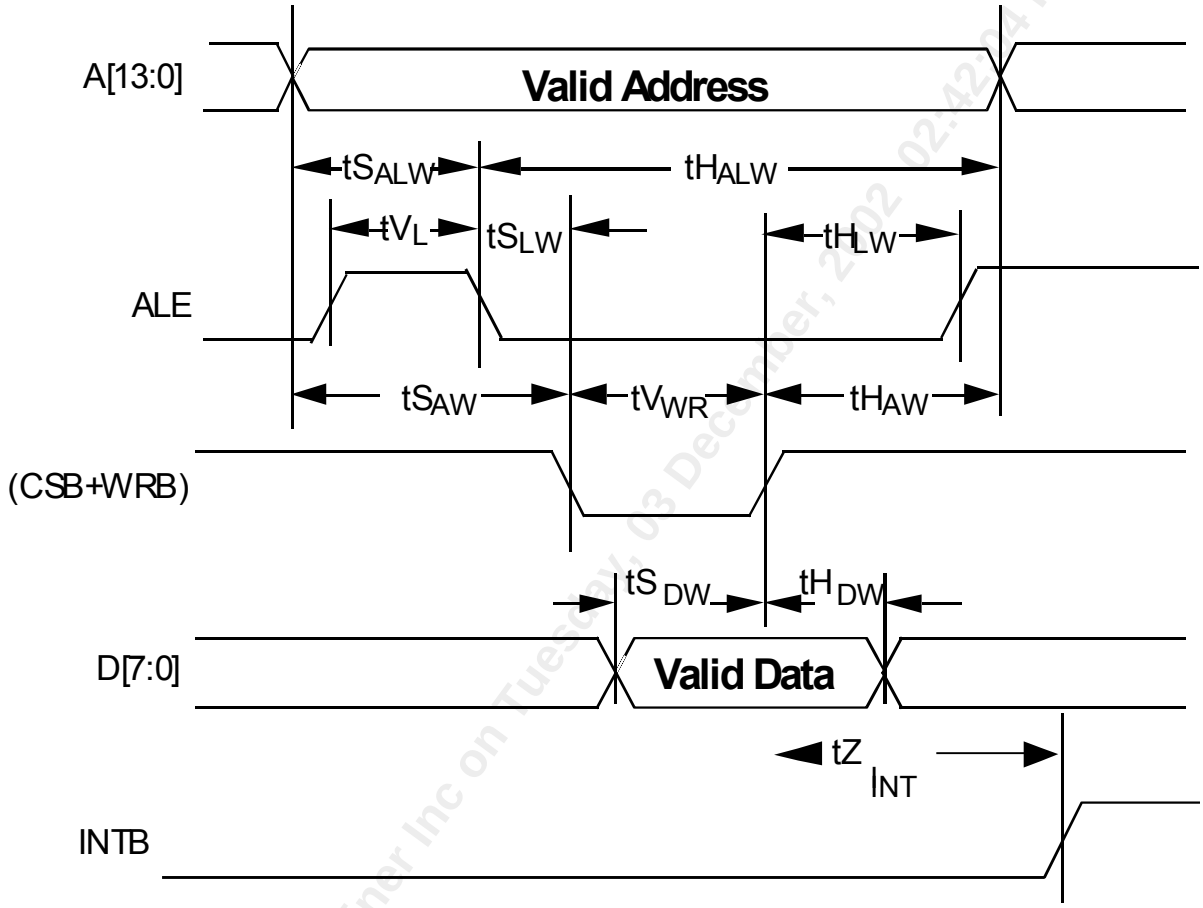
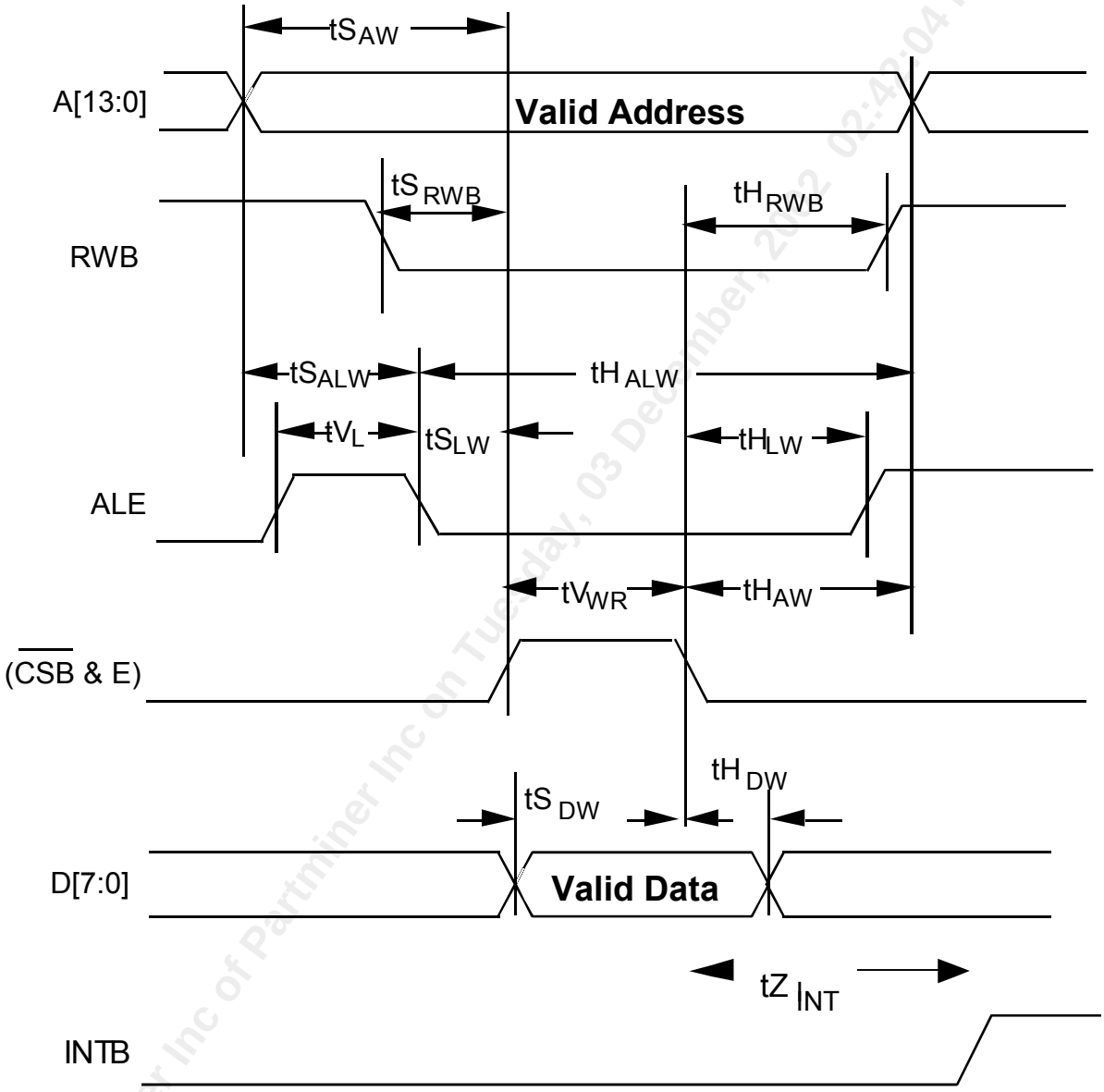


Figure 51 Microprocessor Interface Write Access Timing (Motorola Mode)



Notes

1. In Intel mode, a valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In Motorola mode, a valid write cycle is defined as a logical AND of the E signal, the inverted RWB signal and the inverted CSB signal.
3. Microprocessor timing applies to normal mode register accesses only.
4. In non-multiplexed Address/data bus architectures, ALE should be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW} are not applicable.

5. Parameters tH_{AW} and tS_{AW} are not applicable if Address latching is used.
6. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

18 A.C. Timing Characteristics

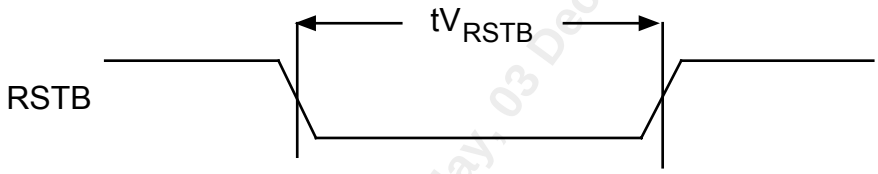
(~~T~~C-TA = -40°C to +85°C, V_{DD} = 3.3V ± 5%, V_{AVD} = 3.3V ± 5%)

18.1 System Reset Timing

Table 33 RSTB Timing

Symbol	Description	Min	Max	Units
TVRSTB	RSTB Pulse Width	100	—	ns

Figure 52 RSTB Timing Diagram



18.2 Receive Timing

Table 34 Receive Line Input Interface Timing

Symbol	Description	Min	Max	Units
	REFCLK Nominal Frequency	19.44	19.44	MHz
	REFCLK Duty Cycle	30	70	%
	REFCLK Frequency Tolerance†	-20	+20	ppm

Note

1. The specification may be relaxed to +/- 50 ppm for LAN applications that do not require this timing accuracy. The specified tolerance is required to meet the SONET/SDH free run accuracy specification.

Table 35 Receive Line Overhead and Alarm Output Timing

Symbol	Description	Min	Max	Units
	RCLK1-4 Duty Cycle (RCLK is nominally 19.44 MHz. RCLK is a divide by eight of the receive line clock.)	40	60	%

Symbol	Description	Min	Max	Units
	PGMRCLK Duty Cycle (PGMRCLK is nominally 19.44 MHz when the RCLKSEL bit in the SPECTRA 4x155 Clock Control register is set low. PGMRCLK is a divide by eight of the receive line clock.) (PGMRCLK is nominally 8 KHz when the RCLKSEL bit is set high. PGMRCLK is a divide by TDB of the receive line clock.)	40	60	%
t_{PRCLK}	RCLK1-4 High to SALM1-4, LOF1-4, LOS1-4, LAIS1-4, and LRDI1-4 Valid Prop Delay	1	10	ns
	RSLDCLK1-4 Duty Cycle (RSLDCLK is nominally 192 MHz or 576 MHz clock when outputting Section or Line DCC respectively.)	40	60	%
t_{PRSLD}	RSLDCLK1-4 Low to RSLD1-4 Valid Prop Delay	-20	20	ns
	RTOHCLK1-4 Duty Cycle (RTOHCLK is nominally a 5.184 MHz clock)	30	70	%
t_{PRTOH}	RTOHCLK1-4 Low to RTOH1-4 and RTOHFP1-4 Valid Prop Delay	-5	10	ns

Figure 53 Receive Line Output Timing

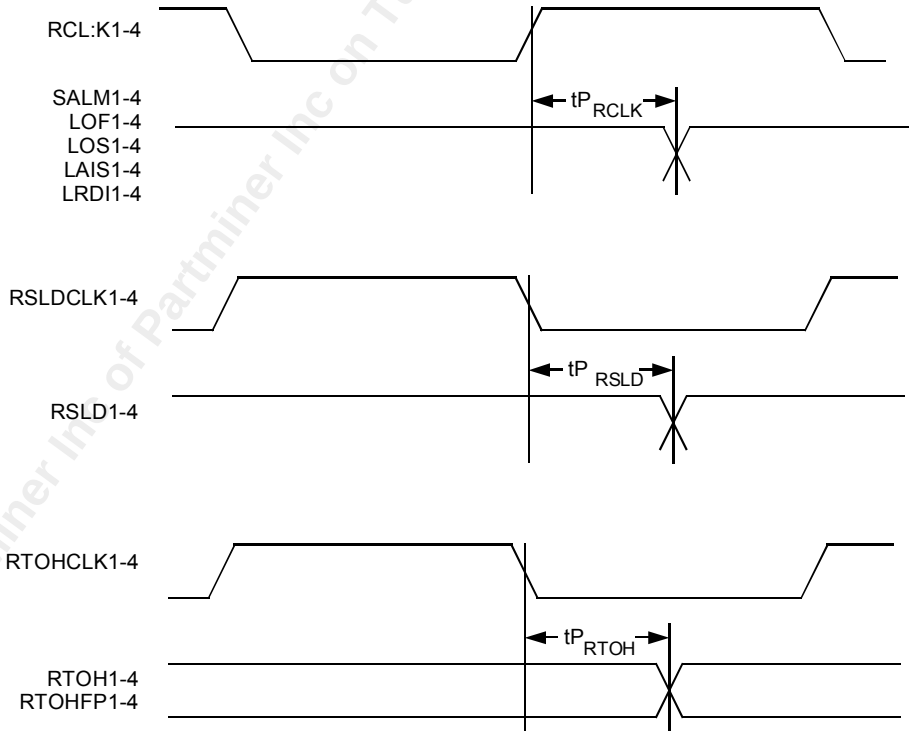


Table 36 Receive Path Overhead and Alarm Port Output Timing

Symbol	Parameter	Min	Max	Units
	RPOHCLK1-4 Duty Cycle (RPOHCLK is nominally 12.96 MHz)	40	60	%
tPRPOHFP	RPOHCLK Low to RPOHFP Valid	-5	15	ns
tPRPOH	RPOHCLK Low to RPOH Valid	-5	15	ns
tPRPOHEN	RPOHCLK Low to RPOHEN Valid	-5	15	ns
tPB3E	RPOHCLK Low to B3E Valid	-5	15	ns
tPRAD	RPOHCLK Low to RAD Valid	-5	15	ns
tPRALM	RPOHCLK Low to RALM Valid	-5	15	ns

Figure 54 Receive Path Overhead and Alarm Port Output Timing

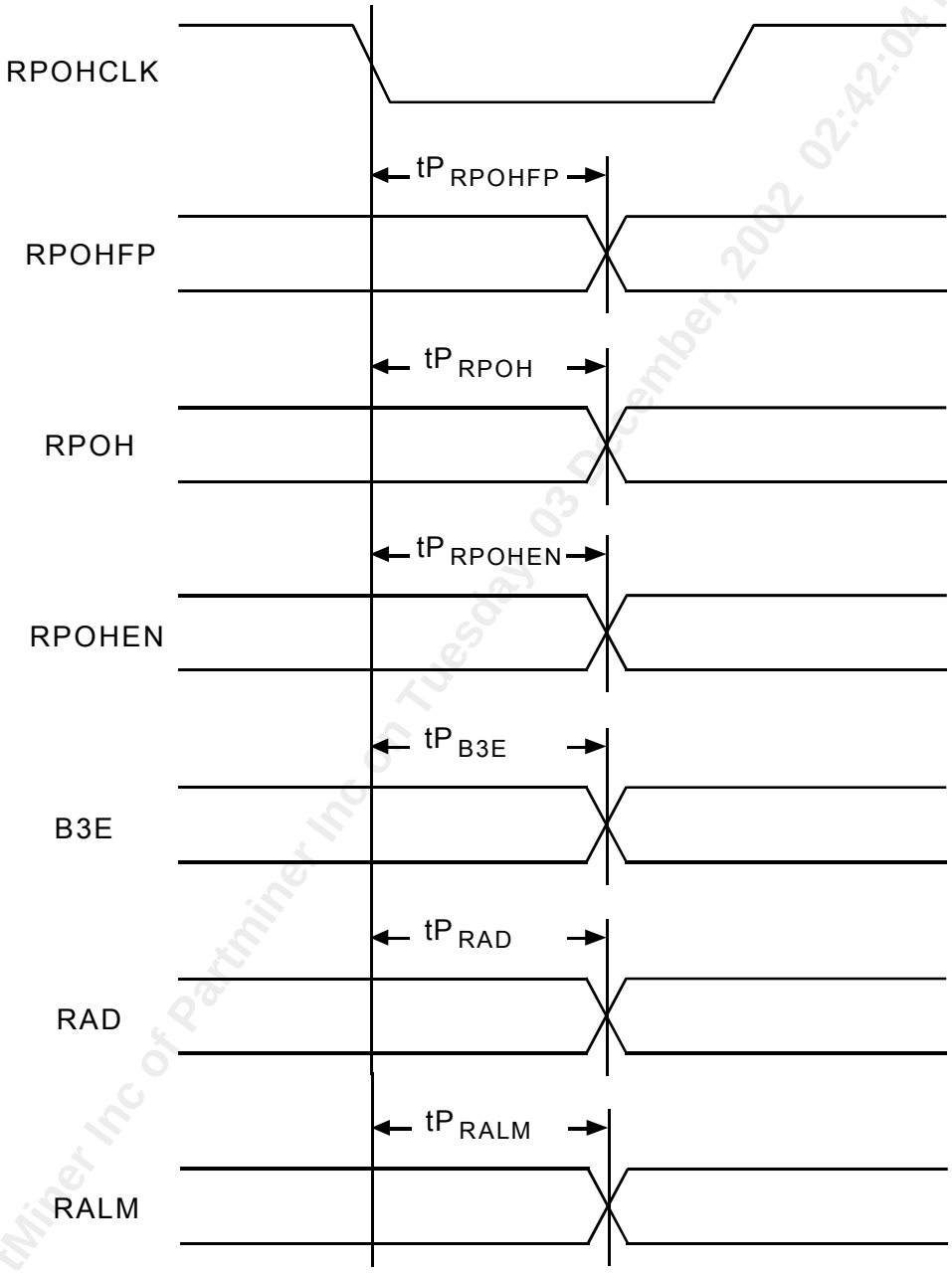


Table 37 Receive Ring Control Port Output Timing

Symbol	Description	Min	Max	Units
	RRCPCLK1-4 Duty Cycle (RRCPCLK1-4 is nominally a 3.24 MHz clock)	40	60	%
tP_{RRCPFP}	RRCPCLK1-4 Low to RRCPFP1-4 Valid Prop Delay	-10	10	ns

Symbol	Description	Min	Max	Units
tP_{RRCPD}	RRCPCLK1-4 Low to RRCPDAT1-4 Valid Prop Delay	-10	10	ns

Figure 55 Ring Control Port Output Timing

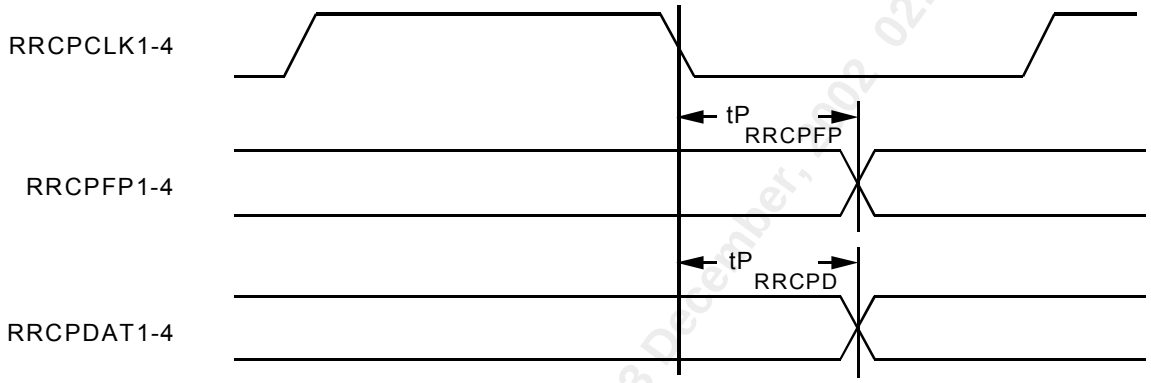
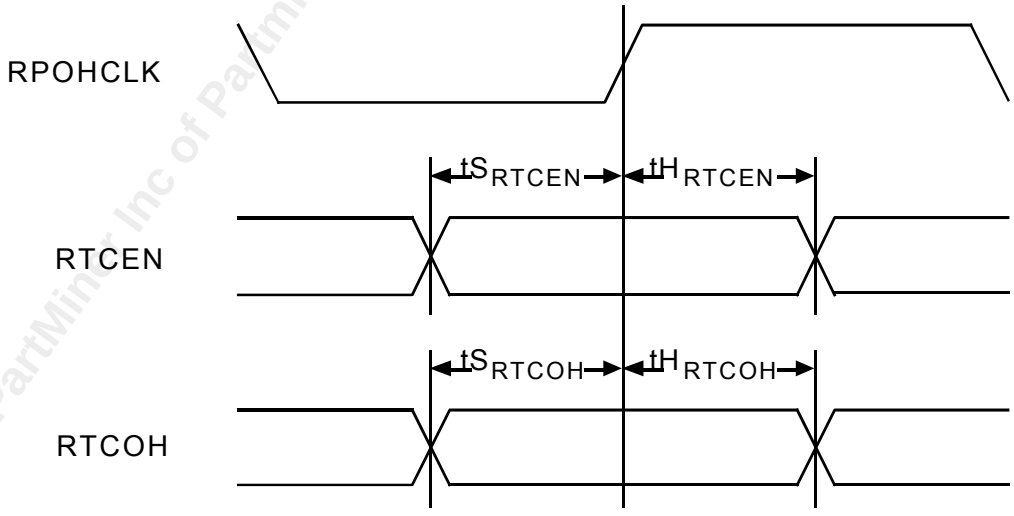


Table 38 Receive Tandem Connection Input Timing

Symbol	Parameter	Min	Max	Units
tSRTCEN	RTCEN Set-up Time	15	—	ns
tHRTCEN	RTCEN Hold Time	15	—	ns
tSRTCOH	RTCOH Set-up Time	15	—	ns
tHRTCOH	RTCOH Hold Time	15	—	ns

Figure 56 Receive Tandem Connection Input Timing.



18.3 Telecom Drop Bus Timing

Table 39 Telecom Drop Bus Input Timing

Symbol	Parameter	Min	Max	Units
	DCK Freq. (Nominally 19.44MHz)	—	20	MHz
	DCK Freq. (Nominally 77.76 MHz)	60	80	MHz
	DCK Duty Cycle	40	60	%
tS_{DFP}	DFP Set-up Time	3	—	ns
tH_{DFP}	DFP Hold Time	0	—	ns

Figure 57 Telecom Drop Bus Input Timing

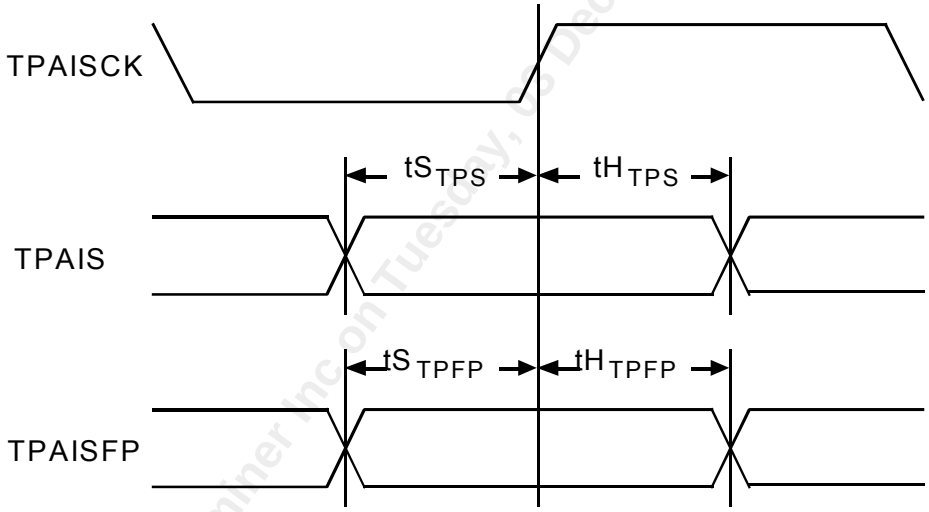


Table 40 Telecom Drop Bus Output Timing at 77.76 MHz DCK

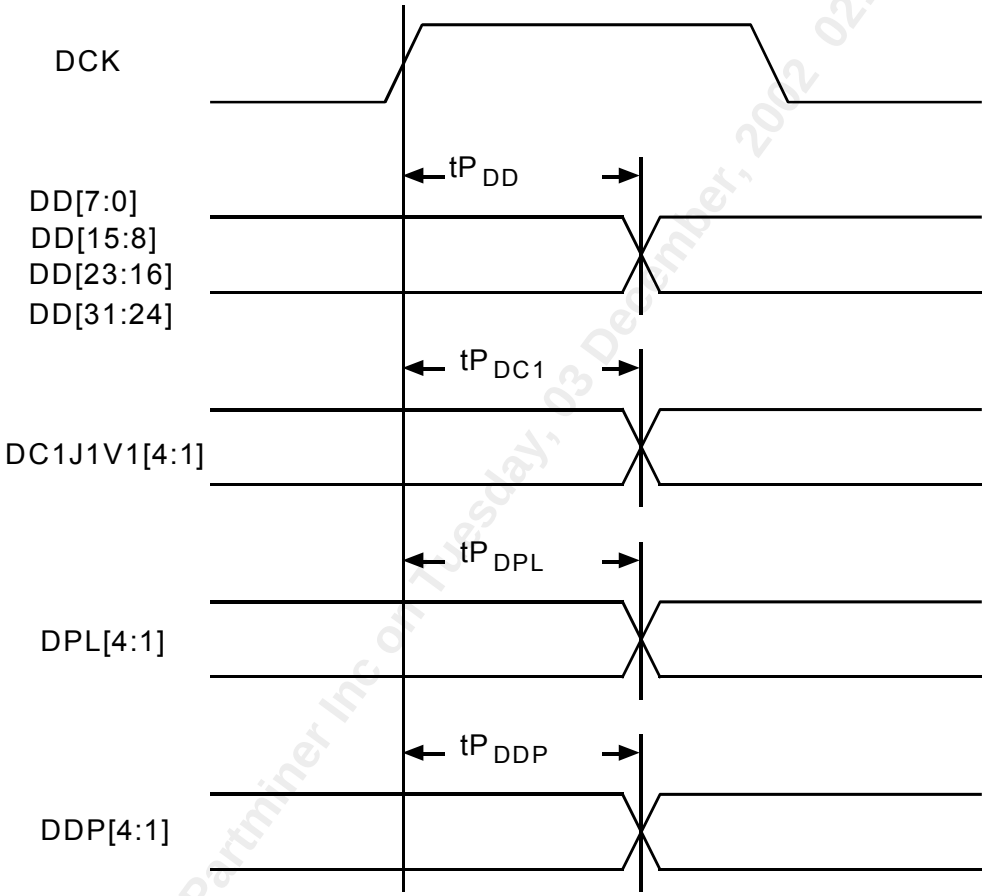
Symbol	Parameter	Min	Max	Units
tP_{DD}	DCK High to DD[7:0], DD[15:8], DD[23:16], DD[31:24] Valid	1	7	ns
tP_{DC1}	DCK High to DC1J1V1[4:1] Valid	1	7	ns
tP_{DPL}	DCK High to DPL[4:1] Valid	1	7	ns
tP_{DDP}	DCK High to DDP[4:1] Valid	1	7	ns

Table 41 Telecom Drop Bus Output Timing at 19.44 MHz DCK

Symbol	Parameter	Min	Max	Units
tP_{DD}	DCK High to DD[7:0], DD[15:8], DD[23:16], DD[31:24] Valid	4	14	ns
tP_{DC1}	DCK High to DC1J1V1[4:1] Valid	4	14	ns
tP_{DPL}	DCK High to DPL[4:1] Valid	4	14	ns

Symbol	Parameter	Min	Max	Units
tP_{DDP}	DCK High to DDP[4:1] Valid	4	14	ns

Figure 58 Telecom Drop Bus Output Timing



18.4 System-side Path Alarm Input Timing

Table 42 System DROP-side Path Alarm Input Timing

Symbol	Parameter	Min	Max	Units
	DPAISCK Freq.	—	20	MHz
	DPAISCK Duty Cycle	40	60	
tS_{DPS}	DPAIS Set-up Time	10	—	ns
tH_{DPS}	DPAIS Hold Time	10	—	ns
tS_{DPFP}	DPAISFP Set-up Time	10	—	ns
tH_{DPFP}	DPAISFP Hold Time	10	—	ns

Figure 59 System DROP-side Path Alarm Input Timing

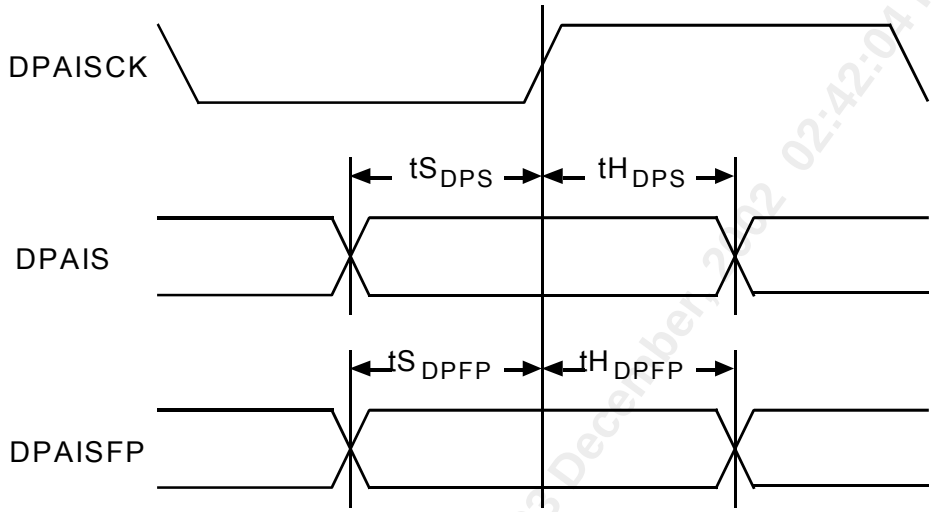
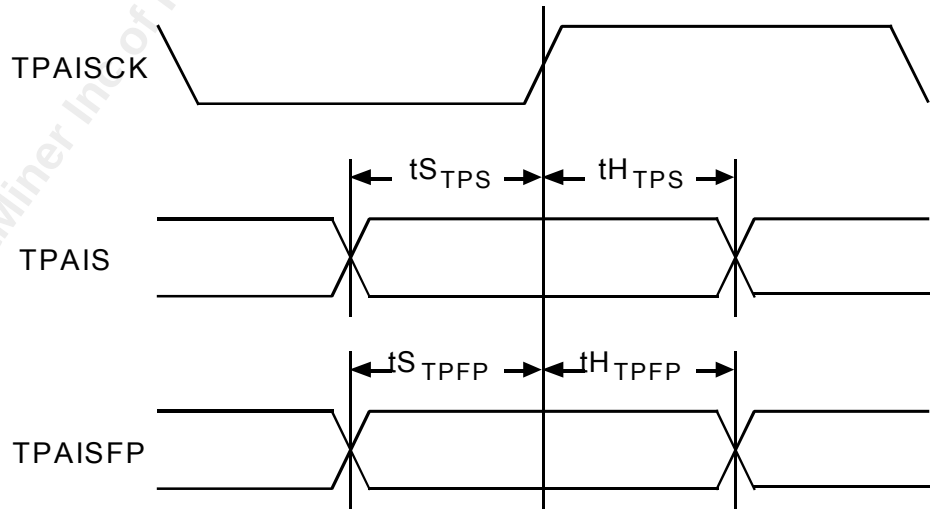


Table 43 System ADD-side Path Alarm Input Timing

Symbol	Parameter	Min	Max	Units
	TPAISCK Freq.	—	20	MHz
	TPAISCK Duty Cycle	40	60	
tS_{TPS}	TPAIS Set-up Time	10	—	ns
tH_{TPS}	TPAIS Hold Time	10	—	ns
tS_{TPFP}	TPAISFP Set-up Time	10	—	ns
tH_{TPFP}	TPAISFP Hold Time	10	—	ns

Figure 60 System ADD-side Path Alarm Input Timing

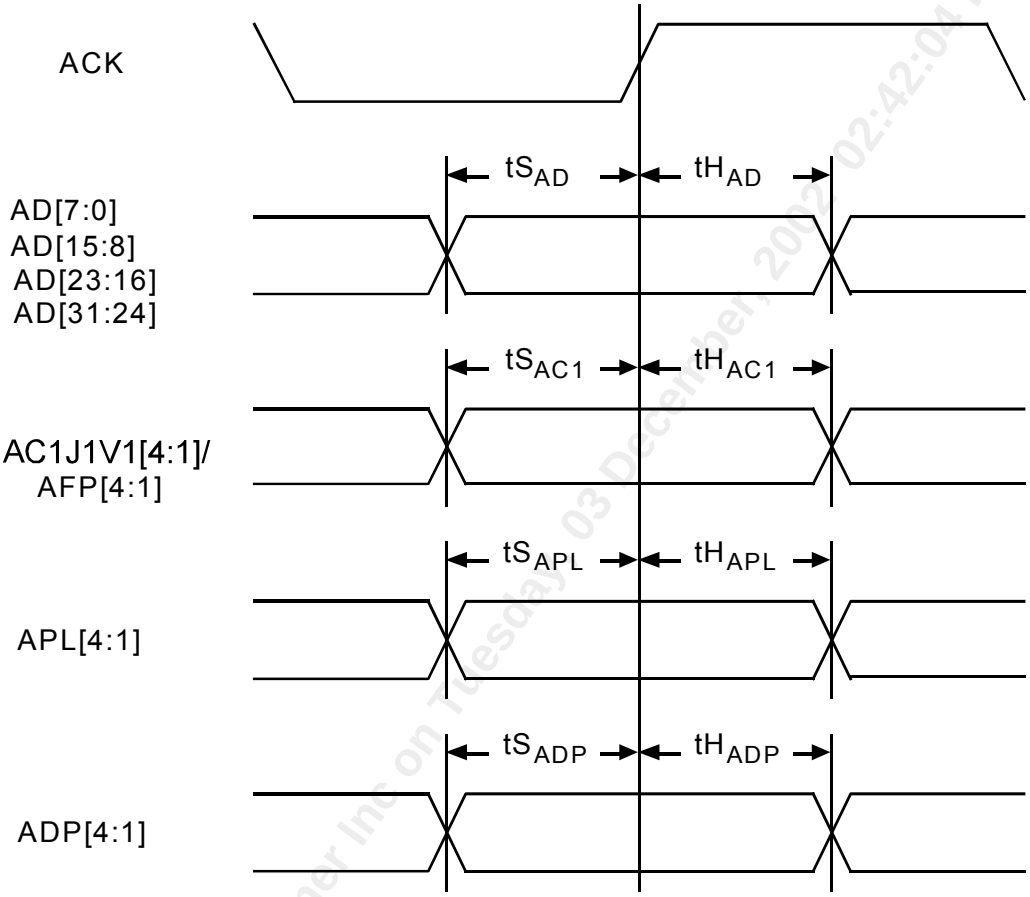


18.5 Telecom Add Bus Timing

Table 44 Telecom Add Bus Input Timing

Symbol	Parameter	Min	Max	Units
	ACK Freq. STS-3 (STM-1) Byte Telecom Bus Nominally 19.44 MHz	—	20	MHz
	ACK Freq. STS-12 (STM-4) Byte Telecom Bus Nominally 77.76 MHz	—	80	MHz
	ACK Duty Cycle	40	60	%
tS_{AD}	AD[7:0], AD[15:8], AD[23:16], AD[31:24] Set-up Time	3	—	ns
tH_{AD}	AD[7:0], AD[15:8], AD[23:16], AD[31:24] Hold Time	0	—	ns
tS_{AC1}	AC1J1V1[4:1]/AFP[4:1] Set-up Time	3	—	ns
tH_{AC1}	AC1J1V1[4:1]/AFP[4:1] Hold Time	0	—	ns
tS_{APL}	APL[4:1] Set-up Time	3	—	ns
tH_{APL}	APL[4:1] Hold Time	0	—	ns
tS_{ADP}	ADP[4:1] Set-up Time	3	—	ns
tH_{ADP}	ADP[4:1] Hold Time	0	—	ns

Figure 61 Telecom Add Bus Input Timing



18.6 Transmit Timing

Table 45 Transmit Alarm Port Input Timing

Symbol	Parameter	Min	Max	Units
	TACK Frequency	5	15	MHz
	TACK Duty Cycle	40	60	%
t_{STAD}	TAD Set-up Time	10	—	ns
t_{HTAD}	TAD Hold Time	10	—	ns
t_{STAFP}	TAFP Set-up Time	10	—	ns
t_{HTAFP}	TAFP Hold Time	10	—	ns

Figure 62 Transmit Alarm Port Input Timing

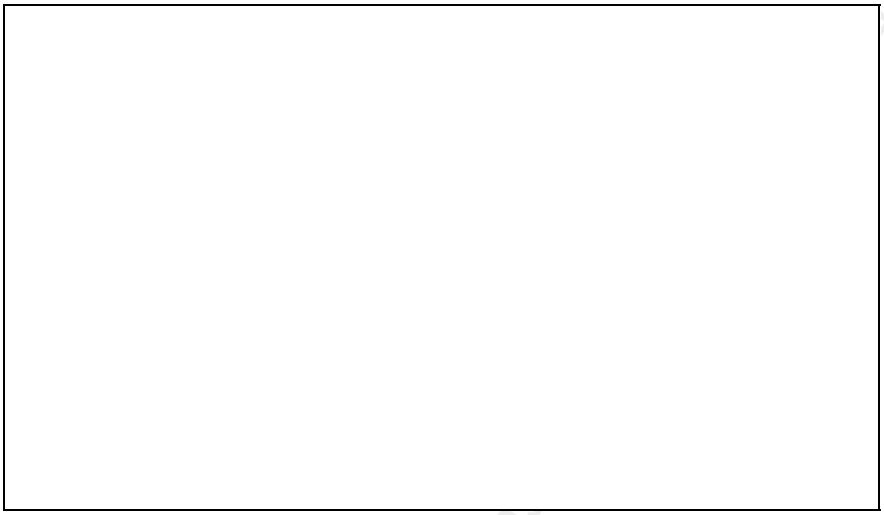


Table 46 Transmit Transport Overhead Input Timing

Symbol	Description	Min	Max	Units
tSTSLD	TSLD Set-up Time to TSLDCLK	20	—	ns
tHTSLD	TSLD Hold Time to TSLDCLK	0	—	ns
tSTTOH	TTOH, TTOHEN Set-up Time to TTOHCLK	20	—	ns
tHTTOH	TTOH, TTOHEN Hold Time to TTOHCLK	0	—	ns

Figure 63 Transmit Transport Overhead Input Timing

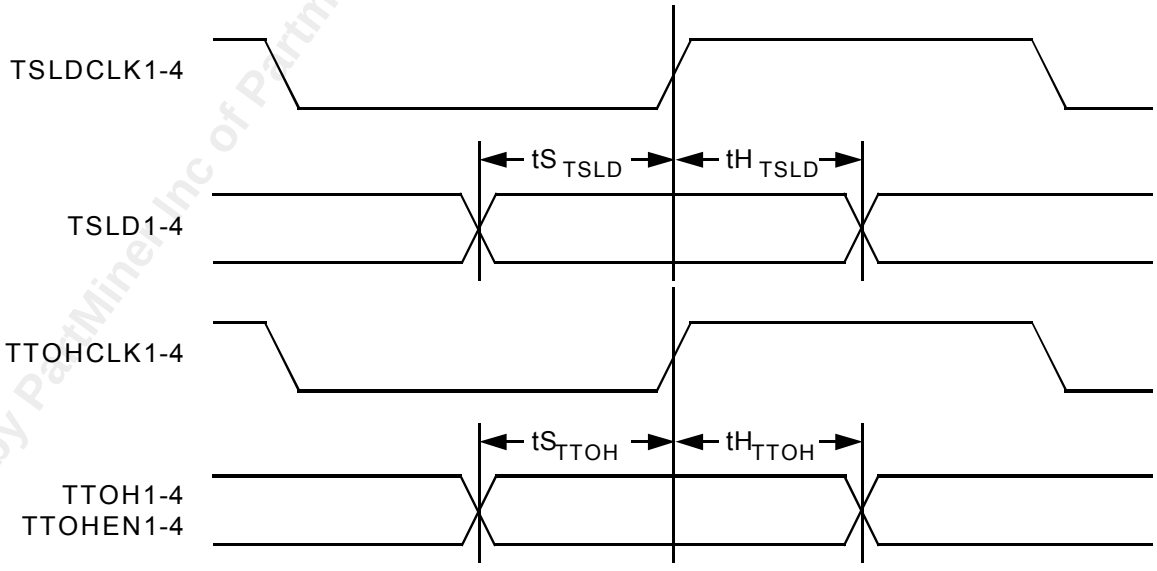


Table 47 Transmit Ring Control Port Input Timing

Symbol	Description	Min	Max	Units
	TRCPCLK1-4 Frequency (nominally 3.24 MHz)	—	3.4	MHz
	TRCPCLK1-4 Duty Cycle	33	67	%
$t_{STRCPFP}$	TRCPFP1-4 Set-up Time to TRCPCLK	10	—	ns
$t_{HTRCPFP}$	TRCPFP1-4 Hold Time to TRCPCLK	10	—	ns
t_{STRCPD}	TRCPDAT1-4 Set-up Time to TRCPCLK	10	—	ns
t_{HTRCPD}	TRCPDAT1-4 Hold Time to TRCPCLK	10	—	ns

Figure 64 Transmit Ring Control Port Input Timing

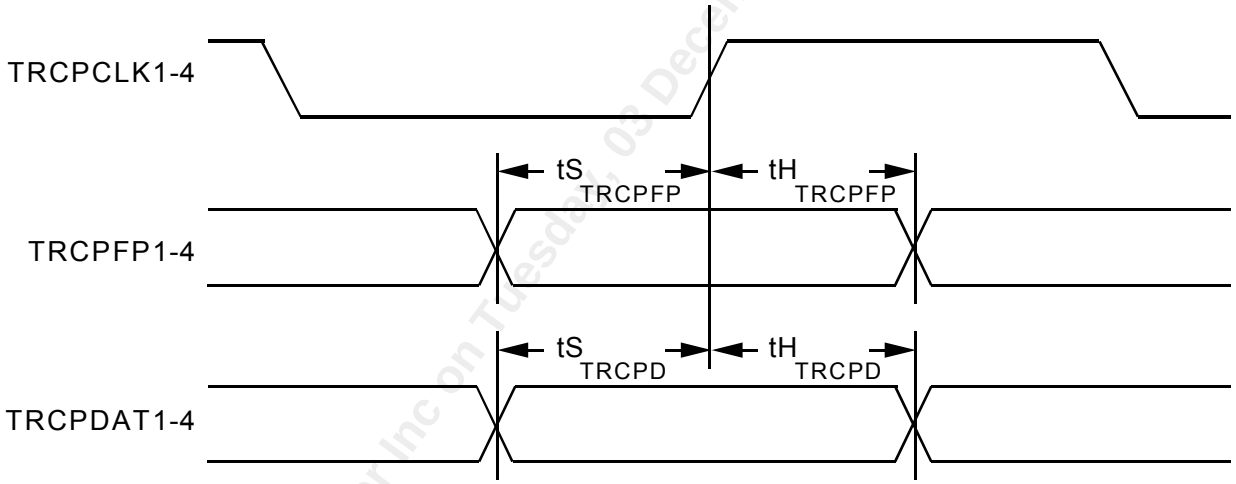


Table 48 Transmit Overhead Output Timing

Symbol	Description	Min	Max	Units
	TSLDCLK1-4 Duty Cycle (TSLDCLK is nominally 192 MHz or 576 MHz clock when inputting Section or Line DCC respectively.)	40	60	%
	TTOHCLK1-4 Duty Cycle (TTOHCLK is nominally a 5.184 MHz clock)	30	70	%
$t_{PTTOHFP}$	TTOHCLK1-4 Low to TTOHFP1-4 Valid Prop Delay	-5	10	ns

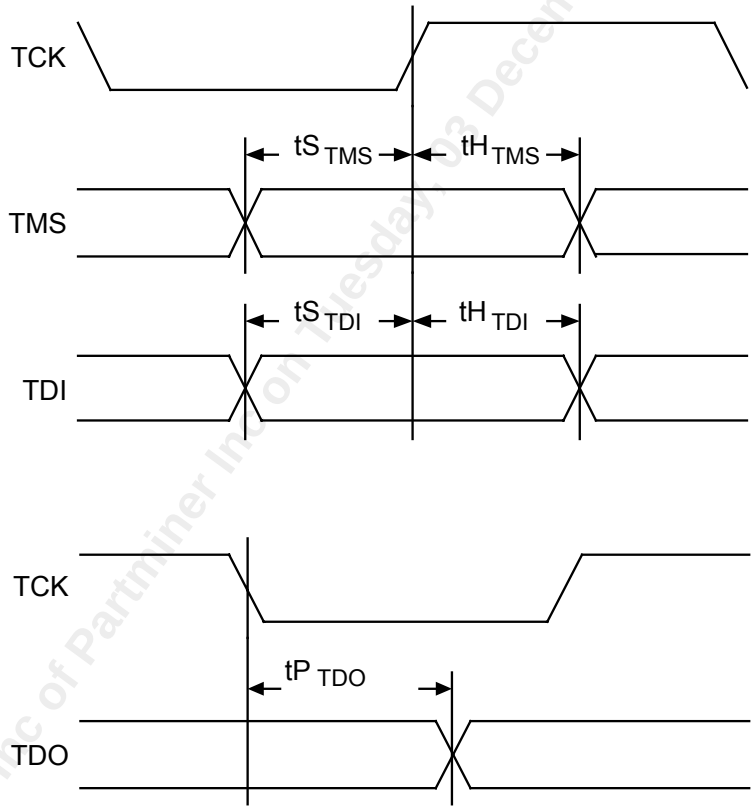
18.7 JTAG Timing

Table 49 JTAG Port Interface

Symbol	Description	Min	Max	Units
	TCK Frequency	—	4	MHz
	TCK Duty Cycle	40	60	%

Symbol	Description	Min	Max	Units
$t_{S}TMS$	TMS Set-up time to TCK	50	—	ns
$t_{H}TMS$	TMS Hold time to TCK	50	—	ns
$t_{S}TDI$	TDI Set-up time to TCK	50	—	ns
$t_{H}TDI$	TDI Hold time to TCK	50	—	ns
$t_{P}TDO$	TCK Low to TDO Valid	2	50	ns
tVTRSTB	TRSTB Pulse Width	100	—	ns

Figure 65 JTAG Port Interface Timing



Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. ~~Maximum o~~Output propagation delays are measured with a 50 pF load on the outputs except where indicated.

19 Ordering and Thermal Information

Table 50 Ordering information

Part Number	Description
PM5316-BI	520 Super Ball Grid Array (SBGA)

Table 51 Thermal information – Theta Jc

Part Number	Ambient Temperature	Theta Jc
PM5316-BI	-40°C to 85°C	1 °C/W

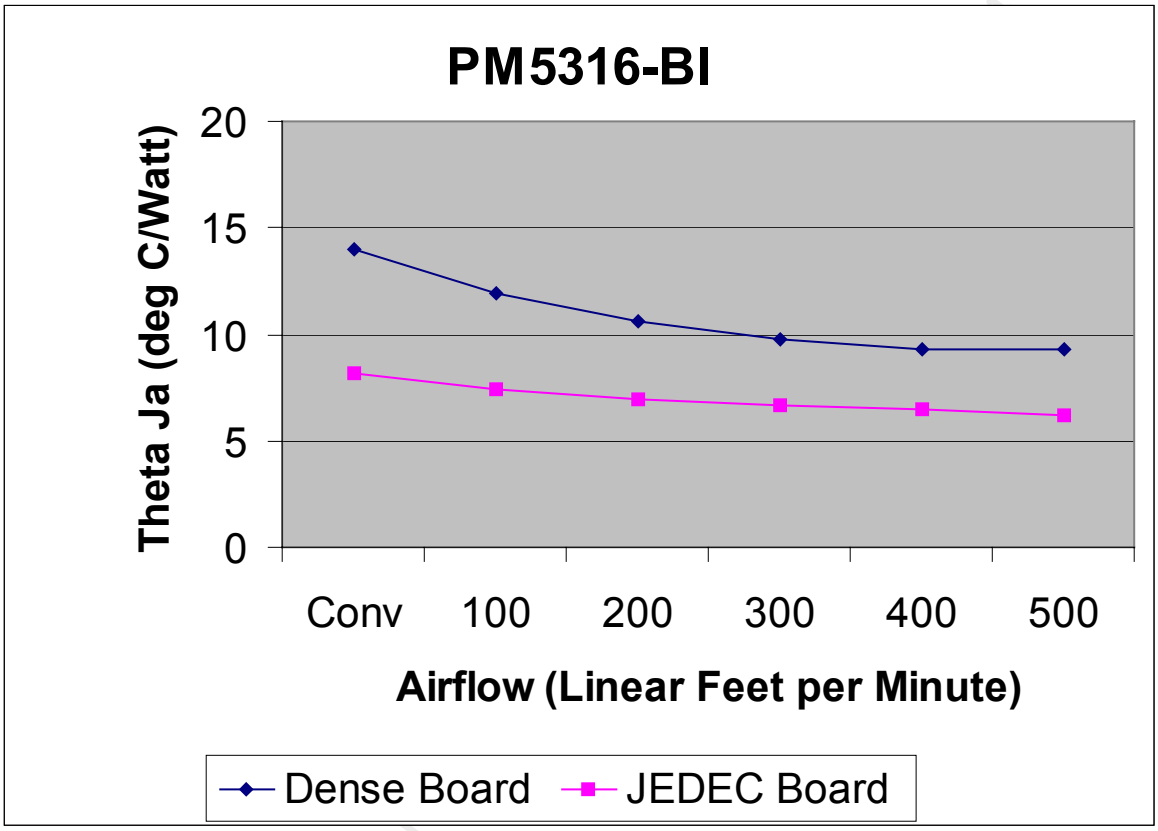
Table 52 Maximum Junction Temperature

PM5316-BI	Maximum Junction Temperature for Long Term Reliability	105 °C

Table 53 Thermal information – Theta Ja vs. Airflow

		Forced Air (Linear Feet per Minute)				
Theta JA @ specified power	**Convection**	**100**	**200**	**300**	**400**	**500**
Dense Board	14.0	12.0	10.6	9.7	9.3	9.3
JEDEC Board	8.2	7.4	6.9	6.6	6.4	6.2

Figure 66 Theta Ja vs. Airflow Plot

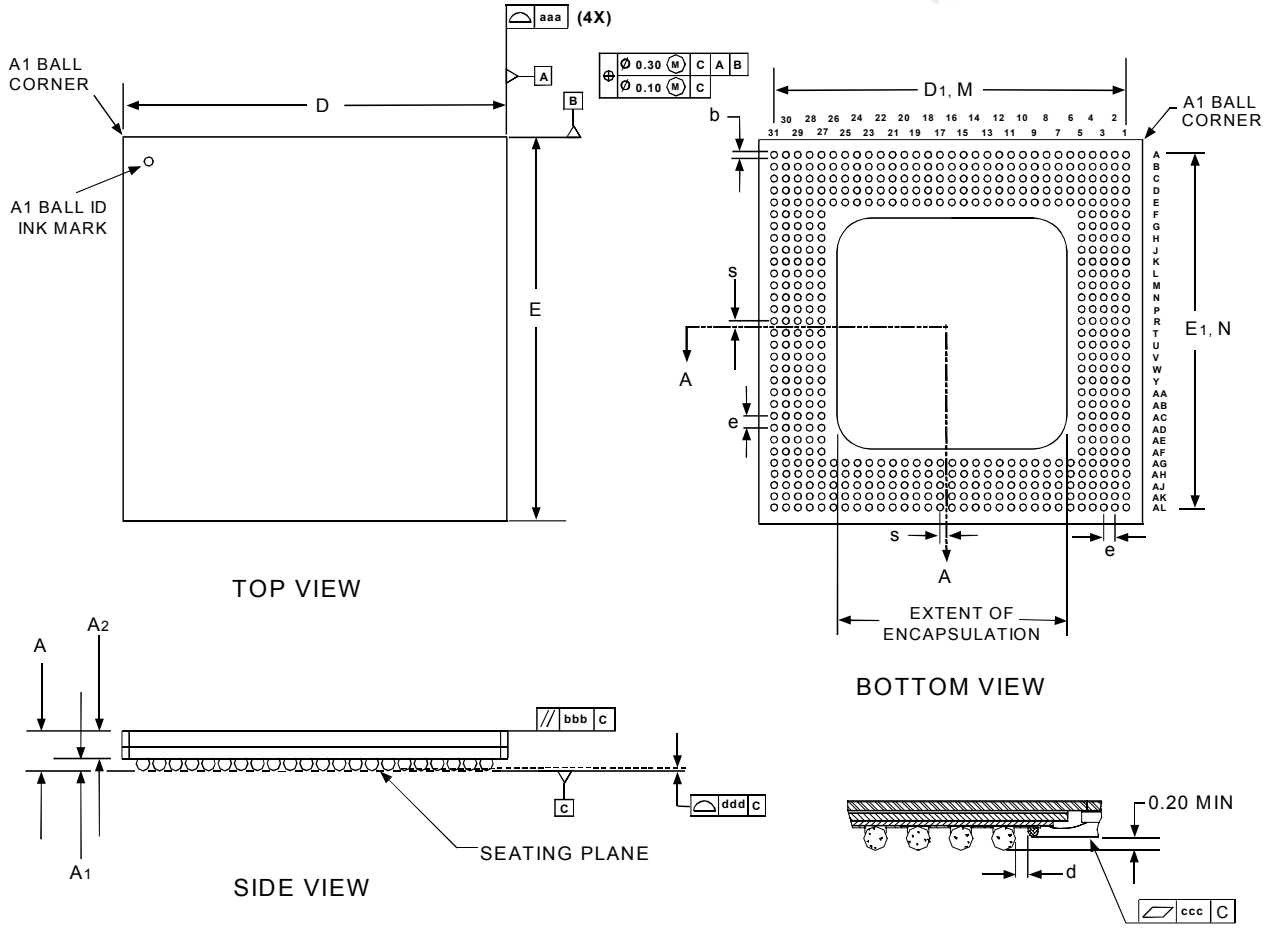


Notes

1. Dense Board – Board with 3x3 array of the same device with spacing of 4mm between devices. 6 layer board (3 signal layers, 3 power layers). Chart represents device in the center of the array. Chart represents values obtained through simulation.
2. JEDEC Board – Single component on a board. 4 layer board (2 signal layers, 2 power layers), metallization length x width = 94 mm x 94 mm. Board dimension = 114mmx142mm. JEDEC Measurement as per EIA/GESD51-1.

20 Mechanical Information

Figure 67 Mechanical Drawing 520 Pin Super Ball Grid Array (SBGA)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ccc DENOTES FLATNESS.
5) DIMENSION ddd DENOTES COPLANARITY.

PACKAGE TYPE : 520 THERMALLY ENHANCED BALL GRID ARRAY - SBGA																
BODY SIZE : 40 x 40 x 1.54 MM																
Dim.	A	A1	A2	D	D1	E	E1	M,N	b	d	e	aaa	bbb	ccc	ddd	S
Min.	1.30	0.50	0.80	39.90	38.00	39.90	38.00		0.60	0.5	-	-	-	-		-
Nom.	1.51	0.60	0.91	40.00	38.10	40.00	38.10	31x31	0.75	-	1.27	-	-	-		0.00
Max.	1.70	0.70	1.00	40.10	38.20	40.10	38.20		0.90	-	-	0.20	0.25	0.20	0.20	-

Notes