

MC74VHC1GT02

Advance Information 2-Input NOR Gate / CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74VHC1GT02 is a single gate 2-input NOR fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0V CMOS logic to 5.0V CMOS Logic or from 1.8V CMOS logic to 3.0V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT02 input structure provides protection when voltages up to 7V are applied, regardless of the supply voltage. This allows the MC74VHC1GT02 to be used to interface 5V circuits to 3V circuits. The output structures also provide protection when $V_{CC} = 0V$. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: $t_{PD} = 4.7ns$ (Typ) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 2\mu A$ (Max) at $T_A = 25^\circ C$
- TTL-Compatible Inputs: $V_{IL} = 0.8V$; $V_{IH} = 2.0V$
- CMOS-Compatible Outputs: $V_{OH} > 0.8V_{CC}$; $V_{OL} < 0.1V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; MM > 200V, CDM > 1500V
- Chip Complexity: 6 FETs or 2 Equivalent Gates

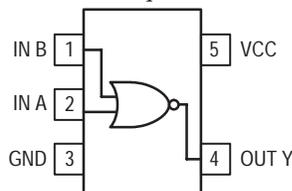
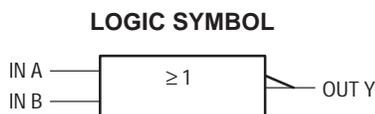


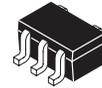
Figure 1. 5-Lead SOT-353 Pinout (Top View)



This document contains information on a new product. Specifications and information herein are subject to change without notice.

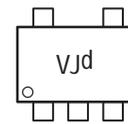


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SC-88A / SOT-353
DF SUFFIX
CASE 419A

MARKING DIAGRAM



Pin 1
d = Date Code

PIN ASSIGNMENT

Pin	Assignment
1	IN B
2	IN A
3	GND
4	OUT Y
5	VCC

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

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MAXIMUM RATINGS*

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN}	-0.5 to +7.0	V
DC Output Voltage $V_{CC} = 0$ High or Low State	V_{OUT}	-0.5 to 7.0 -0.5 to $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current ($V_{OUT} < GND$; $V_{OUT} > V_{CC}$)	I_{OK}	+20	mA
DC Output Current, per Pin	I_{OUT}	+25	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+50	mA
Power dissipation in still air, SC-88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	-65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — SC-88A Package: -5 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{IN}	0.0	5.5	V
DC Output Voltage $V_{CC} = 0$ High or Low State	V_{OUT}	0.0 0.0	5.5 V_{CC}	V
Operating Temperature Range	T_A	-55	+85	°C
Input Rise and Fall Time $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	t_r, t_f	0 0	100 20	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0	V	
V _{IL}	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4	V	
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4mA I _{OH} = -8mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66	V	
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5				0.36 0.36		0.44 0.44		0.52 0.52
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			2.0		20		40	μA
I _{CC(T)}	Quiescent Supply Current	Per Input: V _{IN} = 3.4V Other Input: V _{CC} or GND	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Y	V _{CC} = 3.0 ± 0.3V C _L = 15 pF C _L = 50 pF		7.0 9.5	10.0 13.5		11.0 15.0		13.0 17.5	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15 pF C _L = 50 pF		4.7 5.5	6.7 7.7		7.5 8.5		8.5 9.5	
C _{IN}	Maximum Input Capacitance			5	10		10		10	pF

C _{PD}	Power Dissipation Capacitance (Note NO TAG)	Typical @ 25°C, V _{CC} = 5.0V		pF
		21		

- C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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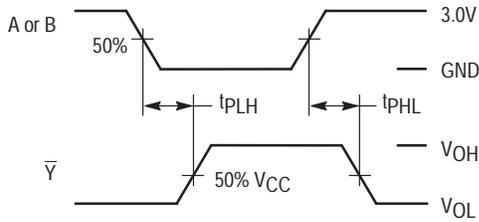
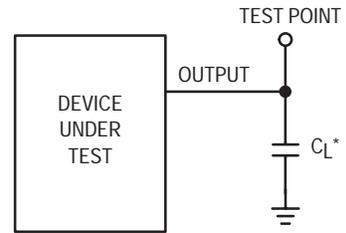


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

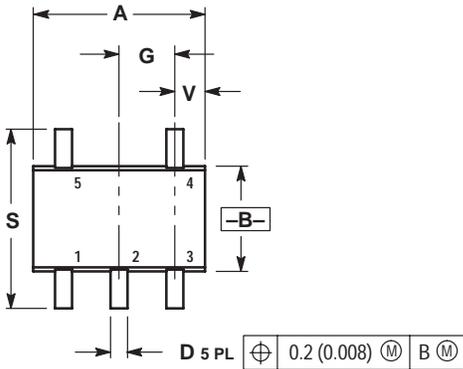
Figure 3. Test Circuit

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size
	Circuit Indicator	Temp Range Identifier	Tech-nology	Input Type	Device Function	Package Suffix	Tape & Reel Suffix		
MC74VHC1GT02DFT1	MC	74	VHC1G	T	02	DF	T1	SC-88A/ SOT-353	7-Inch/3000 Unit

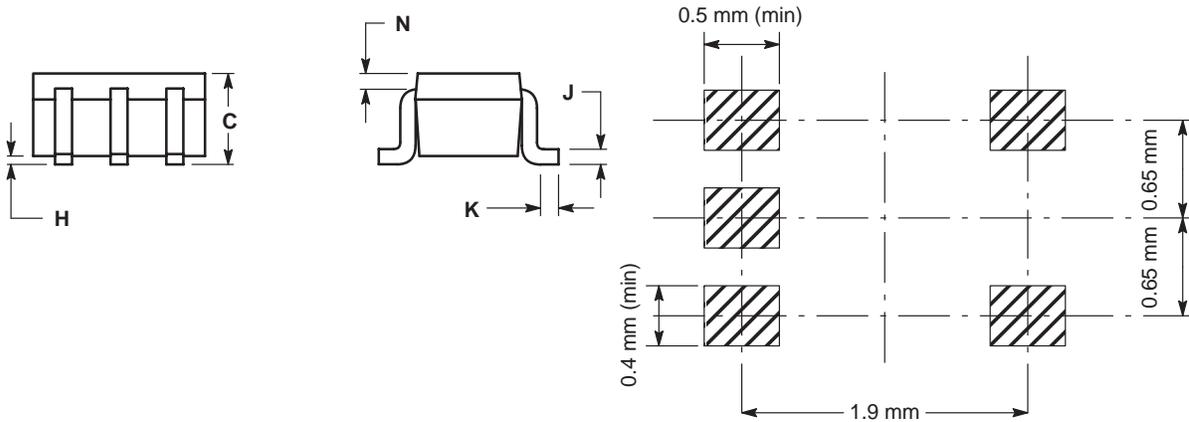
PACKAGE DIMENSIONS

SC-88A / SOT-353
DF SUFFIX
5-LEAD PACKAGE
CASE 419A-01
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40



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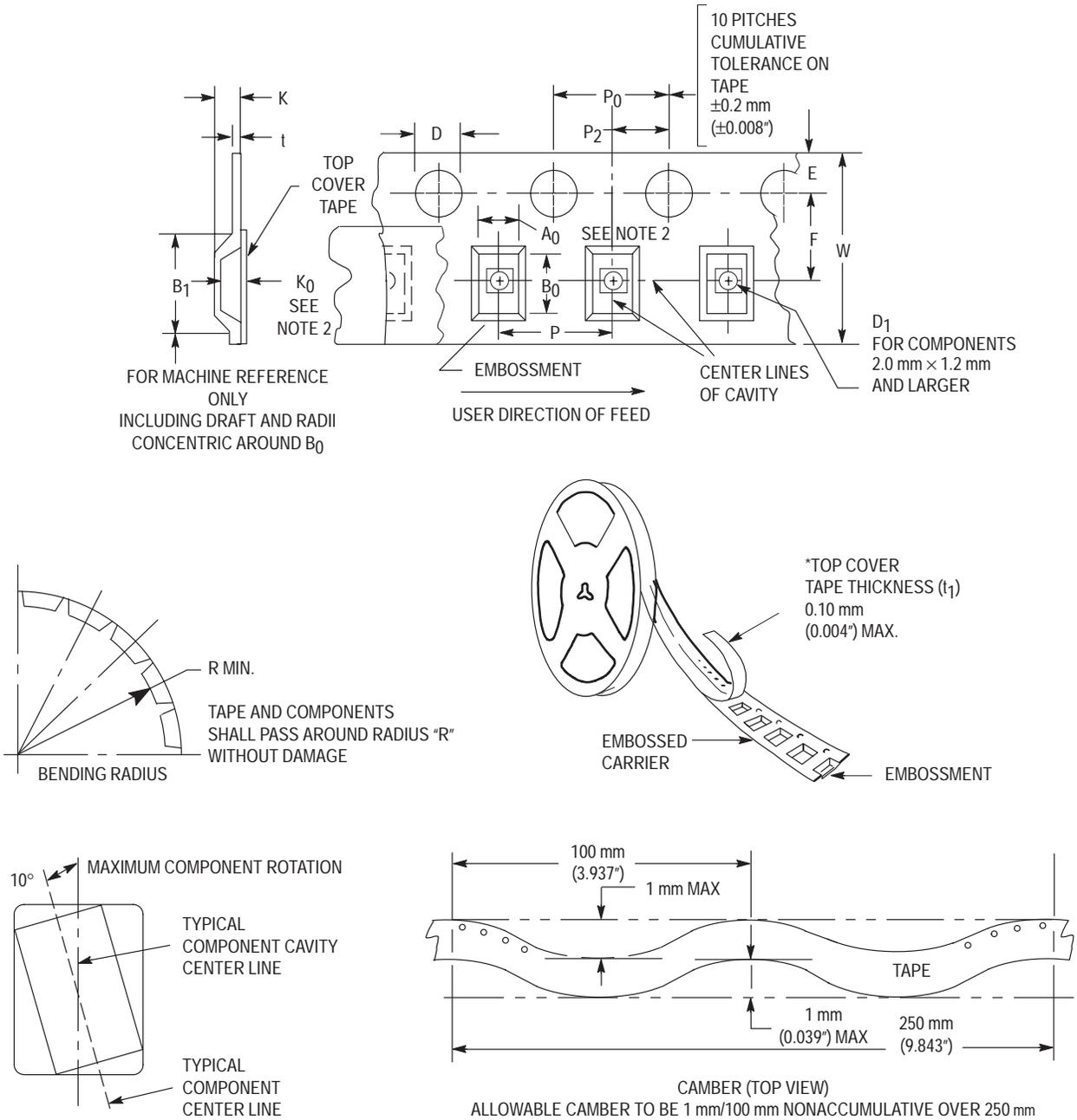


Figure 4. Carrier Tape Specifications

EMBOSSMENT CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B ₁ Max	D	D ₁	E	F	K	P	P ₀	P ₂	R	T	W
8 mm	4.35 mm (0.171")	1.5 +0.1/-0.0 mm (0.059 +0.004/-0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/-0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

1. Metric Dimensions Govern—English are in parentheses for reference only.
2. A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

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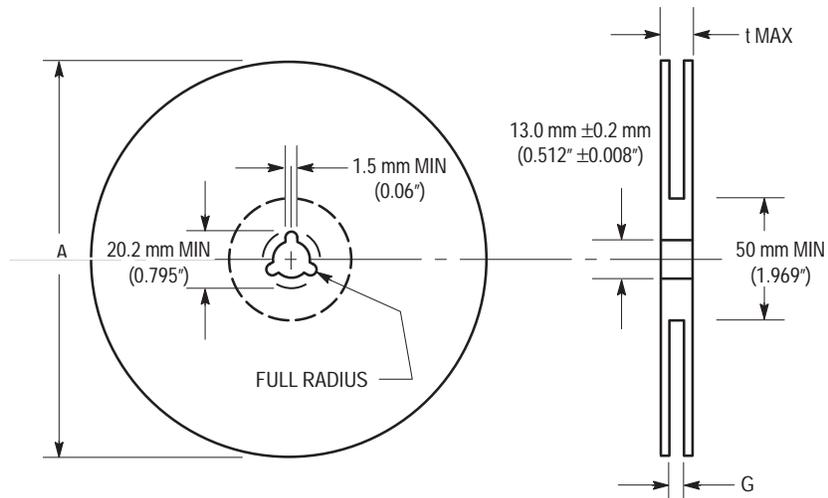


Figure 5. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
8 mm	330 mm (13")	8.400 mm, +1.5 mm, -0.0 (0.33", +0.059", -0.00)	14.4 mm (0.56")

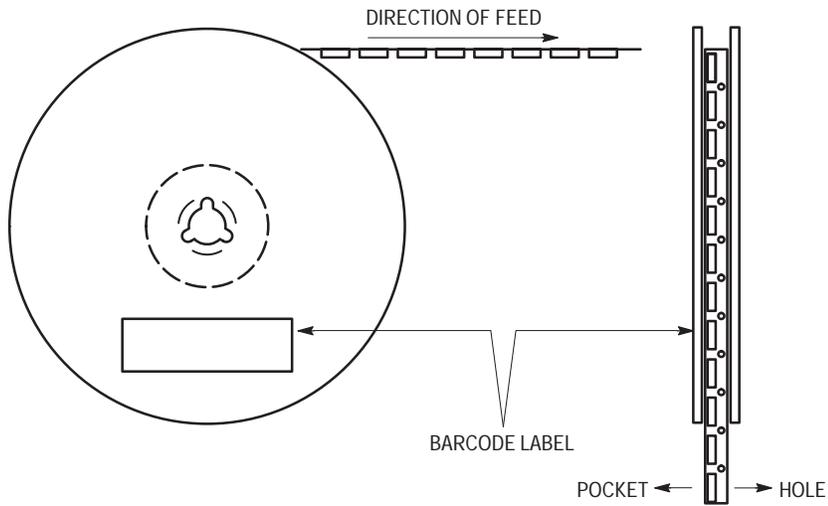


Figure 6. Reel Winding Direction

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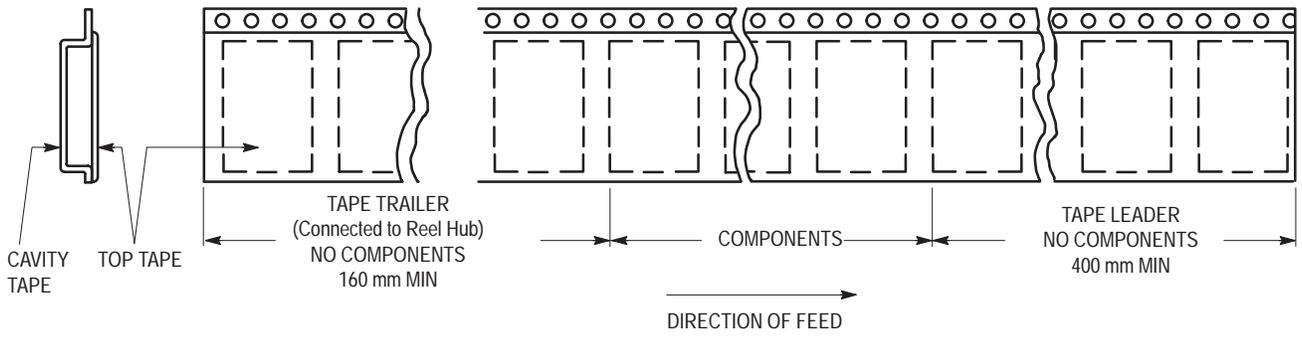


Figure 7. Tape Ends for Finished Goods

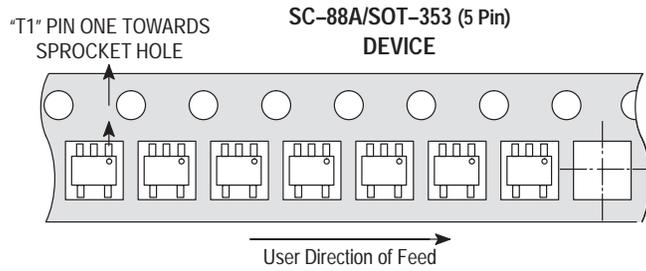


Figure 8. Reel Configuration

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