Product Preview

Analog Switch

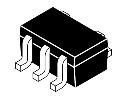
MC74VHC1G66

The MC74VHC1G66 is an advanced high speed CMOS bilateral analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The MC74VHC1G66 is compatible in function to a single gate of the High Speed CMOS MC74VHC4066 and the metal–gate CMOS MC14066. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage than R_{ON} of the metal–gate CMOS or High Speed CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pull–up resistors, it is compatible with LSTTL outputs.

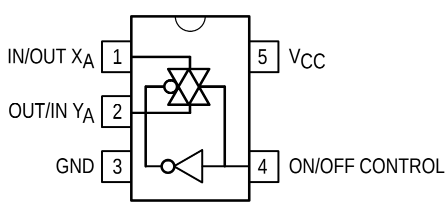
- High Speed: t_{PD} = **TBD** (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14066 or the HC4066
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V, CDM > 1500 V
- Chip Complexity: 11 FETs or 3 Equivalent Gates



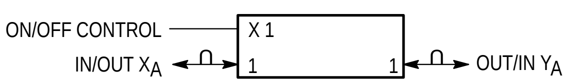
DF SUFFIX
5–LEAD SOT–353 PACKAGE
SC–88A
CASE 419A–01

FUNCTION TABLE

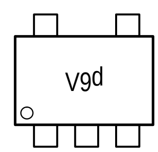
On/Off Control Input	State of Analog Switch
L	Off
H	On



5–Lead SOT–353 Pinout (Top View)



Logic Symbol



Pin 1
d = Date Code

Marking Diagram

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Motorola Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
MC74VHC1G66DFT1	MC	74	VHC1G	66	DF	T1	SC–88A	7–Inch/3000 Unit

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
Digital Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Analog Output Voltage	V_{IS}	–0.5 to V_{CC} + 0.5	V
Digital Input Diode Current	I_{IK}	–20	mA
DC Supply Current, V_{CC} and GND	I_{CC}	+25	mA
Power dissipation in still air, SC–88A †	P_D	200	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

†Derating — SC–88A Package: –3 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5.5	V
Digital Input Voltage	V_{IN}	GND	V_{CC}	V
Analog Input Voltage	V_{IS}	GND	V_{CC}	V
Static or Dynamic Voltage Across Switch	V_{IO}*		100	mV
Operating Temperature Range	T_A	–55	+125	°C
Input Rise and Fall Time ON/OFF Control Input V_{CC} = 3.3V ± 0.3V V_{CC} = 5.0V ± 0.5V	t_r , t_f	 0 0	 100 20	ns/V

* For voltage drops across the switch greater than 100mV (switch on), excessive V_{CC} current may be drawn; i.e. the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
I_{IN}	Maximum Input Leakage Current ON/OFF Control Input	$V_{IN} = V_{CC}$ or GND	0 to 5.5			±0.1		±1.0		±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND V_{IO} = 0V	5.5			2.0		20		40	µA
R_{ON}	Maximum "ON" Resistance	$V_{IN} = V_{IH}$ $V_{IS} = V_{CC}$ or GND $I_{IS} \le$ 20mA (Figure 1)	2.0 3.0 4.5		25 12 8	50 20 15		70 30 25		100 45 35	Ω
		Endpoints $V_{IN} = V_{IH}$ $V_{IS} = V_{CC}$ or GND $I_{IS} \le$ 20mA (Figure 1)	2.0 3.0 4.5		25 12 8	50 20 15		65 26 23		90 40 32	Ω
I_{OFF}	Maximum Off–Channel Leakage Current	$V_{IN} = V_{IL}$ $V_{IO} = V_{CC}$ or GND Switch Off (Figure 2)	5.5			0.1		0.5		1.0	µA
I_{ON}	Maximum On–Channel Leakage Current	$V_{IN} = V_{IH}$ $V_{IS} = V_{CC}$ or GND Switch On (Figure 3)	5.5			0.1		0.5		1.0	µA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	$T_A \le$ 85°C Min	$T_A \le$ 85°C Max	$T_A \le$ 125°C Min	$T_A \le$ 125°C Max	Unit
t_{PLH}, t_{PHL}	Maximum Propogation Delay, Input X to Y	Y_A = Open Figure 4	2.0 3.0 4.5 5.5		1 0 0 0	5 2 1 1		6 3 1 1		7 4 2 1	ns
t_{PLZ}, t_{PHZ}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
t_{PZL}, t_{PZH}	Maximum Propogation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω Figure 5	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Contol Input = GND Analog I/O Feedthrough	5.0		 4 4	 10 10		 10 10		 10 10	

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 1.)	18	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response Figure 7	f_{in} = 1 MHz Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads –3dB R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	150 175 200	MHz
ISO_{off}	Off–Channel Feedthrough Isolation Figure 8	f_{in} = Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0 kHz, R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	–40 –40 –40	
$NOISE_{feed}$	Feedthrough Noise Control to Switch Figure 9	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 2ns) Adjust R_L at setup so that I_S = 0 A R_L = 600Ω, C_L = 50 pF	3.0 4.5 5.5	45 60 130	mV_{PP}
		R_L = 50Ω, C_L = 10 pF	3.0 4.5 5.5	25 30 60	
THD	Total Harmonic Distortion Figure 10	f_{in} = 1 kHz, R_L = 10kΩ, C_L = 50 pF THD = $THD_{Measured}$ – THD_{Source} V_{IS} = 3.0 V_{PP} sine wave V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 3.3 4.5 5.5	 0.20 0.10 0.06	%

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

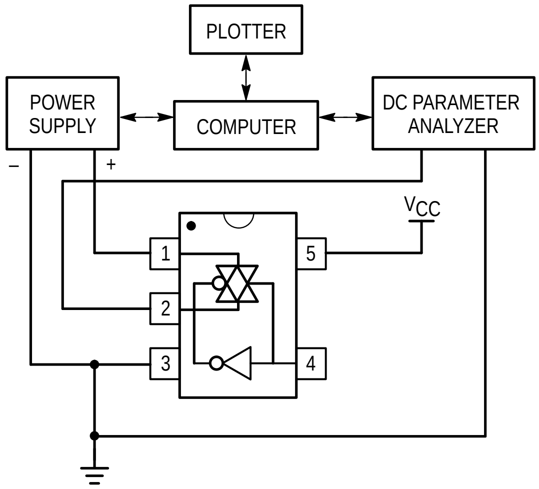


Figure 1. On Resistance Test Set–Up

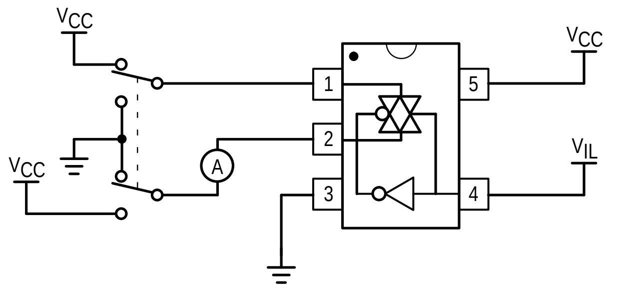


Figure 2. Maximum Off–Channel Leakage Current Test Set–Up

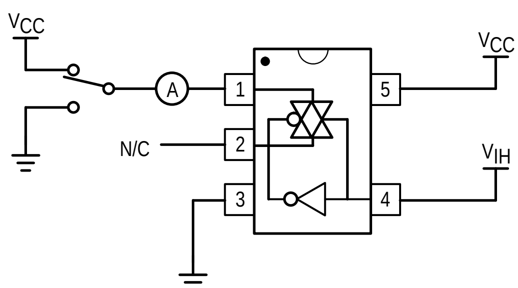


Figure 3. Maximum On–Channel Leakage Current Test Set–Up

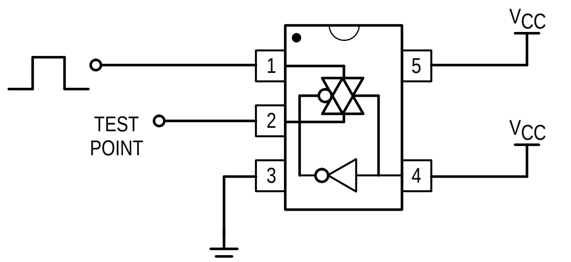


Figure 4. Propagation Delay Test Set–Up

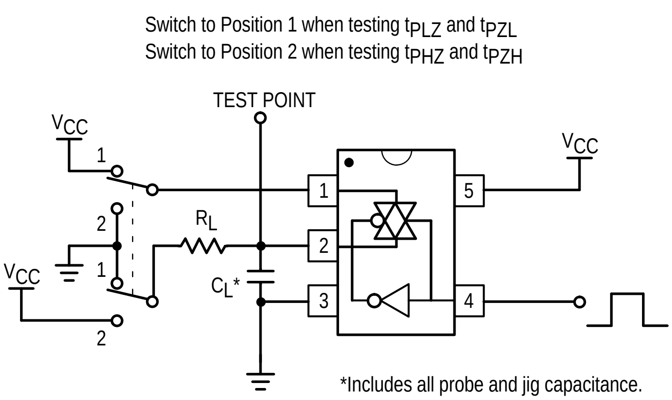


Figure 5. Propagation Delay Output Enable/Disable Test Set–Up

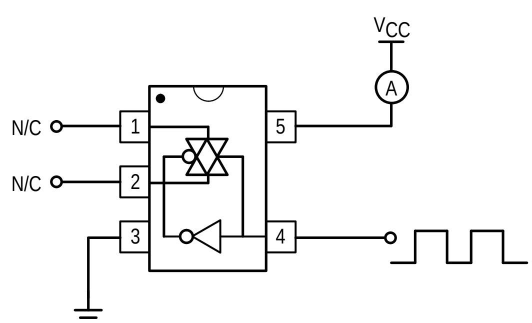


Figure 6. Power Dissipation Capacitance Test Set–Up

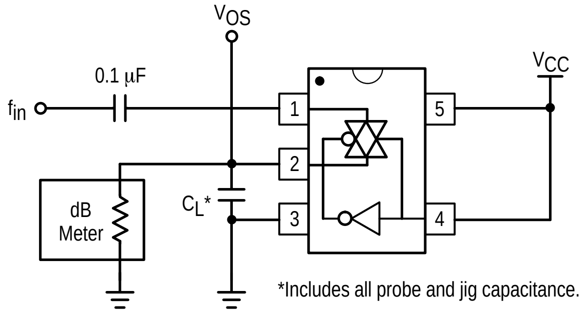


Figure 7. Maximum On–Channel Bandwidth Test Set–Up

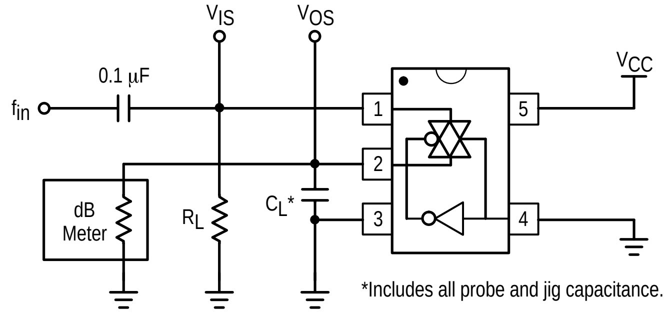


Figure 8. Off–Channel Feedthrough Isolation Test Set–Up

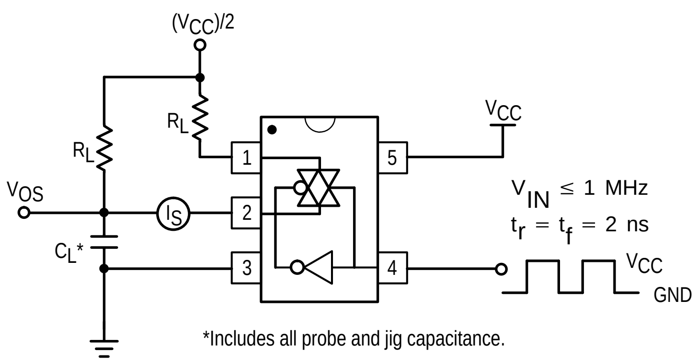


Figure 9. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set–Up

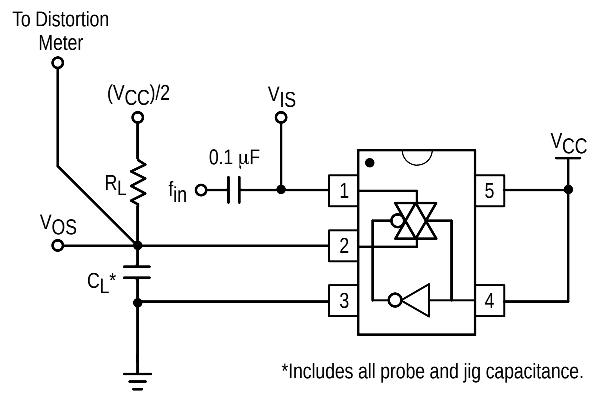


Figure 10. Total Harmonic Distortion Test Set–Up

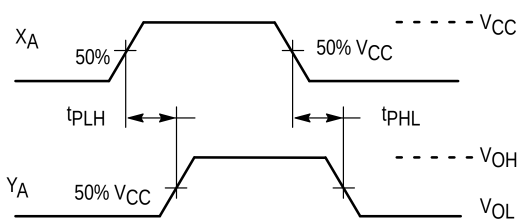


Figure 11. Propagation Delay, Analog In to Analog Out Waveforms

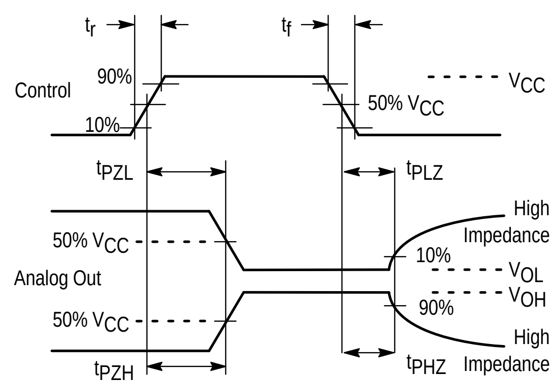


Figure 12. Propagation Delay, ON/OFF Control

OUTLINE DIMENSIONS

DF SUFFIX
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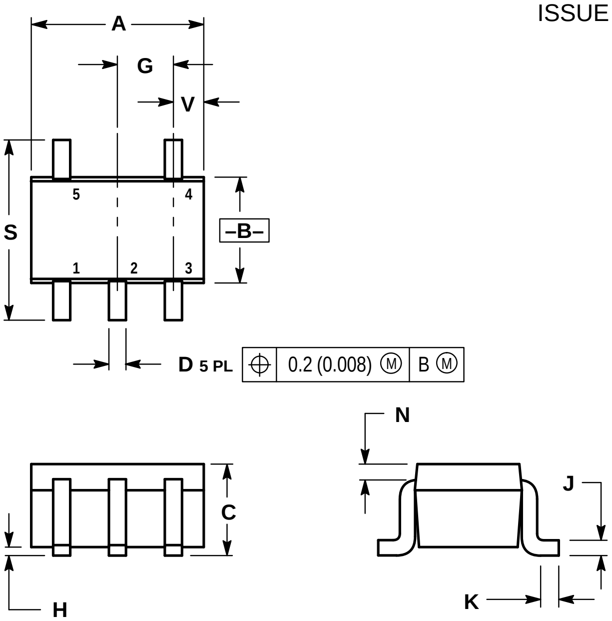
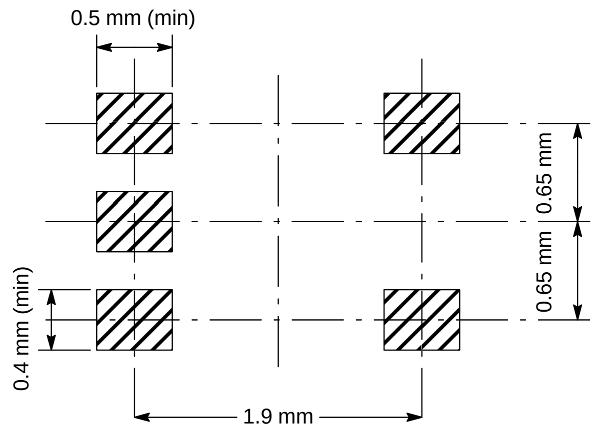
CASE 419A–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	—	0.004	—	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

SOT–353



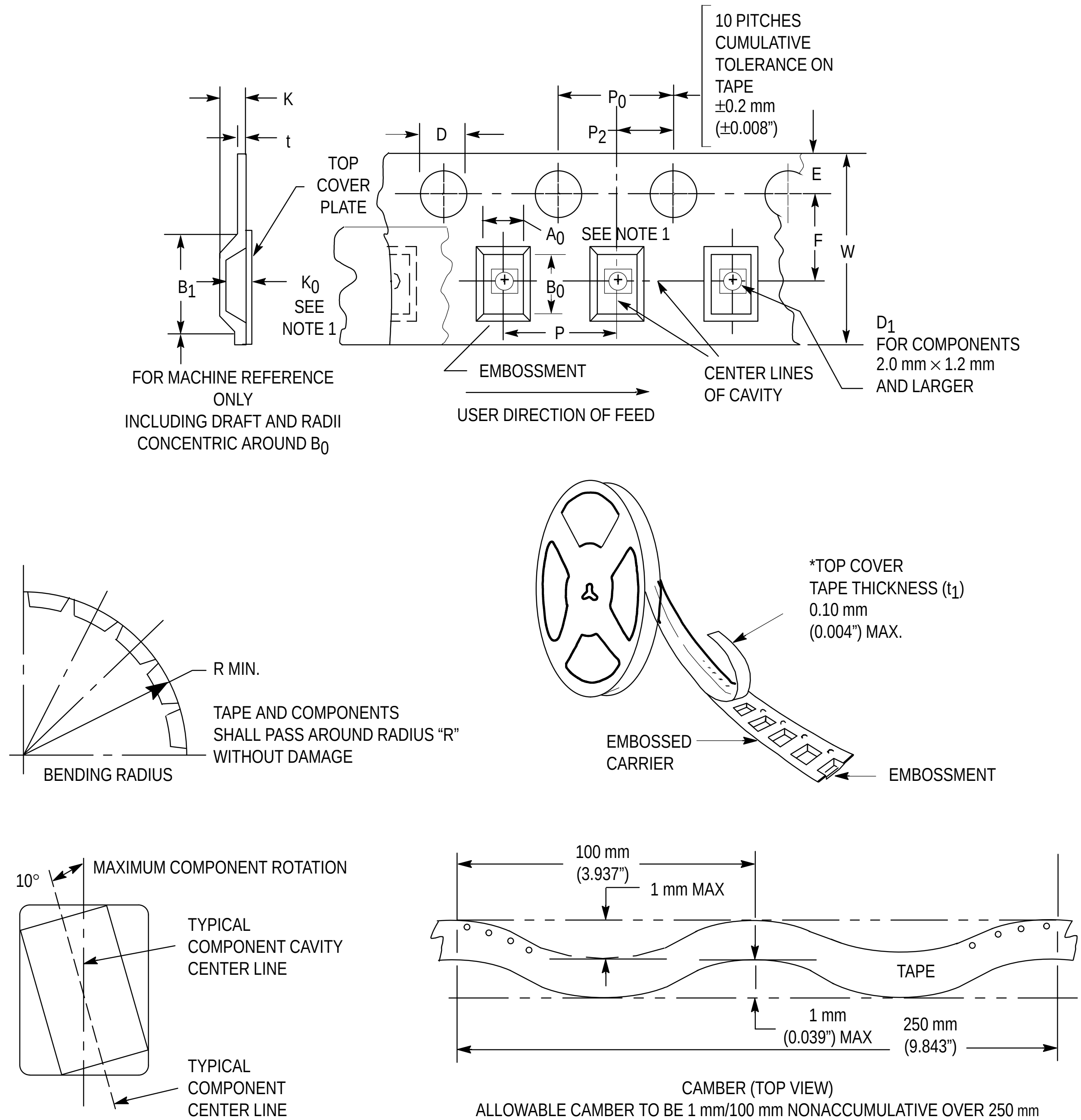


Figure 13. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 1 and 2)

Tape Size	B_1 Max	D	D_1	E	F	K	P	P_0	P_2	R	T	W
8 mm	4.55 mm (0.179")	1.5 +0.1/ –0.0 mm (0.059 +0.004/ –0.0")	1.0 mm Min (0.039")	1.75 ±0.1 mm (0.069 ±0.004")	3.5 ±0.5 mm (1.38 ±0.002")	2.4 mm (0.094")	4.0 ±0.10 mm (0.157 ±0.004")	4.0 ±0.1 mm (0.156 ±0.004")	2.0 ±0.1 mm (0.079 ±0.002")	25 mm (0.98")	0.3 ±0.05 mm (0.01 +0.0038/ –0.0002")	8.0 ±0.3 mm (0.315 ±0.012")

1. Metric Dimensions Govern–English are in parentheses for reference only.
2. A_0, B_0, and K_0 are determined by compnent size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

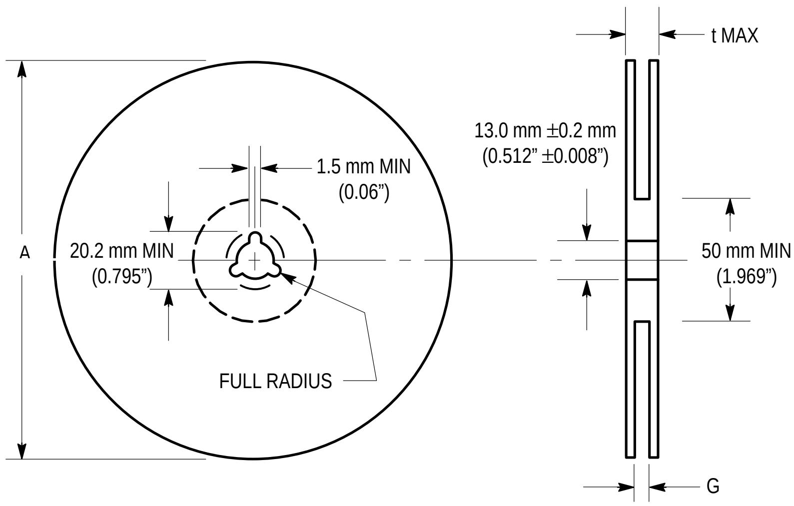


Figure 14. Reel Dimensions

REEL DIMIENSIONS

Tape Size	A Max	G	t Max
8 mm	330 mm (14.1")	8.400 mm, +1.5 mm, –0.0 (0.33", +0.059", –0.00)	14.4 mm (0.56")

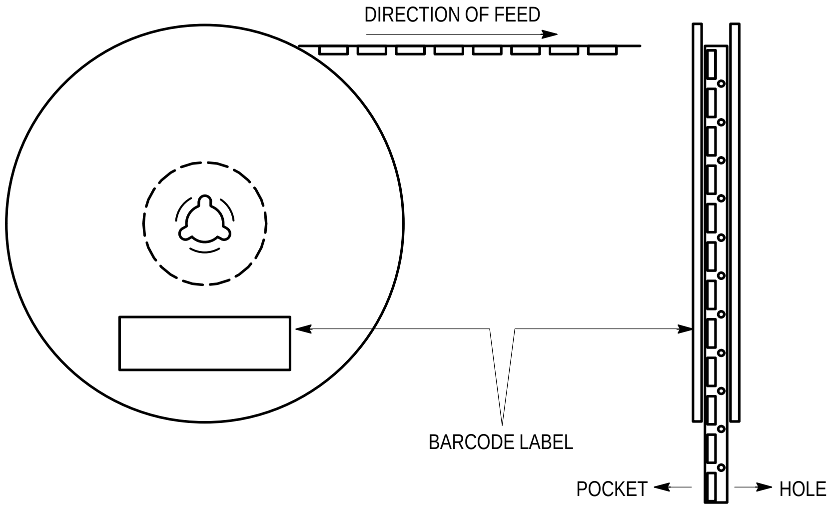


Figure 15. Reel Winding Direction

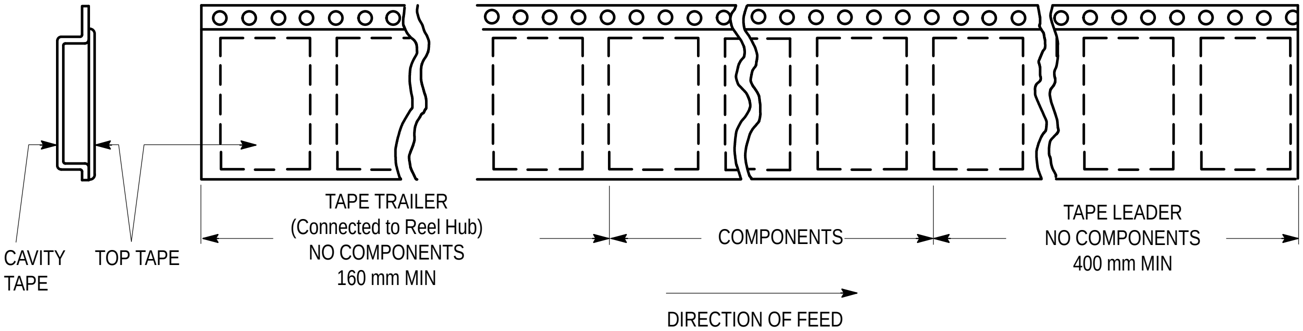


Figure 16. Tape Ends for Finished Goods

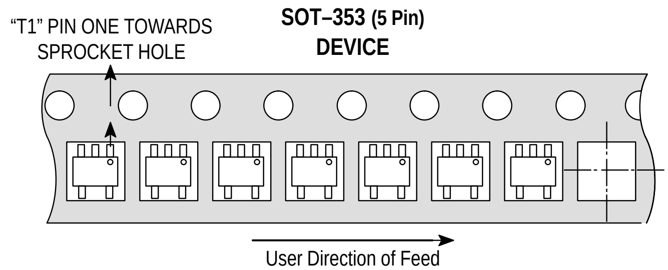


Figure 17. Reel Configuration

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