MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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Product Preview
Multiplexer - Demultiplexer

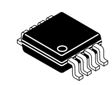
MC74VHC1G53

The MC74VHC1G53 is an advanced high speed CMOS multiplexer – demultiplexer analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining CMOS low power dissipation. This multiplexer – demultiplexer controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The MC74VHC1G53 is compatible in function to a single gate of the High Speed CMOS MC74VHC4053 and the metal–gate CMOS MC14053. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage than R_{ON} of the metal–gate CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs; with pull–up resistors, it is compatible with LSTTL outputs.

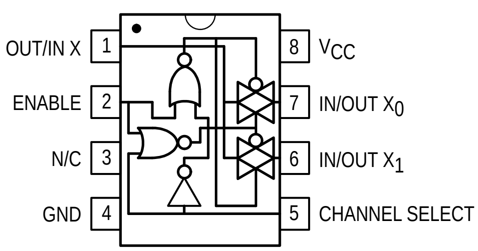
- High Speed: t_{PD} = 4 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max) at T_A = 25°C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage than the MC14053B or the HC4053
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V, CDM > 1500 V



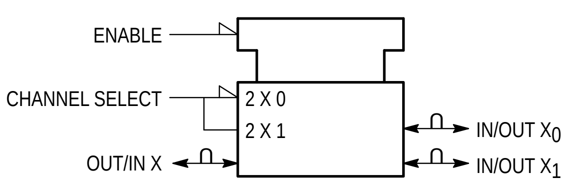
PLANNED PACKAGE
8–LEAD MICRO 8 PACKAGE
T_{amb} = –55°C to 125°C

FUNCTION TABLE

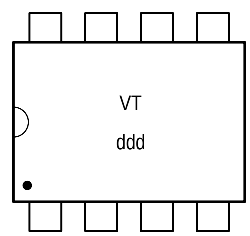
Enable	Select	ON Channel
L	L	X_0
L	L	X_1
H	X	NONE



PIN ASSIGNMENT



LOGIC SYMBOL



MARKING DIAGRAM
d = date code

DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Motorola Circuit Indicator	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
MC74VHC1G53DMT1	MC	74	VHC1G	53	DM	R2	Micro 8	13–Inch/4000 Unit

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur. Exposureto these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

Characteristics	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +7.0	V
Digital Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5	V
Analog Input Voltage	V_{IS}	–0.5 to V_{CC} + 0.5	V
Digital Input Diode Current	I_{IK}	–20	mA
DC Supply Current, V_{CC} and GND	I_{CC}	±25	mA
Power dissipation in still air, Micro–8 †	P_D	300	mW
Lead temperature, 1 mm from case for 10 s	T_L	260	°C
Storage temperature	T_{stg}	–65 to +150	°C

†Power Dissipation Derating: Micro–8 Package: – 4.4 mW/°C from 65°C to 125°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	2.0	5.5	V
Digital Input Voltage	V_{IN}	GND	V_{CC}	V
Analog Input Voltage	V_{IS}	GND	V_{CC}	V
Static or Dynamic Voltage Across Switch	V_{IO}*	—	100	mV
Operating Temperature Range	T_A	–55	+125	°C
Input Rise and Fall Time, SELECT & ENABLE V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	t_r, t_f	0 0	100 20	ns/V

* For voltage drops across the switch greater than 100 mV (switch on), excessive V_{CC} current may be drawn; i.e. the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \leq 85°C$ Min	$T_A \leq 85°C$ Max	$T_A \leq 125°C$ Min	$T_A \leq 125°C$ Max	Unit
V_{IH}	Minimum High–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
I_{IN}	Maximum Input Leakage Current ON/OFF Control Input	$V_{IN} = V_{CC}$ or GND	0 to 5.5			±0.1		±1.0		±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND V_{IO} = 0 V	5.5			2.0		20		40	µA
R_{ON}	Maximum "ON" Resistance	$V_{IN} = V_{IH}$ $V_{IS} = V_{CC}$ to GND $I_{IS} \leq 20$ mA (Figure 1)	2.0 3.0 4.5		25 12 5	50 20 10		70 30 15		100 45 25	Ω
		Endpoints $V_{IN} = V_{IH}$ $V_{IS} = V_{CC}$ to GND $I_{IS} \leq 20$ mA (Figure 1)	2.0 3.0 4.5		25 12 5	50 20 10		65 26 13		90 40 22	Ω
I_{OFF}	Maximum Off–Channel Leakage Current, Any One Channel	$V_{IN} = V_{IL}$ $V_{IO} = V_{CC}$ to GND Switch Off (Figure 2)	5.5			0.1		0.5		1.0	µA
	Maximum Off–Channel Leakage Current, Common Channel	$V_{IN} = V_{IL}$ $V_{IO} = V_{CC}$ to GND Switch Off (Figure 3)	5.5			0.1		1.0		2.0	µA
I_{ON}	Maximum On–Channel Leakage Current	$V_{IN} = V_{IH}$ $V_{IS} = V_{CC}$ to GND (Figure 4)	5.5			0.1		0.5		1.0	µA

AC ELECTRICAL CHARACTERISTICS (C_{load} = 50 pF, Input t_r/t_f = 3.0 ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$ Min	$T_A = 25°C$ Typ	$T_A = 25°C$ Max	$T_A \leq 85°C$ Min	$T_A \leq 85°C$ Max	$T_A \leq 125°C$ Min	$T_A \leq 125°C$ Max	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input X to X_0 or X_1	Figure 5	2.0 3.0 4.5 5.5		1 0 0 0	5 2 1 1		6 3 1 1		7 4 2 1	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, SELECT to Analog Output	Figure 6	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
t_{PZL}, t_{PZH} t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ENABLE to Analog Output	R_L = 1000 Ω Figure 7	2.0 3.0 4.5 5.5		15 8 6 4	35 15 10 7		46 20 13 9		57 25 17 11	ns
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Analog I/O (Control Input = GND) Feedthrough	5.0		4 4	10 10		10 10		10 10	

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (per Switch) (Note 1) Figure 8	18	pF

(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit † 25°C	Unit
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response Figure 9	f_{in} = 1 MHz Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads –3 dB R_L = 50 Ω, C_L = 10 pF	3.0 4.5 5.5	150 175 200	MHz
ISO_{off}	Off–Channel Feedthrough Isolation Figure 10	f_{in} = Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω, C_L = 50 pF	3.0 4.5 5.5	–50 –50 –50	dB
		f_{in} = 1.0 MHz, R_L = 50 Ω, C_L = 10 pF	3.0 4.5 5.5	–40 –40 –40	
$NOISE_{feed}$	Feedthrough Noise Channel Select to Switch Figure 11	V_{in} ≤ 1 MHz Square Wave (t_r = t_f = 2 ns) Adjust R_L at setup so that I_S = 0 A R_L = 600 Ω, C_L = 50 pF	3.0 4.5 5.5	45 60 100	mV_{PP}
		R_L = 50 Ω, C_L = 10 pF	3.0 4.5 5.5	25 30 60	
THD	Total Harmonic Distortion Figure 12	f_{in} = 1 kHz, R_L = 10 kΩ, C_L = 50 pF THD = $THD_{Measured}$ – THD_{Source} V_{IS} = 3.0 V_{PP} sine wave V_{IS} = 4.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 3.3 4.5 5.5	 0.20 0.10 0.06	%

†**Guaranteed limits not tested. Determined by design and verified by qualification.**

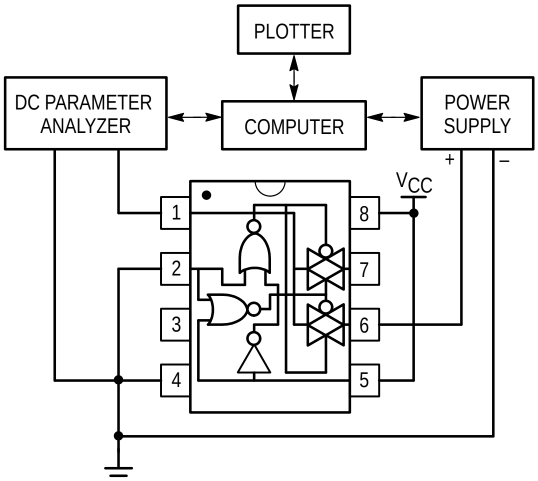


Figure 1. On Resistance Test Set–Up

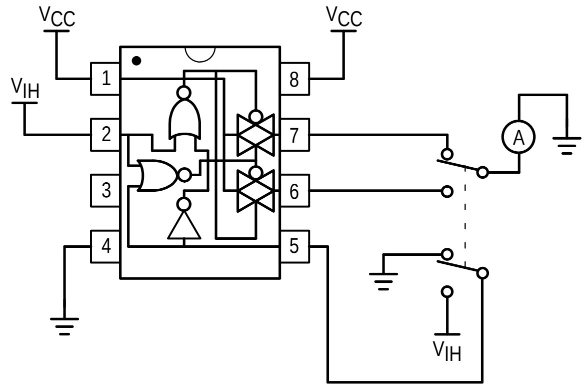


Figure 2. Maximum Off–Channel Leakage Current Test Set–Up, Any One Channel

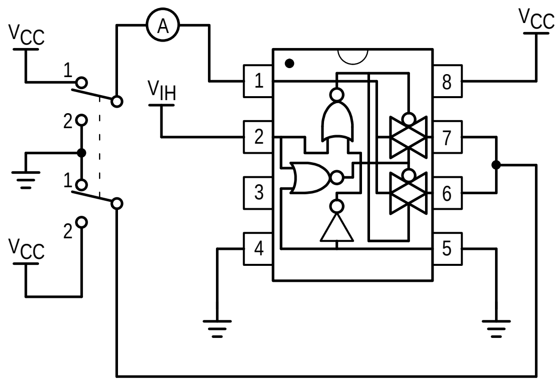


Figure 3. Maximum Off–Channel Leakage Current Test Set–Up, Common Channel

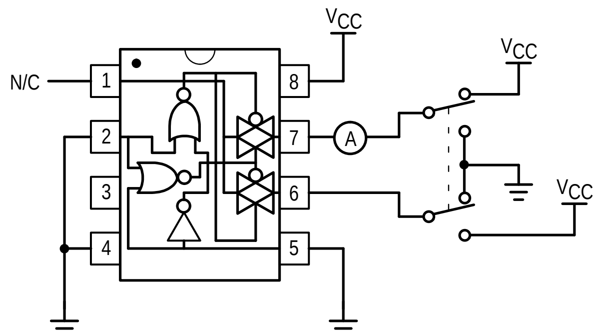


Figure 4. Maximum On–Channel Leakage Current Test Set–Up

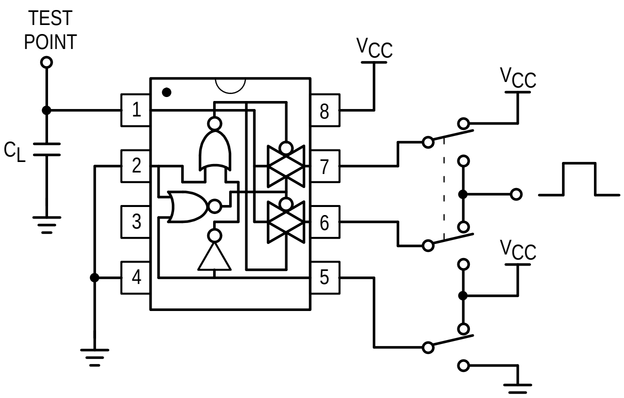


Figure 5. Propagation Delay Test Set–Up, Analog I/O to Analog I/O

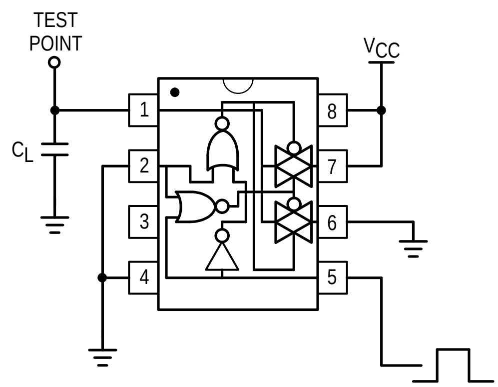


Figure 6. Propagation Delay Test Set–Up, Channel Select to Analog I/O

Switch SW1 to Position 1 when testing t_{PLZ} and t_{PZL}
Switch SW1 to Position 2 when testing t_{PHZ} and t_{PZH}
Testing should be repeated with Switch SW2 in Position 2 to test both channels

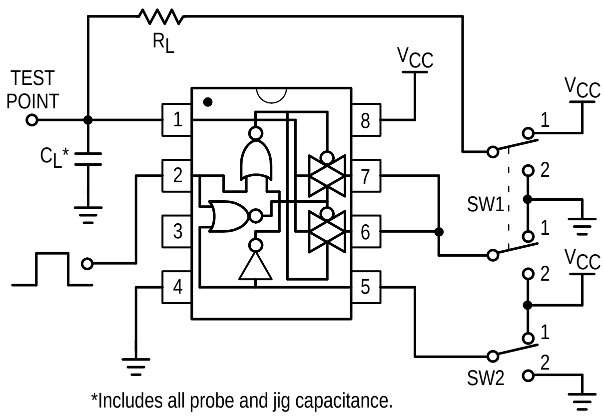


Figure 7. Propagation Delay Output Enable/ Disable to Analog Output Test Set–Up

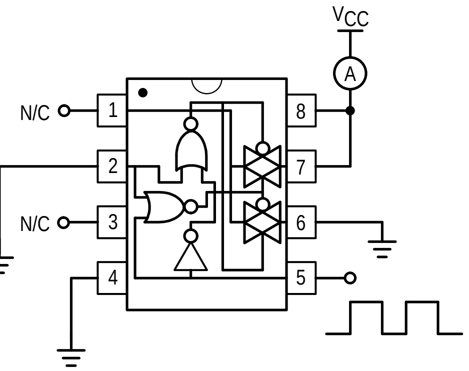


Figure 8. Power Dissipation Capacitance Test Set–Up

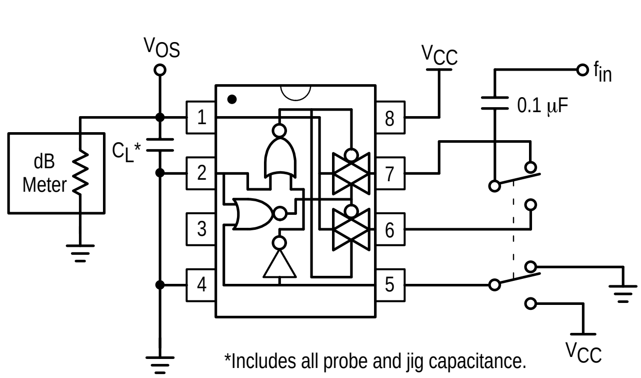


Figure 9. Maximum On–Channel Bandwidth Test Set–Up

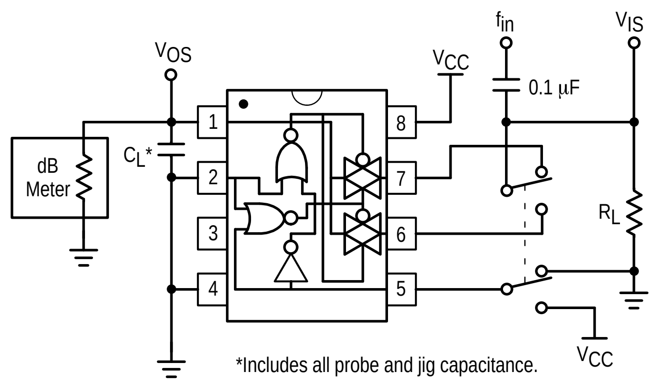


Figure 10. Off–Channel Feedthrough Isolation Test Set–Up

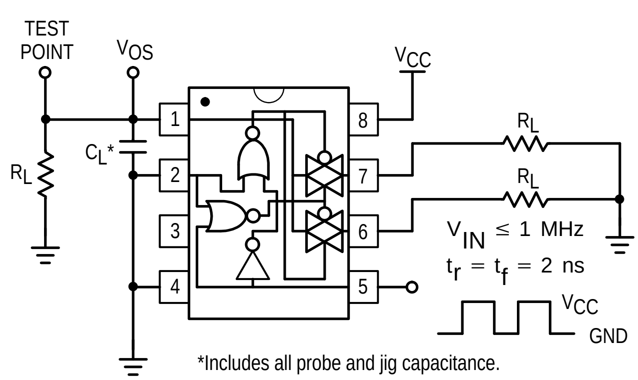


Figure 11. Feedthrough Noise, Channel Select to Analog Out, Test Set–Up

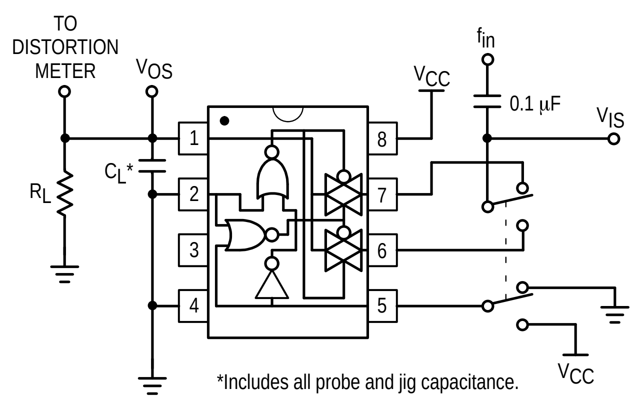
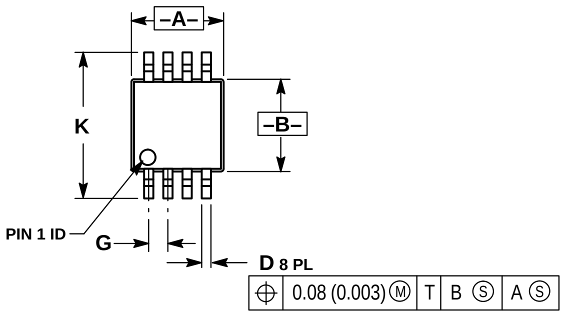
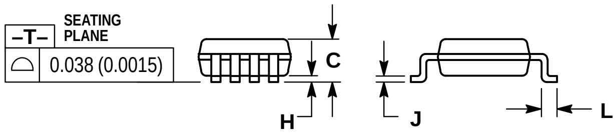


Figure 12. Total Harmonic Distortion Test Set–Up

OUTLINE DIMENSIONS

PLANNED PACKAGE
8–Lead Micro 8
T_{amb} = –55°C to 125°C





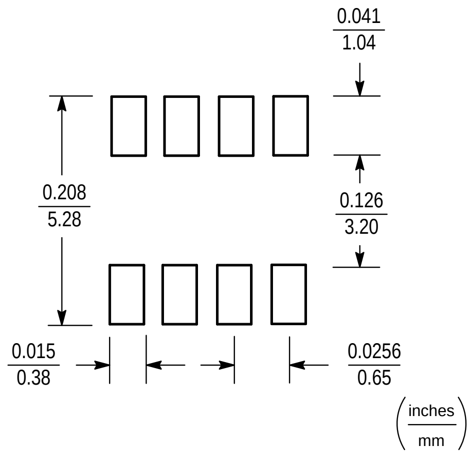
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

INFORMATION FOR USING THE Micro8 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.



Micro8 POWER DISSIPATION

The power dissipation of the Micro8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet for the Micro8 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 300 mW.

$$P_D = \frac{100°C - 25°C}{250°C/W} = 300 \text{ mW}$$

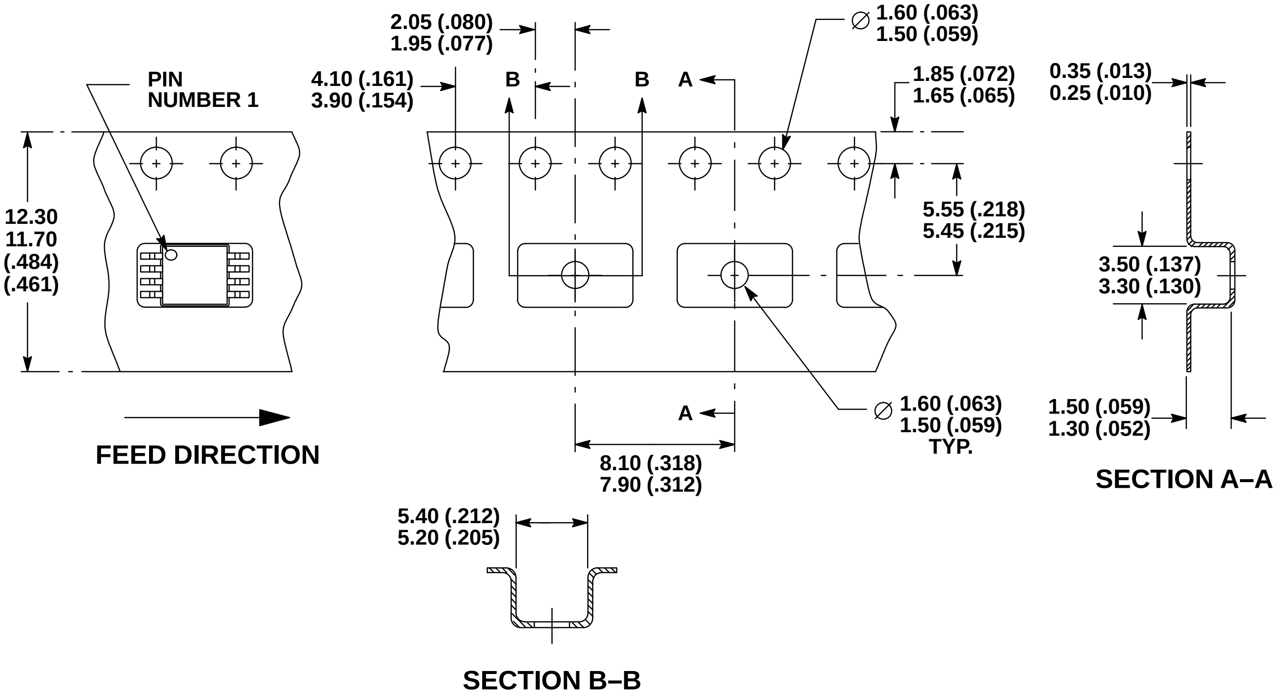
The 250°C/W for the Micro8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 300 mW using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.



NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.

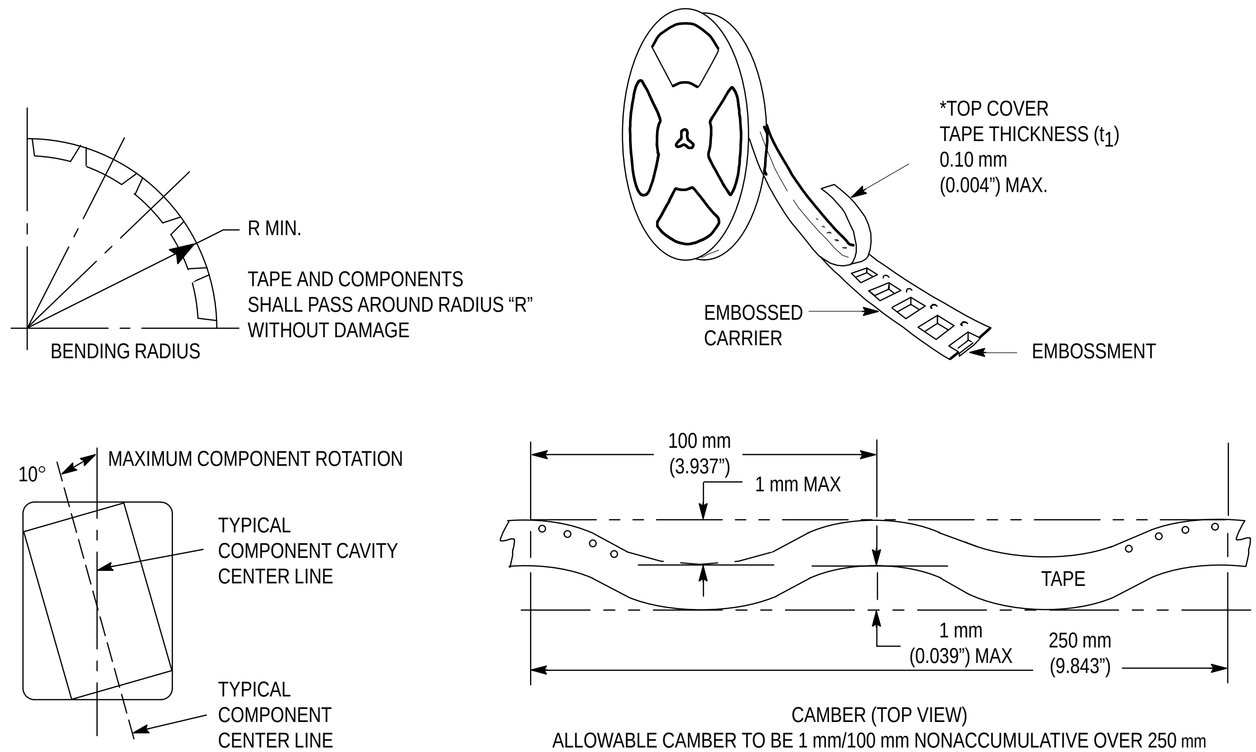


Figure 13. Carrier Tape Specifications

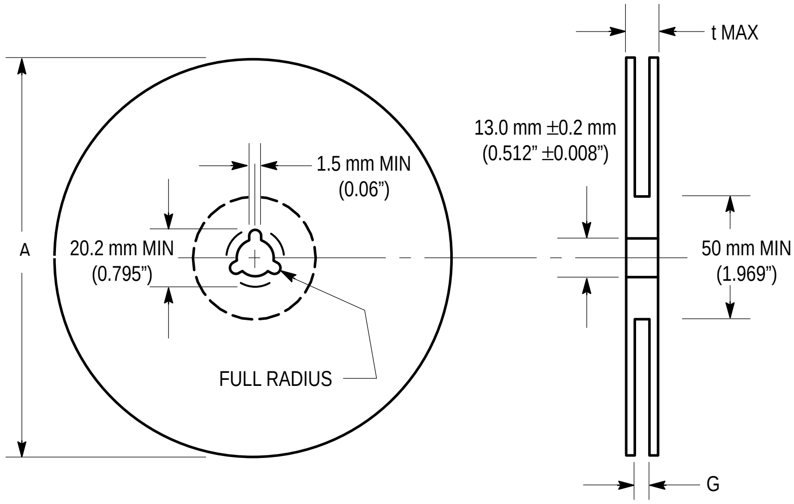


Figure 14. Reel Dimensions

REEL DIMIENSIONS

Tape Size	A Max	G	t Max
12 mm	330 mm (12.992”)	12.4 mm, +2.0 mm, –0.0 (0.49”, +0.079”, –0.00)	18.4 mm (0.72”)

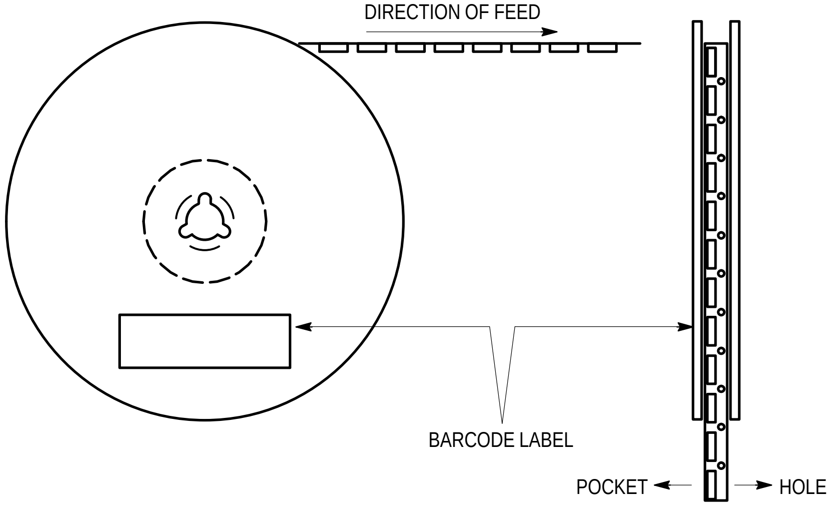


Figure 15. Reel Winding Direction

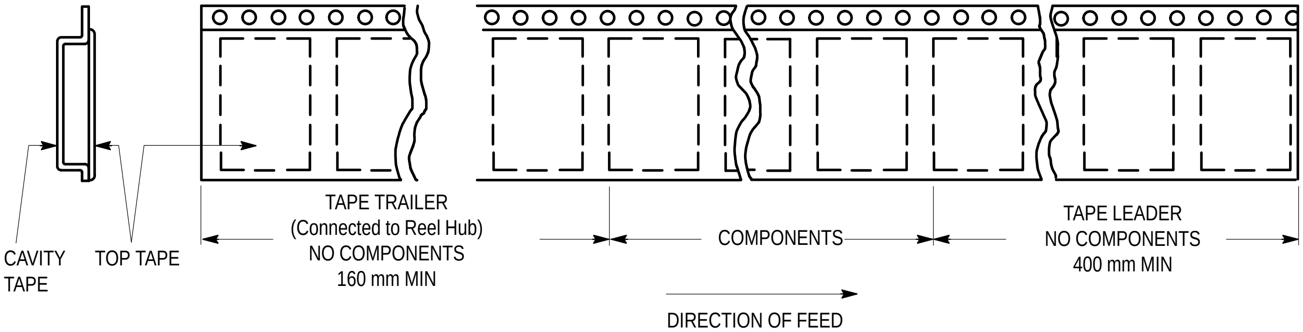


Figure 16. Tape Ends for Finished Goods

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