



MICROCIRCUIT DATA SHEET

MNLM139A-X-RH REV 0A0

Original Creation Date: 11/11/98
 Last Update Date: 12/11/98
 Last Major Revision Date: 11/11/98

LOW POWER LOW OFFSET VOLTAGE QUAD COMPARATOR: ALSO AVAILABLE GUARANTEED TO 100K RAD(Si) TESTED TO MIL-STD-883, METHOD 1019.5.

General Description

The LM139A consists of four independent precision voltage comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and the time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139A was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, it will directly interface with MOS logic-where the low power drain of the LM139A is a distinct advantage over standard comparators.

Industry Part Number

LM139A

NS Part Numbers

LM139AE/883
 LM139AJ-MLS
 LM139AJ-QMLV*
 LM139AJ/883
 LM139AJRQML**
 LM139AJRQMLV***
 LM139AW-MLS
 LM139AW-QMLV****
 LM139AW/883
 LM139AWG-QMLV*****
 LM139AWG/883
 LM139AWGRQML*****
 LM139AWGRQMLV*****
 LM139AWRQML*****
 LM139AWRQMLV*****

Prime Die

LM139

Controlling Document

See Features Page

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Wide supply voltage range
LM139A 2Vdc to 28Vdc or ± 1 Vdc to ± 14 Vdc
- Very low supply current drain (0.8 mA) - independent of supply voltage
- Low input biasing current 25nA
- Low input offset current ± 5 nA
and offset voltage ± 1 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250mV at 4mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- SMD : 5962-9673801VCA*, VDA****, VXA*****,
- SMD : 5962R9673801QCA**, VCA***, QXA*****, VXA*****, QDA*****, VDA*****

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage V+		36 Vdc or ± 18 Vdc
Differential Input Voltage (Note 5)		36 Vdc
Input Voltage		-0.3 Vdc to +36 Vdc
Input Current (Note 6) (Vin < -0.3 Vdc)		50mA
Power Dissipation (Note 2, 3)		
LCC		1250mW
CERDIP		1200mW
CERPACK		680mW
CERAMIC S.O.I.C.		680mW
Output Short-Circuit to GND (Note 4)		Continuous
Maximum Junction Temperature		150 C
Storage Temperature Range		-65 C to +150 C
Lead Temperature (Soldering, 10 seconds)		260 C
Operating Temperature Range		-55 C to +125 C
Thermal Resistance		
ThetaJA		
LCC	(Still Air)	100 C/W
	(500LF/Min Air flow)	73 C/W
CERDIP	(Still Air)	103 C/W
	(500LF/Min Air flow)	65 C/W
CERPACK	(Still Air)	183 C/W
	(500LF/Min Air flow)	120 C/W
CERAMIC S.O.I.C.	(Still Air)	183 C/W
	(500LF/Min Air flow)	120 C/W
ThetaJC		
LCC		28 C/W
CERDIP		23 C/W
CERPACK		23 C/W
CERAMIC S.O.I.C.		23 C/W
ESD Tolerance (Note 7)		600V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{dmax} = (T_{jmax} - TA)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small ($P_d \leq 100mW$), provided the output transistors are allowed to saturate.

(Continued)

- Note 4: Short circuits from the output to V+ can cause excessive heating and eventual destruction. When considering short circuit to ground, the maximum output current is approximately 20mA independent of the magnitude of V+.
- Note 5: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -3.0 Vdc (or 0.3 Vdc below the magnitude of the negative power supply, if used) (at 25 C).
- Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to the diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 Vdc (at 25 C).
- Note 7: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS: See NOTE 3

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_+ = 5V$, $V_{cm} = 0$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
I _{cc}	Supply Current	R _l = Infinity				2	mA	1, 2, 3
		V ₊ = 30V, R _l = Infinity				2	mA	1, 2, 3
I _{ce_x}	Output Leakage Current	V ₊ = 30V, V _o = 30V				1	μA	1, 2, 3
V _{sat}	Saturation Voltage	I _{sink} = 4mA				400	mV	1
						700	mV	2, 3
I _{sink}	Output Sink Current	V _o = 1.5V			6		mA	1
V _{io}	Input Offset Voltage				-2	2	mV	1
					-4	4	mV	2, 3
			V ₊ = 30V		-2	2	mV	1
					-4	4	mV	2, 3
			V ₊ = 30V, V _{cm} = 28.5V, V _{out} = 1.5V		-2	2	mV	1
	V ₊ = 30V, V _{cm} = 28.0V, V _{out} = 1.5V			-4	4	mV	2, 3	
+I _{bias}	Input Bias Current	V _o = 1.5V			-100	-1	nA	1
					-300	-1	nA	2, 3
-I _{bias}	Input Bias Current	V _o = 1.5V			-100	-1	nA	1
					-300	-1	nA	2, 3
I _{io}	Input Offset Current	V _o = 1.5V			-25	25	nA	1
					-100	100	nA	2, 3
PSRR	Power Supply Rejection Ratio	V ₊ = 5V to 30V			60		dB	1
CMRR	Common Mode Rejection Ratio	V ₊ = 30V, V _{cm} = 0V to 28.5V			60		dB	1
A _v	Voltage Gain	V ₊ = 15V, R _l ≥ 15K Ohms, V _{out} = 1V to 11V			50		V/mV	1
V _{cm}	Common Mode Voltage Range	V ₊ = 30V	1		0	V ₊ - 1.5	V	1
			1		0	V ₊ - 1.5	V	2, 3
V _{diff}	Differential Input Voltage	V ₊ = 30V, V _{diff} = 36V	2			500	nA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: See NOTE 3

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: $V_+ = 5V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
t _{RLH}	Response Time					5	uS	4
						0.8	uS	4
t _{RHL}	Response Time					2.5	uS	4
						0.8	uS	4

DC PARAMETERS: DRIFT VALUES (See NOTE 3)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_+ = 5V$, $V_{cm} = 0V$. "Deltas not required on B-Level product. Deltas required for S-Level (-MLS) product as specified on Internal Processing Instructions (IPI) and for QMLV product at Group B, Subgroup 5 ONLY."

V _{io}	Input Offset Voltage				-1	1	mV	1
+I _{bias}	Input Bias Current	$V_o = 1.5V$			-15	15	nA	1
-I _{bias}	Input Bias Current	$V_o = 1.5V$			-15	15	nA	1
I _{io}	Input Offset Current	$V_o = 1.5V$			-10	+10	nA	1

DC/AC PARAMETERS: POST RADIATION LIMITS +25 C (See NOTE 3)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: $V_+ = 5V$, $V_{cm} = 0V$.
AC: $V_+ = 5V$

V _{io}	Input Offset Voltage	$V_+ = 5V$, $V_{cm} = 0$	3		-2.5	2.5	mV	1
		$V_+ = 30V$, $V_{cm} = 0$	3		-2.5	2.5	mV	1
		$V_+ = 30V$, $V_{cm} = 28.5V$, $V_{out} = 1.5V$	3		-2.5	2.5	mV	1
		$V_+ = 30V$, $V_{cm} = 28.0V$, $V_{out} = 1.5V$	3		-2.5	2.5	mV	1
+I _{bias}	Input Bias Current	$V_o = 1.5V$	3		-110	-1	nA	1
-I _{bias}	Input Bias Current	$V_o = 1.5V$	3		-110	-1	nA	1
t _{RLH}	Response Time		3			0.9	uS	4

Note 1: Parameter guaranteed by V_{io} tests.

Note 2: V_{diff} is measured by applying +36V/-36V, with reference to gnd, to the two inputs.

Note 3: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019.5

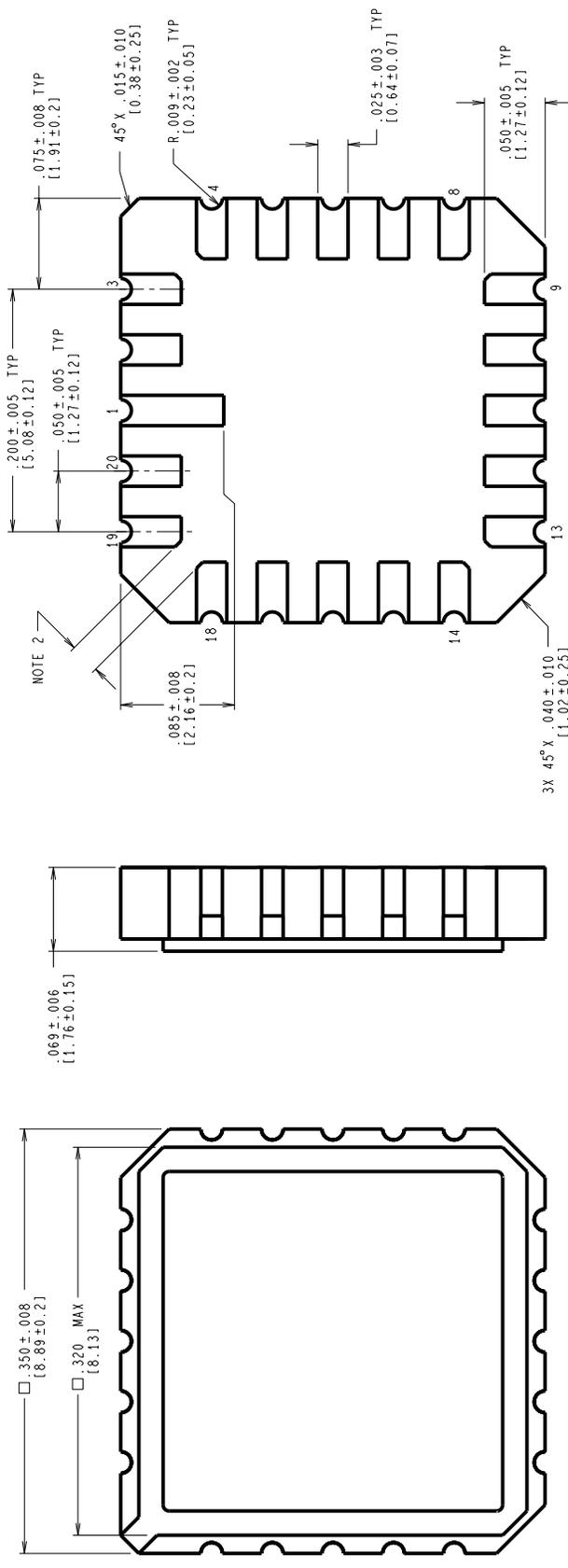
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
5542HRA2	(blank)
5715HRA2	CERPACK (W), 14 LEAD (B/I CKT)
5816HRA3	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000184A	CERPACK (W), 14 LEAD (PINOUT)
P000201A	LCC (E), TYPE C, 20 TERMINAL (PINOUT)
P000238A	CERAMIC SOIC (WG), 14 LEAD (PINOUT)
P000271A	CERDIP (J), 14 LEAD (PINOUT)
W14BRN	CERPACK (W), 14 LEAD (P/P DWG)
WG14ARC	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

SE
L1
LE
BO

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW	10005	02/10/94 DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

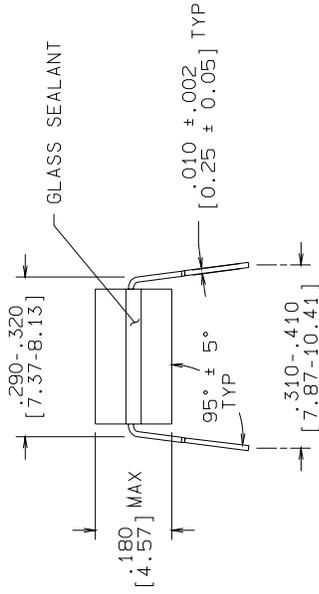
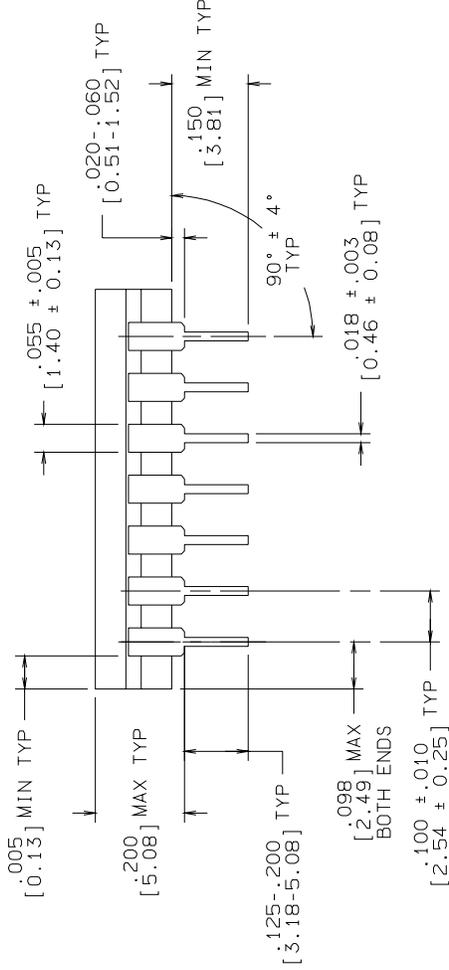
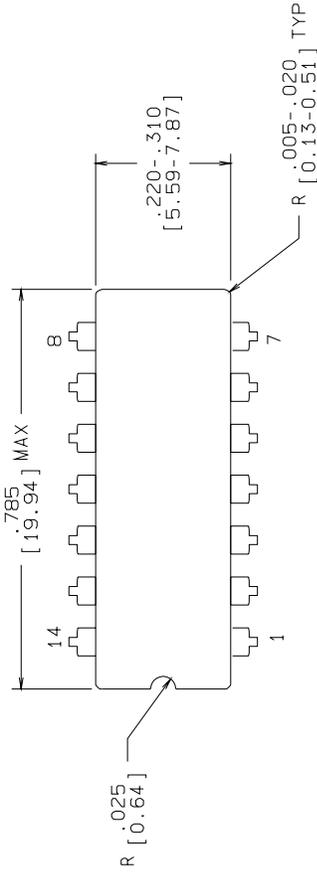
- LEAD FINISH TO BE ONE OF THE FOLLOWING:
 - 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.
 - SOLDER DIP. SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.
- CORNER PADS MAY HAVE A 45° X 0.20 IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE 0.15 IN/0.38mm DIMENSION.
- REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS		DATE
DRN	Design	02/10/94
CHK	Eng	
CHK	Eng	
APPROVAL		

		NATIONAL SEMICONDUCTOR CORPORATION 2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL			
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E
DO NOT SCALE DRAWING			
SHEET 1 of 1			

R E V I S I O N S			
LTR	DESCRIPTION	E.C.N.	DATE
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93
			TL/



CONTROLLING DIMENSION: INCH

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICRONS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

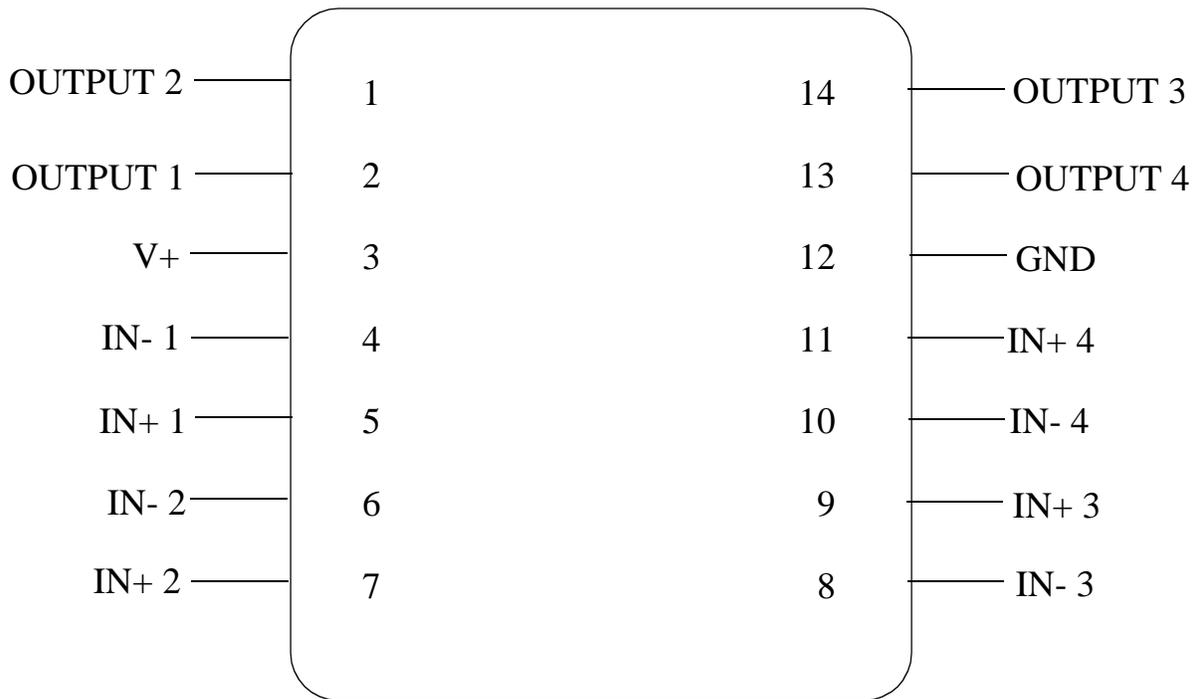
MIL/AERO MIL-M-38510
 CONFIGURATION CONTROL CONFIGURATION CONTROL

APPROVALS	DATE	APPROVALS	DATE
DRAWN: T. LEQUANG	09/15/93		
DFTG. CHK.			
ENGR. CHK.			
APPROVAL			

 PROJECTION INCH [MM]		SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H		
DO NOT SCALE DRAWING		SHEET	1	OF	1

NATIONAL SEMICONDUCTOR CORPORATION
 2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J),
 14 LEAD,



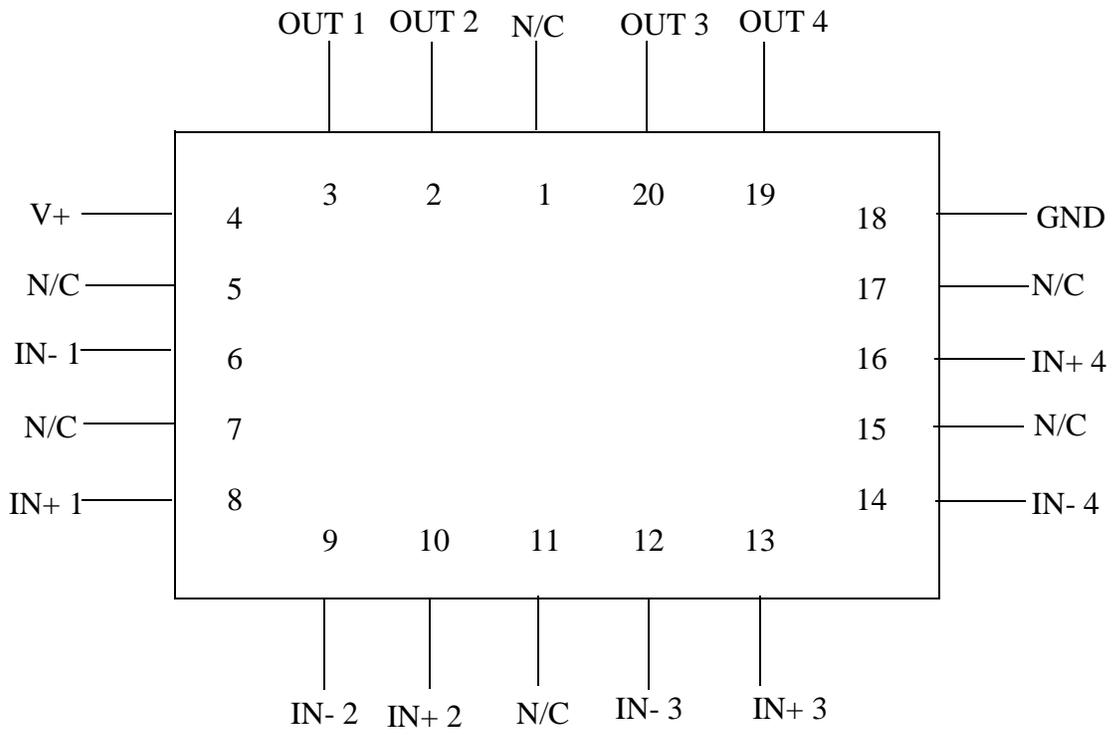
LM139AW, LM139W
14 - LEAD CERPACK
CONNECTION DIAGRAM

TOP VIEW
P000184A

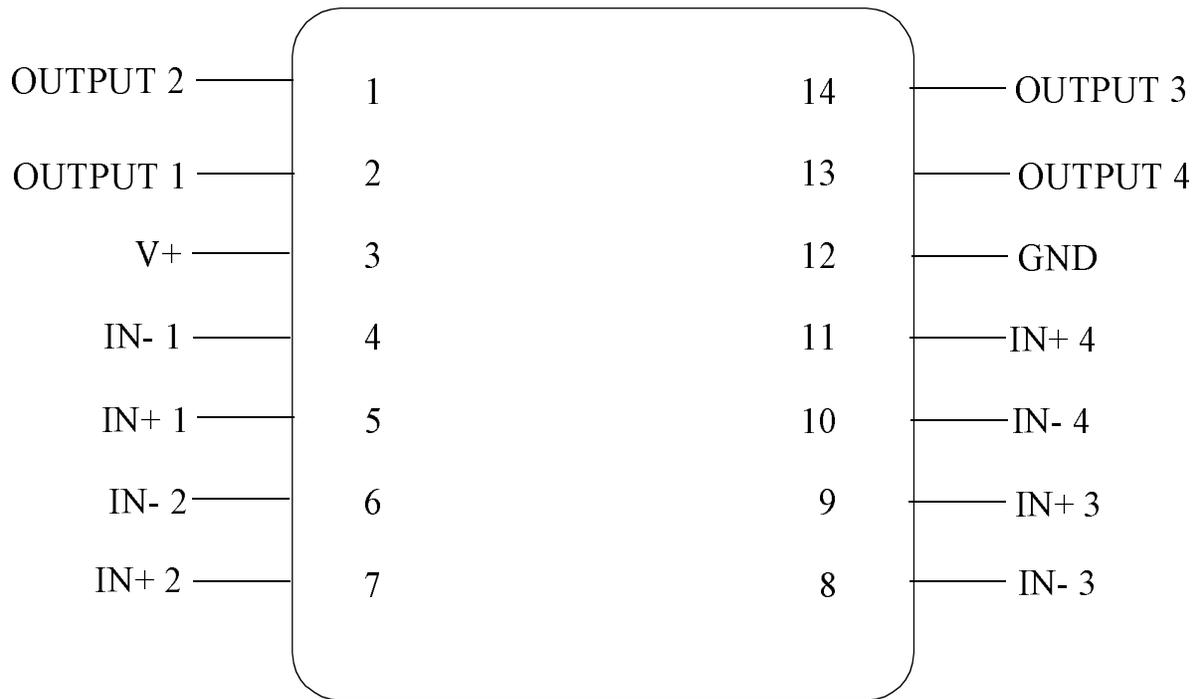


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MIL/AEROSPACE OPERATIONS
 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050



LM139AE, LM139E
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000201A



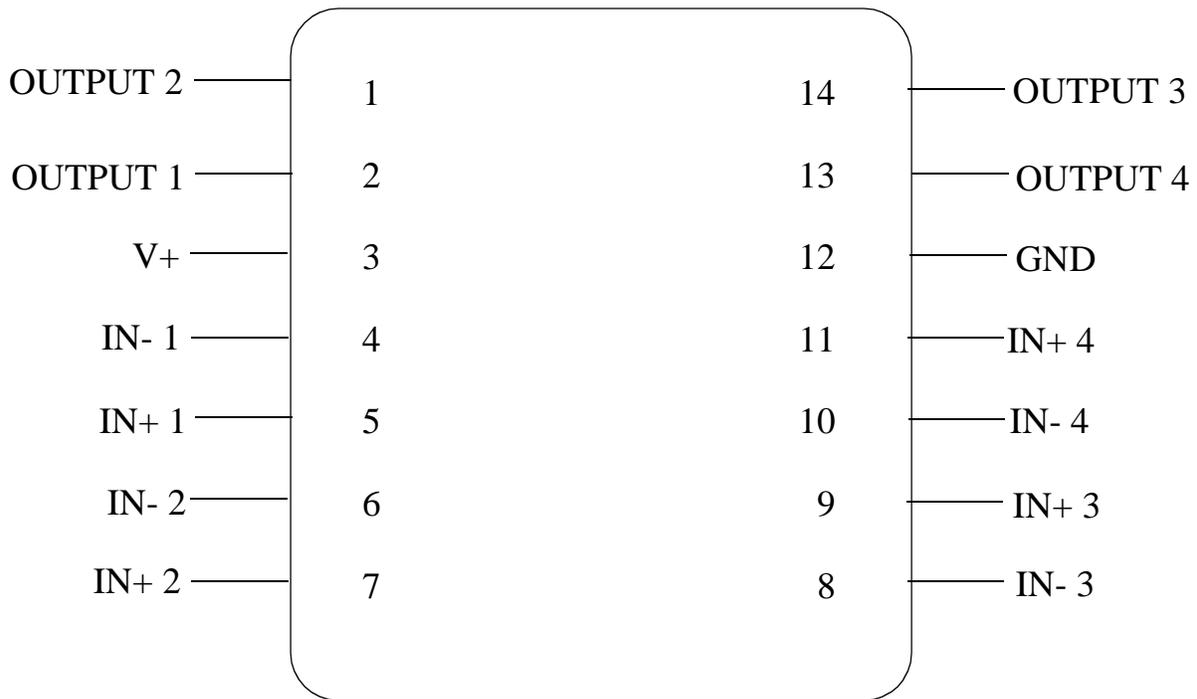
LM139AWG, LM139WG
14 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM

TOP VIEW
P000238A



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 2900 SEMICONDUCTOR DRIVE
 SANTA CLARA, CA 95050



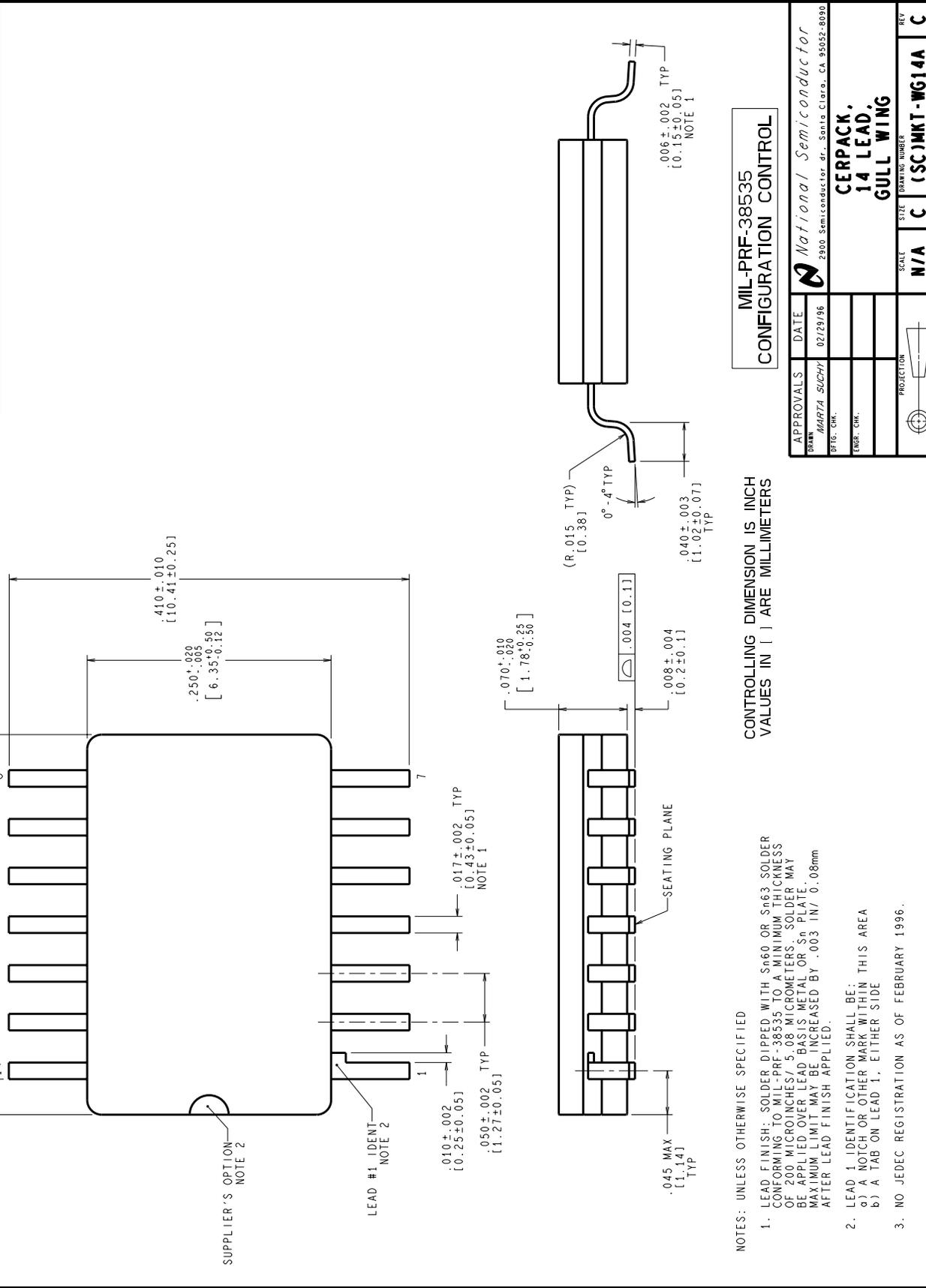
LM139AJ, LM139J
14 - LEAD DIP
CONNECTION DIAGRAM
TOP VIEW
P000271A



National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
A	RELEASE TO DOCUMENT CONTROL	11375	02/29/1996
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM. .040±.003 WAS .037±.003	11442	04/19/1996
C	R. .015(0.38) WAS R. .006(0.15)	11839	10/08/1997

APPROVALS	DATE	BY/APP'D
DRN MARTA SUCHY	02/29/96	MS/KH
DATE CHK.		MS/KH
ENGR. CHK.		TL/



- NOTES: UNLESS OTHERWISE SPECIFIED
- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
 - LEAD 1 IDENTIFICATION SHALL BE:
 - A NOTCH OR OTHER MARK WITHIN THIS AREA
 - A TAB ON LEAD 1, EITHER SIDE
 - NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

**MIL-PRF-38535
CONFIGURATION CONTROL**

 National Semiconductor 2800 Semiconductor Dr., Santa Clara, CA 95052-8000	
SCALE	N/A
SIZE	C
DRAWING NUMBER	(SC)MKT-WG14A
REV	C

DO NOT SCALE DRAWING SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003131	12/11/98	Rose Malone	Initial MDS Release: MNLM139A-X-RH, Rev. 0A0 - Added Rad Hard Devices and Limits. Replaces MNLM139A-X, Rev. 1E1.