



MICROCIRCUIT DATA SHEET

MNDS26LV32A-X REV 0A0

Original Creation Date: 11/19/98
 Last Update Date: 02/11/99
 Last Major Revision Date:

3V ENHANCED CMOS QUAD DIFFERENTIAL LINE RECEIVER

General Description

The DS26LV32A is a high speed quad differential CMOS receiver that is comparable to TIA/EIA-422-B and ITU-T V.11 standards, but with a specified common mode voltage range of -0.5V to +5.5V due to the lower operating supply voltage of 3.0V to 3.6V. The TRI-STATE enables, EN and \overline{EN} , allow the device to be active High or active Low. The enables are common to all four receivers. The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as $\pm 200mV$ over the common mode range of -0.5V to +5.5V. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Industry Part Number

DS26LV32A

NS Part Numbers

DS26LV32AW-QML

Prime Die

DS26LV32A

Controlling Document

5962-9858501QFA

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Low power CMOS design
- $\pm 0.2V$ sensitivity over the entire common mode range
- Input fail-safe circuitry
- Inputs won't load line when $V_{cc} = 0V$
- TRI-STATE outputs for connection to system buses
- ESD Rating (HBM, 1.5K ohm, 100pF) $\geq 2000V$
- Typical Part to Part Skew < TBD

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vcc)	7V
Common Mode Range (Vcm)	±14V
Differential Input Voltage (Vdiff)	±14V
Enable Input Voltage (Vin)	-0.5V to Vcc +0.5V
Storage Temperature Range (Tstg)	-65 C to +150 C
Lead Temperature (Soldering 4 seconds)	260 C
Maximum Power Dissipation +25C (Note 2)	1087 mW
Thermal Resistance. (Theta JA)	138 C/Watt
Thermal Resistance. (Theta JC)	13.5 C/Watt

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Derate W package 7.3mW/C above +25C.

Recommended Operating Conditions

Operating Voltage (Vcc)	3.0V to 3.6V
Operating Temperature Range (TA)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vth	Minimum Differential Input Voltage	Vcc=3.0/3.6V, Vout=Voh or Vol, -0.5V<Vcm<+5.5V			-200	+200	mV	1, 2, 3
Rin	Input Resistance	Vcc=3.6V, -0.5V<Vcm<+5.5V, "One input AC Gnd"			5		KOhm	1, 2, 3
Iin	Input Current	Vcc=3.6V, Vin=+5.5V Other Input = Gnd			0	+1.8	mA	1, 2, 3
		Vcc=3.6V, Vin=-0.5V Other Input = Gnd			0	-1.8	mA	1, 2, 3
		Vcc=0V, Vin=+5.5V Other Input = Gnd			0	+1.8	mA	1, 2, 3
		Vcc=0V, Vin=-0.5V Other Input = Gnd			0	-1.8	mA	1, 2, 3
Voh	Logical "1" Output Voltage	Vcc=3.0V, Vdiff=+1V, Iout=-6.0mA			2.4		V	1, 2, 3
Vol	Logical "0" Output Voltage	Vcc=3.0V, Vdiff=-1V, Iout=6.0mA				0.5	V	1, 2, 3
Vih	Minimum Enable High Level Voltage		1		2.0		V	1, 2, 3
Vil	Maximum Enable Low Level Voltage		1			0.8	V	1, 2, 3
Ioz	Maximum TRI-STATE Output Leakage Current	Vcc=3.6V, Vout=Vcc or Gnd Enable = Vil, $\overline{\text{ENABLE}}$ = Vih				+50	uA	1, 2, 3
Ien	Maximum Enable Input Current	Vcc=3.6V, Vin = Vcc or Gnd				± 1.0	uA	1, 2, 3
Icc	Quiescent Power Supply Current	Vcc=3.6V, No Load, En, $\overline{\text{En}}$ = Vcc or Gnd -0.5V<Vcm<+5.5V				20	mA	1, 2, 3
Ios	Output Short Circuit Current	Vcc=3.0V/3.6V, Vout=0V, Vdiff=+1V	2		-10	-70	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: PROPAGATION DELAY TIME:

(The following conditions apply to all the following parameters, unless otherwise specified.)
 AC: $V_{cc}=3.0/3.6V$, $C_1=50pF$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH	Input to Output Propagation Delay	$V_{cm}=1.5V$	3		6	45	nS	9, 10, 11
tPHL	Input to Output Propagation Delay	$V_{cm}=1.5V$	3		6	45	nS	9, 10, 11
tsk1	Skew $t_{pHLD}-t_{pLHD}$ (same channel)					6	nS	9, 10, 11
tsk2	Pin to Pin Skew (Same device)					6	nS	9, 10, 11
tPLZ	Output Disable Time	2K Ohms to V_{cc}	4			50	nS	9, 10, 11
tPZL	Output Enable Time	2K Ohms to V_{cc}	4			50	nS	9, 10, 11
tPHZ	Output Disable Time	2K Ohms to Gnd	4			50	nS	9, 10, 11
tPZH	Output Enable Time	2K Ohms to Gnd	4			50	nS	9, 10, 11

Note 1: Parameter tested go-no-go only.

Note 2: Short one output at a time to Gnd.

Note 3: Generator waveform is specified as follows: $f=1MHz$, duty cycle=50%, $Z_o=50$ Ohms, $t_r=t_f \leq 6ns$. Receiver inputs = 1V to 2V with measure points equal to 1.5V on the inputs to 1/2 V_{cc} on the output.

Note 4: Generator waveform is specified as follows: $f=1MHz$, duty cycle=50%, $Z_o=50$ Ohms, $t_r=t_f \leq 6ns$. EN/ \overline{EN} inputs = 0V to 3V with measure points equal to 1.5V on the inputs, to 1/2 V_{cc} on the outputs for ZL and ZH, and ($V_{ol}+0.3V$) for LZ, and ($V_{oh}-0.3V$) for HZ.

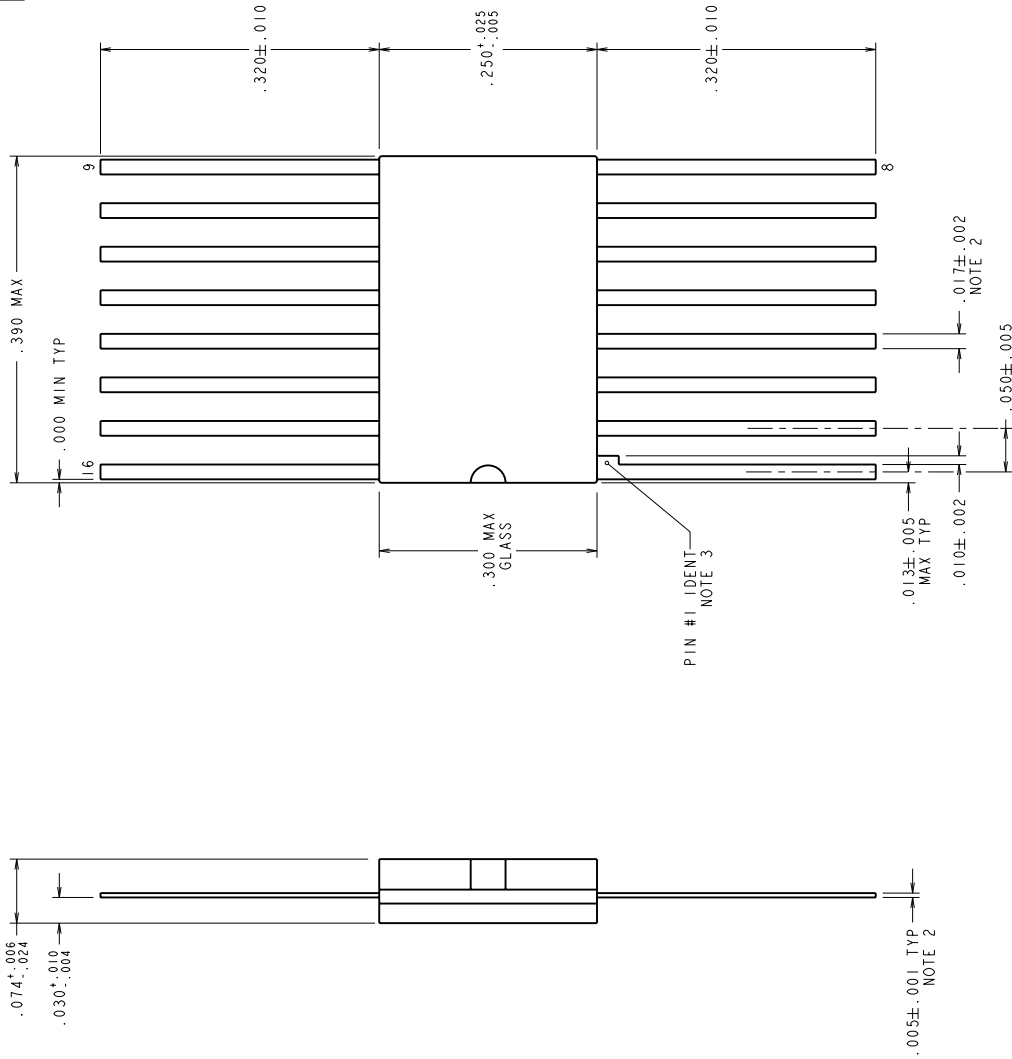
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
W16ARL	CERPACK (W), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
K	REVISE AND REDRAW PER NEW STANDARD.	10514	07/28/94	DEG/AEP
L	.017±.002 WAS .017±.020.	10656	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
 - a) A NOTCH OR OTHER MARK WITHIN THIS AREA
 - b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION M0-092, VARIATION AC, DATED 04/89.

MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN <i>D. F. Grady</i>	07/28/94
DFTG. CHK.	
EMER. CHK.	

PROJECTION	
	1/8" MIN

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W16A	L

DO NOT SCALE DRAWING SHEET 1 of 1

National Semiconductor
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CERPACK, 16 LEAD

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003117	02/11/99	Mike Fitzgerald	Initial MDS Release