National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC401A-X REV 0B0

Original Creation Date: 11/24/98
Last Update Date: 03/09/99
Last Major Revision Date: 11/24/98

FAST SETTLING, WIDEBAND HIGH-GAIN MONOLITHIC OP AMP

General Description

The CLC401 is a wideband, fast-settling operational amplifier designed for applications requiring a gain greater than ±7. Constructed using an advanced complementary bipolar process and a proprietary design, the CLC401 features dynamic performance far beyond that of typical high-speed monolithic operational amplifiers. For example, at a gain of +20 V/V, the -3dB bandwidth is 150MHz and the rise/fall time is only 2.5ns.

The wide bandwidth and linear phase (0.2 deviation from linear at 50MHz) and a very flat gain response makes the CLC401 ideal for many digital communication system applications. For example, demodulators need both DC coupling and high-frequency amplification - requirements that are ordinarily difficult to meet.

The very fast 10ns settling to 0.1% and the ability to drive capacitive loads lend themselves well to flash A/D applications. Systems employing D/A converters also benefit from the settling time and also by the fact that current-to-voltage transimpedance amplification is easily accomplished.

The CLC401 provides a quick, effective design solution. Its stable operation over the entire ±7 to ±50 gain range precludes the need for external compensation. And, unlike many other high-speed op amps, the CLC401's power dissipation of 150mW is compatible with designs which must limit total power dissipation or power supply requirements.

Industry Part Number

CLC401A

NS Part Numbers

CLC401AJ-MLS
CLC401AJ-QML

Prime Die

UB1364A

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- -3dB bandwidth of 150MHz
- 0.1% settling in 10ns
- Low power, 150mW
- Overload and short circuit protected
- Stable without compensation
- Recommended gain range ±7 to ±50
- CONTROLLING DOCUMENT:
  CLC401AJ-QML 5962-8997301PA

Applications

- Flash, precision A/D conversion
- Photodiode, CCD preamps
- IF processors
- High-speed modems, radios
- Line drivers
- DC-coupled log ampifiers
- High-speed communications

(Absolute Maximum Ratings)

(Note 1)

Supply Voltage (Vs)	±7V dc
Output Current (Iout)	±70mA
Maximum Power Dissipation (Pd) (Note 2)	1.2W
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C to +150 C
Lead Temperature (soldering, 10 seconds)	+300 C
Thermal Resistance	
Junction-to-ambient (ThetaJA)	
Ceramic DIP (Still Air)	134 C/W
(500 LFPM)	80 C/W
Junction-to-case (ThetaJC)	
Ceramic DIP	27 C/W
Package Weight (typical)	
Ceramic DIP	TBD
ESD Tolerance (Note 3)	
ESD Rating	1000 V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±5V dc
Gain Range	+7 to +40 and -1 to -40
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Open Loop Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vs = ±5V dc, and Av = +20. -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current noninverting				-20	+20	uA	1, 2
					-36	+36	uA	3
-Iin	Input Bias Current (Inverting)				-30	+30	uA	1
					-40	+40	uA	2
					-46	+46	uA	3
Tc (+Iin)	Average +Input Bias Current Drift		1		-200	+200	nA/C	1, 2, 3
Tc (-Iin)	Average -Input Bias Current Drift		1		-200	+200	nA/C	1, 2, 3
Vio	Input Offset Voltage				-6	+6	mV	1
					-11	+11	mV	2
					-10	+10	mV	3
Tc (Vio)	Average Offset Voltage Drift		1		-50	+50	uV/C	1, 2, 3
IS	Supply Current	No Load				±21	mA	1, 2, 3
PSRR	Power Supply Rejection Ratio	+VS = +4.5V to +5.0V -VS = -4.5V to -5.0V			50		dB	1, 2, 3
+RIN	Input Resistance		1		100		kOhm	1, 2
			1		50		kOhm	3
Rout	Output Impedance (DC)		1			0.3	Ohm	1, 2, 3
CIN	Input Capacitance	TA=+25C	1			2.5	pF	4
CMRR	Common Mode Rejection Ratio		1		50		dB	4, 5, 6
Vout	Output Voltage Swing	No Load			2.9		V	1, 2
					2.7		V	3

Electrical Characteristics

AC PARAMETERS: Closed Loop Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, Vs = ±5V dc, and Av = +20. -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small Signal Bandwidth	-3dB bandwidth, VOUT < 2 VPP			100		MHz	4
					70		MHz	5
					100		MHz	6
LSBW	Large Signal Bandwidth	-3dB bandwidth, VOUT < 4 VPP	1		65		MHz	4, 6
			1		55		MHz	5
GFPL	Gain Flatness Peaking	0.1 MHz to 25 MHz, VOUT < 2 VPP				0.1	dB	4
						0.1	dB	5, 6
GFPH	Gain Flatness Peaking	> 25 MHz, VOUT < 2 VPP				0.2	dB	4
						0.2	dB	5, 6
GFR	Gain Flatness Rolloff	0.1 MHz to 50 MHz, VOUT < 2 VPP				1.0	dB	4
						1.3	dB	5
						1.0	dB	6

AC PARAMETERS: Distortion

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, Vs = ±5V dc, and Av = +20. -55 C ≤ Ta ≤ +125 C (Note 3)

HD2	2nd Harmonic Distortion	2 VPP at 20 MHz				-35	dBc	4
						-35	dBc	5, 6
HD3	3rd Harmonic Distortion	2 VPP at 20 MHz				-50	dBc	4
						-45	dBc	5
						-50	dBc	6

AC PARAMETERS: Equivalent Input Noise

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, Vs = ±5V dc, and Av = +20. -55 C ≤ Ta ≤ +125 C (Note 3)

NF	Noise Floor	> 1.0 MHz	1, 2			-155	dBm	4, 6
			1, 2			-154	dBm	5
INV	Integrated Noise	1.0 MHz to 150 MHz	1, 2			50	uV	4, 6
			1, 2			55	uV	5

Electrical Characteristics

AC PARAMETERS: Time Domain Response

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, Vs = ±5V dc, and Av = +20. -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SR	Slew Rate	AV = +2, measured at ±1V at 6V step	1		800		V/uS	9, 11
		AV = +2, measured at ±1V at 6V step	1		700		V/uS	10
TRS	Rise Time	2V Step	1			3.5	nS	9, 11
			1			5.0	nS	10
TRL	Fall Time	5V Step	1			7.0	nS	9, 11
			1			8.0	nS	10
TSP	Settling Time to ±0.1%	2V Step at 0.1%	1			15	nS	9, 10, 11
OS	Overshoot	2V Step	1			10	%	9, 10, 11

DC PARAMETERS: DRIFT LIMITS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vs = ±5V dc, and Av = +20. "Deltas not required on B-level product. Deltas required for S-level (-MLS) product as specified on Internal Processing Instructions (IPI)." (Note 3)

+Iin	Input Bias Current (noninverting)				-2.0	2.0	uA	1
-Iin	Input Bias Current (inverting)				-3.0	3.0	uA	1
Vio	Input Offset Voltage				-1.0	1.0	mV	1
IS	Supply Current	No Load				2.0	mA	1

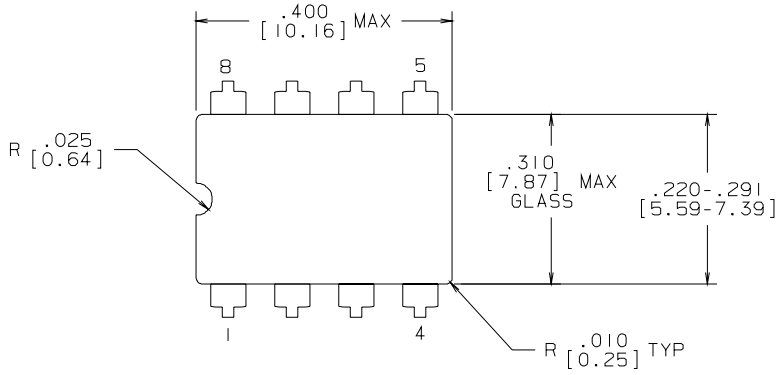
Note 1: If not tested, shall be guaranteed to the limits specified in Table 1
Note 2: Noise tests are performed from 5MHz to 200MHz.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.
Note 4: Group A testing only.

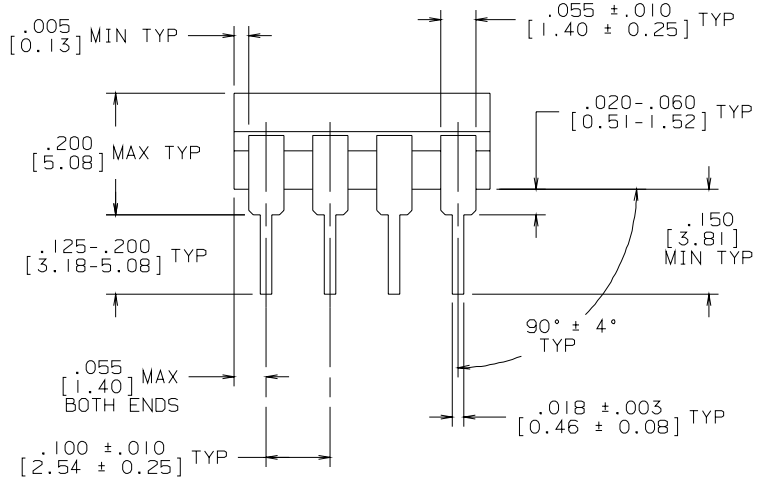
Graphics and Diagrams

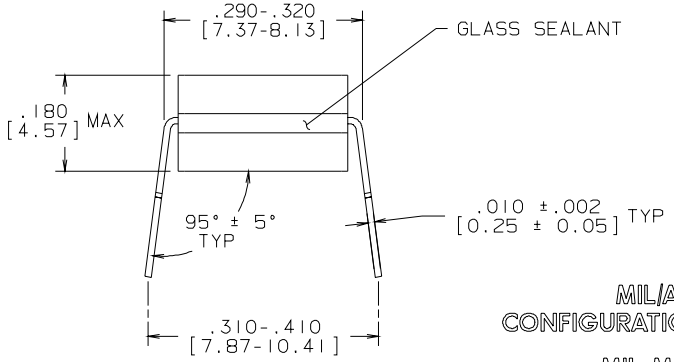
GRAPHICS#	DESCRIPTION
07081HRA3	CERDIP (J), 8 LEAD (B/I CKT)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000421A	CERDIP (J), 8 LEAD (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
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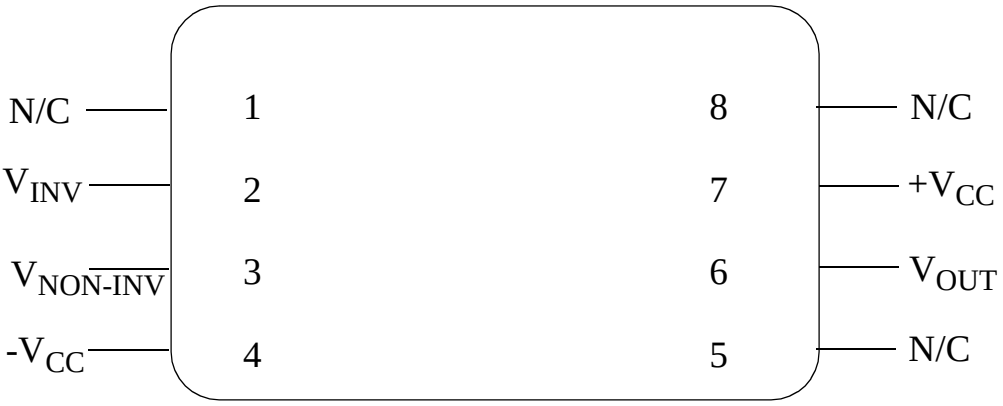
CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC401J

8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000421A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003170	03/09/99	Shaw Mead	Initial MDS Release
0B0	M0003271	03/09/99	Rose Malone	Update MDS: MNCLC401A-X, Rev. 0A0 to MNCLC401A-X, Rev. 0B0. Moved Reference to Controlling Document to Features Section. Added Reference to MIL-STD-883, Method 5004 and Method 5005 to Main Table, and limits to Thermal Resistance under Absolute Section.