OKI Semiconductor

This version: Sep. 1998

ML9070-02/03

DIRECT BUS CONNECTED CMOS REAL TIME CLOCK/CALENDAR

DESCRIPTION

The ML9070-02/03 is a silicon gate CMOS Real Time Clock/Calendar for use in direct bus-connection Microcontroller/Microprocessor applications. An on-chip 32.768 kHz crystal oscillator time base is divided to provide addressable 4-bit I/O data for SECONDS, MINUTES, HOURS, DAY OF WEEK, DATE, MONTH and YEAR. Data access is controlled by 4-bit address, chip selects ($\overline{CS}_0$, CS_1), $\overline{WRITE}$, $\overline{READ}$, and ALE. The ML9070-03 is not provided with the ALE pin. Control Registers D, E and F provide 30 SECOND error adjustment, INTERRUPT REQUEST (IRQ FLAG) and BUSY status bits, clock STOP, HOLD, and RESET FLAG bits, 4 selectable INTERRUPTS rates are available at the STD.P (STANDARD PULSE) output utilizing Control Register inputs T0, T1 and the INT/STND (INTERRUPT/STANDARD). Masking of the interrupt output (STD.P) can be accomplished via the MASK bit. The ML9070-02/03 can operate in a 12/24 hour format and Leap Year timing is automatic.
The interface supply voltage is 2.7 V to 5.5 V and the clock supply voltage during battery backup is 2.0 V to 5.5 V. A low current consumption has been realized.

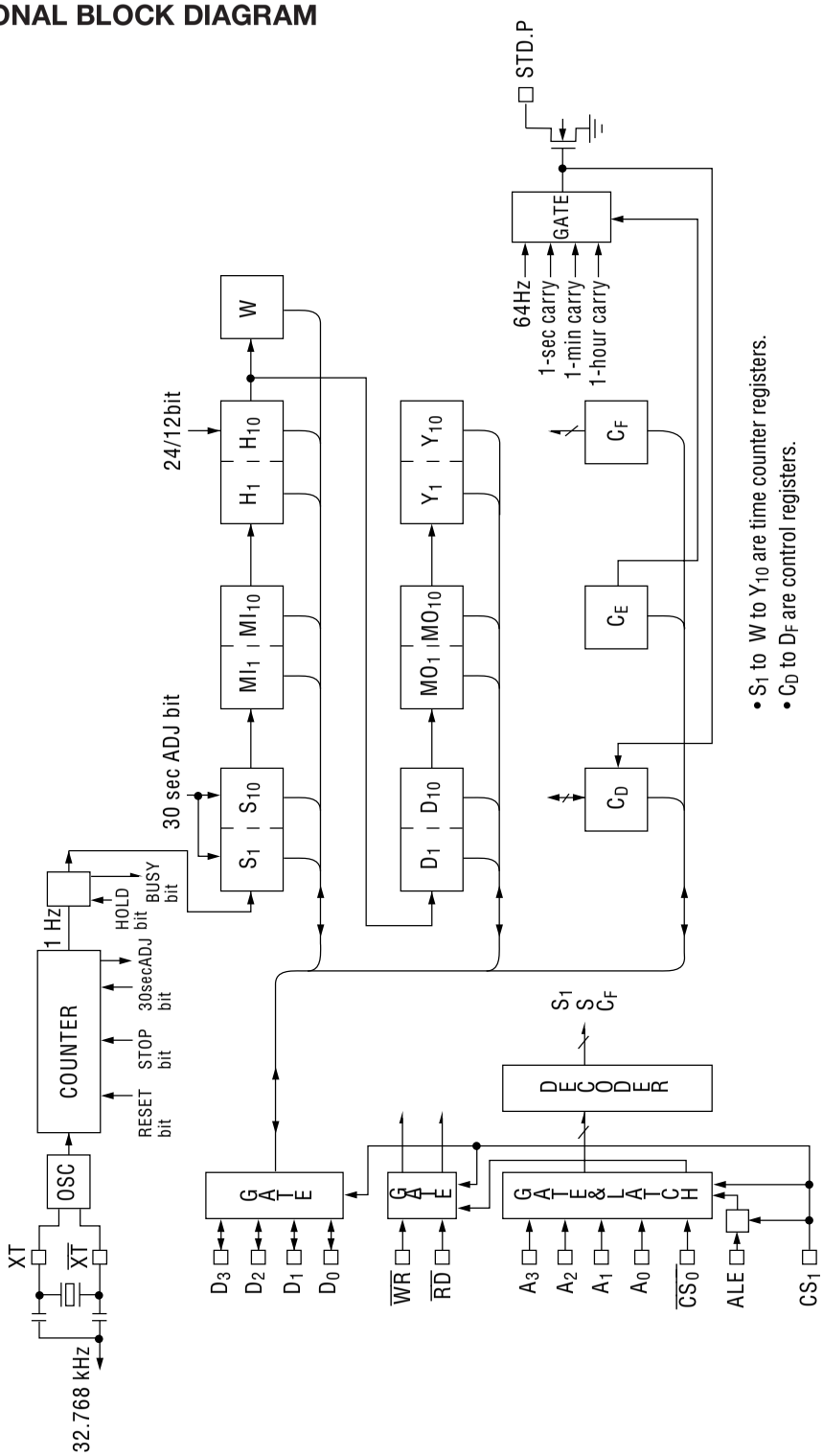
FEATURES

- Real time clock/calendar of SECONDS, MINUTES, HOURS, DAY OF WEEK, DATE, MONTH and YEAR
- 4-bit data bus
- 4-bit address bus
- $\overline{READ}$, $\overline{WRITE}$ ALE, and CHIP SELECT INPUTS
- Auto leap year
- ±30 second error correction by software
- Selectable interrupt outputs - 1/64 second, 1second, 1minute, 1hour
- Stop and restart of clock
- 12/24 hour format
- The ML9070-02 can input ALE from a microcontroller.
  (In case there is no ALE input from a microcontroller, fix ALE to "H" or use ML9070-03.)
- Wide range of interface power supply : 2.7 V to 5.5 V
- Wide range of clock power supply : 2.0 V to 5.5 V
- Low current consumption

ML9070-02
- 18-pin plastic DIP (DIP18-P-300-2.54)
- 24-pin plastic SOP (SOP24-P-430-1.27-K)

ML9070-03
- 16-pin plastic DIP (DIP16-P-300-2.54)
- 16-Pin plastic SOP (SOP16-P-300-1.27-K)

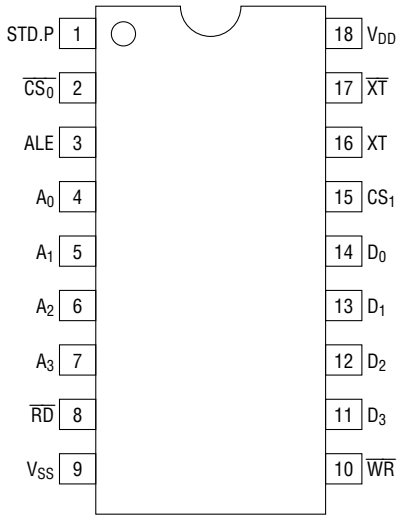
FUNCTIONAL BLOCK DIAGRAM



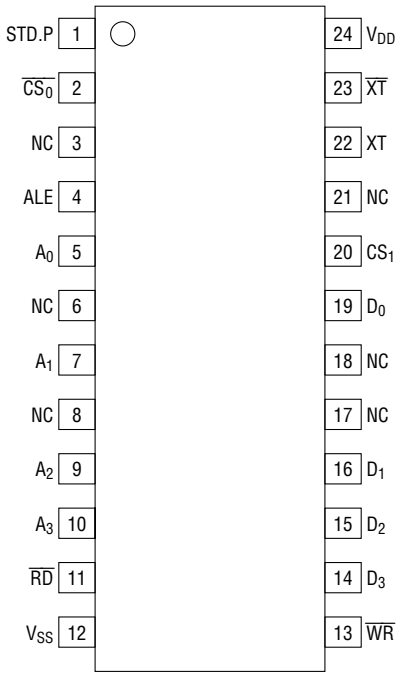
(Note) The ML9070-03 operates similarly as when $\overline{CS}_0$ is fixed to "L", and ALE to "H".

PIN CONFIGURATIONS

ML9070-02RA
(Top View) 18-Pin Plastic DIP



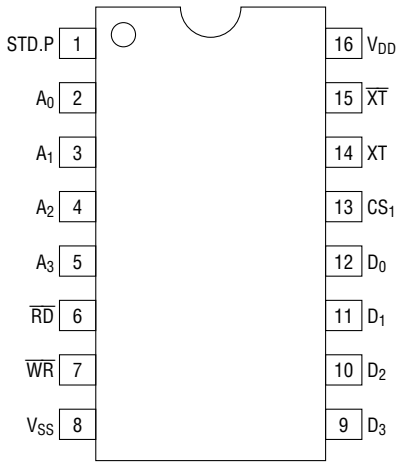
ML9070-02MA
(Top View) 24-Pin Plastic SOP



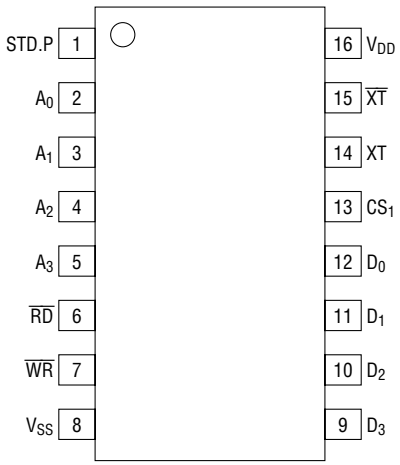
NC : NO CONNECTION (Unused pin)

Note) "M9070-02" is marked on actual devices.

ML9070-03RA
(Top View) 16-Pin Plastic DIP



ML9070-03MA
(Top View) 16-Pin Plastic SOP



Note) "M9070-03" is marked on actual devices.

PIN DESCRIPTION

- D_0 to D_3 (Data bus 0 to 3)
  Data bus Input/output pins to be directly connected to a microcontroller bus for reading and writing of the clock/calendar's registers and control registers.
  The interface is logically positive. When $\overline{CS_0}$ = "L", CS_1 = "H", $\overline{RD}$ = "L" and $\overline{WR}$ = "H", these pins are in the output mode. Otherwise these pins are in the high impedance state.
  The ML9070-03 has no $\overline{CS_0}$ pin and operates similarly as when $\overline{CS_0}$ is fixed to "L". In the ML9070-03, input/output of these pins are determined by the same settings as those in the ML9070-02 except setting of the $\overline{CS_0}$ pin.

- A_0 to A_3 (Address bus 0 to 3)
  Address input pin for use by a microcontroller to select internal clock/calendar's registers and control registers for Read/Write operations. Address input pins A_0 - A_3 are used in combination with ALE for addressing registers.

- ALE (Address Latch Enable)
  Address Latch Enable pin. This pin enables writing of address data when ALE = "H" and $\overline{CS_0}$ = "L" ; address data is latched when ALE = "L". Microcontroller having an ALE output should connect to this pin ; otherwise it should be connected at V_{DD}. CS_1 works independently of ALE. When a 4-bit microcontroller and other peripheral ICs share A_0 to A_3, ALE is also used to specify this IC. The ML9070-03 has no ALE pin and operates similarly as when ALE is fixed to "H".

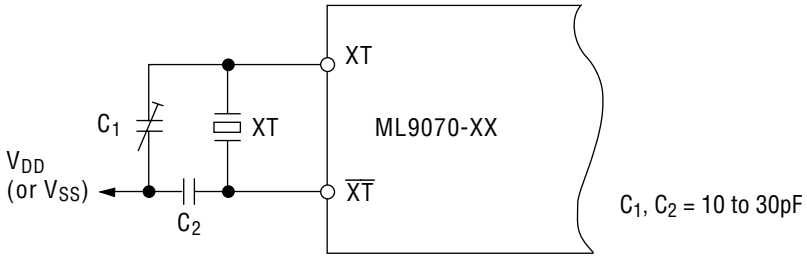
- $\overline{WR}$ (WRite)
  Writing of data is performed by this pin.
  When CS_1 = "H" and $\overline{CS_0}$ = "L", D_0 - D_3 data is written into the register specified by A_0 to A_3 and ALE at the rising edge of $\overline{WR}$.

- $\overline{RD}$ (ReaD)
  Reading of register data is accomplished using this pin. When CS_1 = "H", $\overline{CS_0}$ = "L" and $\overline{RD}$ = "L", the data of this register is output to D_0 - D_3.
  It is inhibited to set both $\overline{RD}$ and $\overline{WR}$ to "L" simultaneously because this setting causes a malfunction.

- $\overline{CS_0}$, CS_1 (Chip Select 0, 1)
  Chip Select pins. These pins enable or disable ALE, $\overline{RD}$ and $\overline{WR}$ operations. $\overline{CS_0}$ and ALE work in combination with one another.
  When $\overline{CS_0}$ = "L" and CS_1 = "H", ALE, $\overline{RD}$ and $\overline{WR}$ are enabled. Otherwise, the device is unconditionally equivalent to ALE = "L", $\overline{WR}$ = $\overline{RD}$ = "H".
  For details, refer to "CS_1 (Chip Select)" in "APPLICATION NOTE".
  The ML 9070-03 has no $\overline{CS_0}$ pin and operates similarly as when ALE is fixed to "H" and $\overline{CS_0}$ to "L".

- STD.P (STanDard Pulse)
  Output pin of N-CH OPEN DRAIN type. The output data is controlled by the D_1 data (INT/STD bit) content of C_E register. This pin has a priority to $\overline{CS_0}$ and CS_1.
  Refer to "C_E Register" in "FUNCTIONAL DESCRIPTION OF REGISTERS".

- XT, $\overline{XT}$ (X'Tal OSC)
  32.768kHz crystals are connected to these pins.
  The connection diagram is shown below.



  The impedance of the crystal should be less than 30kΩ.

  When an external clock is used, it is to be input to XT, while $\overline{XT}$ should be left open.
  The oscillation crystal and capacitors should be placed as close to the IC as possible.
  The oscillation circuit and other signal lines on any side of the substrate should be distant from each other.

- V_{DD}, V_{SS}
  Power supply pins. V_{DD} is used for positive supply and V_{SS} is for negative supply.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input Voltage	V_I		V_{SS}–0.3 to V_{DD}+0.3	
Output Voltage	V_O		V_{SS}–0.3 to V_{DD}+0.3	
Storage Temperature	T_{STG}	—	–55 to +150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	2.7 to 5.5	V
Clock Supply Voltage	V_{CLK}	—	2.0 to 5.5	V
Crystal Frequency	$f_{(XT)}$	—	32.768	kHz
Operating Temperature	T_{op}	—	–40 to +85	°C

(Note) The clock supply voltage assures crystal oscillation and clock.

DC CHARACTERISTICS

(V_{DD} = 2.7 to 5.5V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Terminal
"H" Input Voltage (1)	V_{IH1}	V_{DD} = 2.7 to 4.0 V	4/5V_{DD}	—	V_{DD}	V	All input terminals except CS_1,XT
		V_{DD} = 4.0 to 5.5 V	2.2	—	V_{DD}	V	
"L" Input Voltage (1)	V_{IL1}	V_{DD} = 2.7 to 4.0 V	V_{SS}	—	1/5V_{DD}	V	
		V_{DD} = 4.0 to 5.5 V	V_{SS}	—	0.8	V	
"H" Input Current (1)	I_{IH1}	V_I = V_{DD}	—	—	1	µA	Input terminals other than D_0 to D_3, XT
"L" Input Current (1)	I_{IL1}	V_I = 0 V	—	—	–1	µA	
"H" Input Voltage (2)	V_{IH2}	V_{DD} = 2.0 to 5.5 V	4/5V_{DD}	—	V_{DD}	V	CS_1
"L" Input Voltage (2)	V_{IL2}	V_{DD} = 2.0 to 5.5 V	V_{SS}	—	1/5V_{DD}	V	
"H" Input Current (2)	I_{IH2}	V_I = V_{DD}	—	—	10	µA	D_0 to D_3
"L" Input Current (2)	I_{IL2}	V_I = 0 V	—	—	–10	µA	
"L" Output Voltage (1)	V_{OL1}	I_O = 2.5 mA	—	—	0.4	V	D_0 to D_3
"H" Output Voltage	V_{OH}	I_O = –400 µA	2.4	—	—	V	
"L" Onput Voltage (2)	V_{OL2}	I_O = 2.5 mA	—	—	0.4	V	STD. P
OFF Leak Current	I_{OFF}	V_I = V_{DD} or 0 V, V_O = V_{DD}	—	—	10	µA	
Current Consumption (1)	I_{DD1}	$f_{(XT)}$ = 32.768 kHz, V_{DD} = 5 V	—	—	20	µA	V_{DD}
Current Consumption (2)	I_{DD2}	$V_{I(CS1)}$ = 0 V, V_{DD} = 2 V	—	—	5	µA	

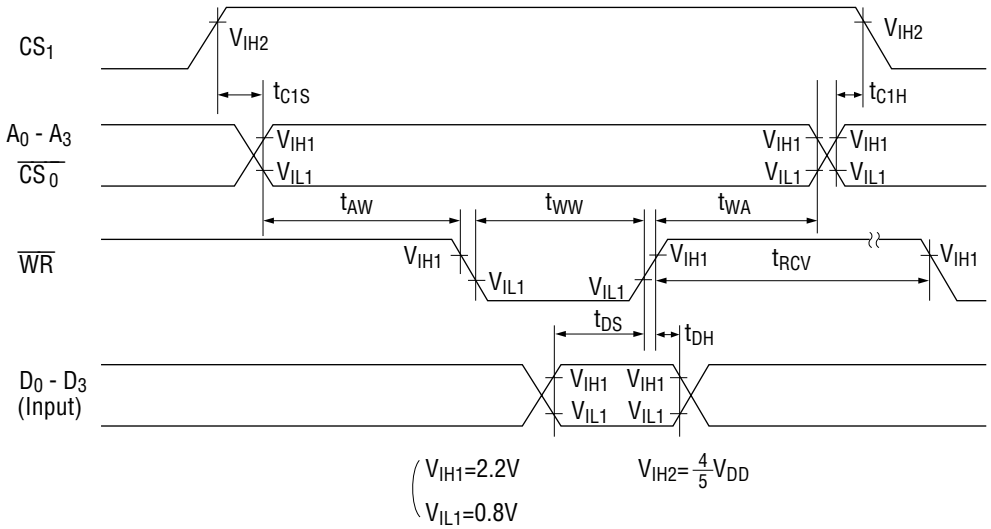
SWITCHING CHARACTERISTICS

● ML9070-02/03

• WRITE mode (ALE = "H")

(V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Setup Time	t_{C1S}	—	100	—	ns
CS_1 Hold Time	t_{C1H}	—	100	—	
Address Stable Before WRITE	t_{AW}	—	20	—	
Address Stable After WRITE	t_{WA}	—	10	—	
$\overline{WR}$ Pulse Width	t_{WW}	—	120	—	
Data Setup Time	t_{DS}	—	100	—	
Data Hold Time	t_{DH}	—	10	—	
$\overline{RD}$ / $\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	



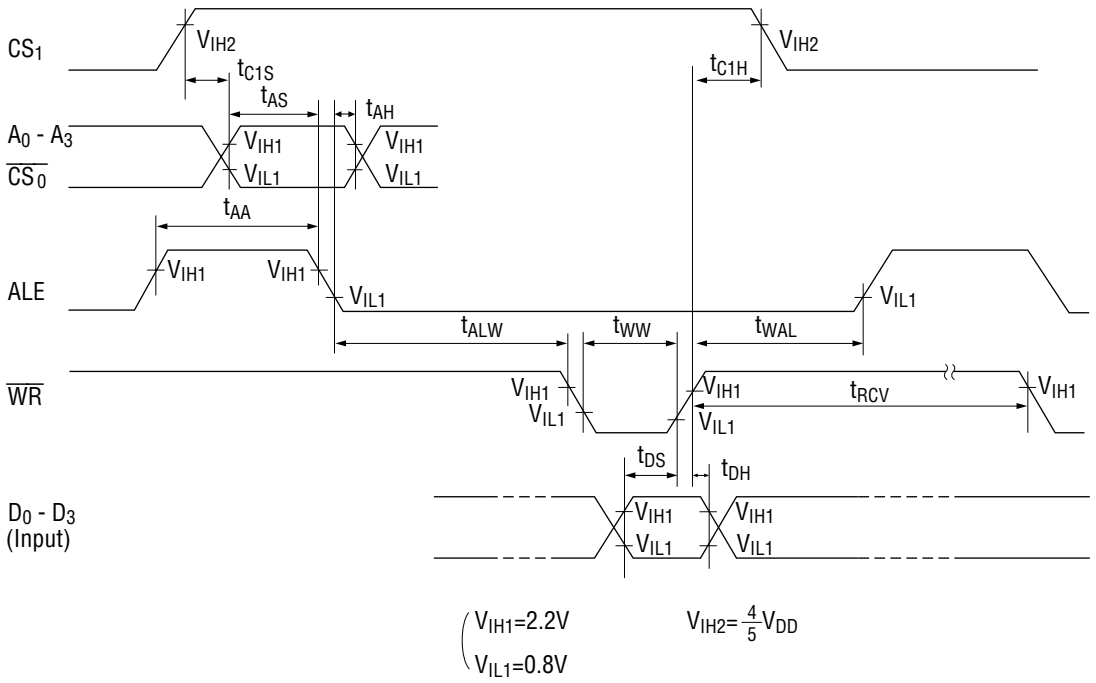
(Note) The ML9070-03 has no $\overline{CS_0}$ input.

● ML9070-02

• WRITE mode (with use of ALE)

(V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Setup Time	t_{C1S}	—	100	—	ns
Address Setup Time	t_{AS}	—	25	—	
Address Hold Time	t_{AH}	—	25	—	
ALE Pulse Width	t_{AA}	—	40	—	
ALE Before WRITE	t_{ALW}	—	10	—	
WRITE Pulse Width	t_{WW}	—	120	—	
ALE After WRITE	t_{WAL}	—	20	—	
DATA Setup Time	t_{DS}	—	100	—	
DATA Hold Time	t_{DH}	—	10	—	
CS_1 Hold Time	t_{C1H}	—	100	—	
$\overline{RD}$ / $\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	

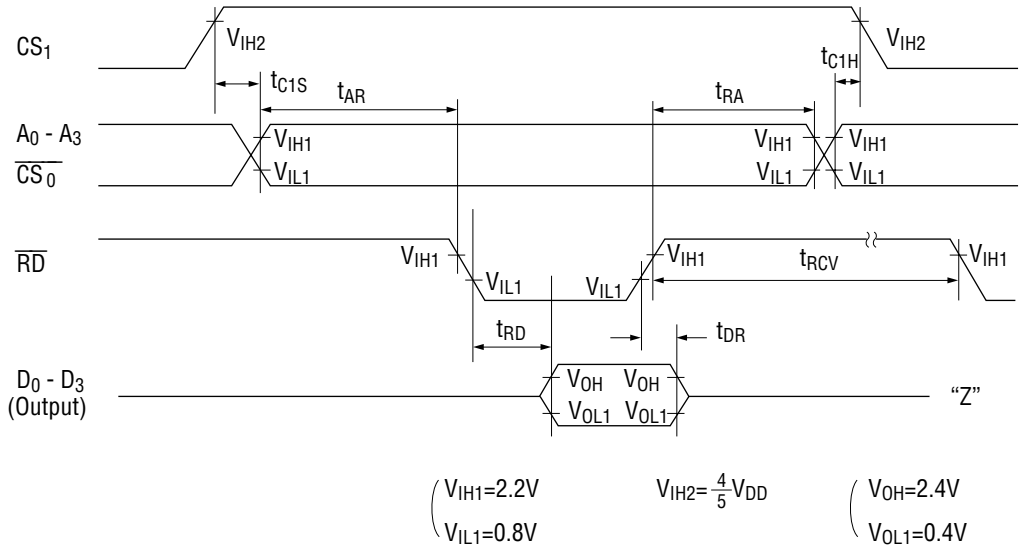


● ML9070-02/03

• READ mode (ALE = "H")

(V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Setup Time	t_{C1S}	—	100	—	ns
CS_1 Hold Time	t_{C1H}	—	100	—	
Address Stable Before READ	t_{AR}	—	–10	—	
Address Stable After READ	t_{RA}	—	0	—	
$\overline{RD}$ to Data	t_{RD}	C_L = 150pF	—	120	
Data Hold	t_{DR}	—	0	—	
$\overline{RD}$ / $\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	



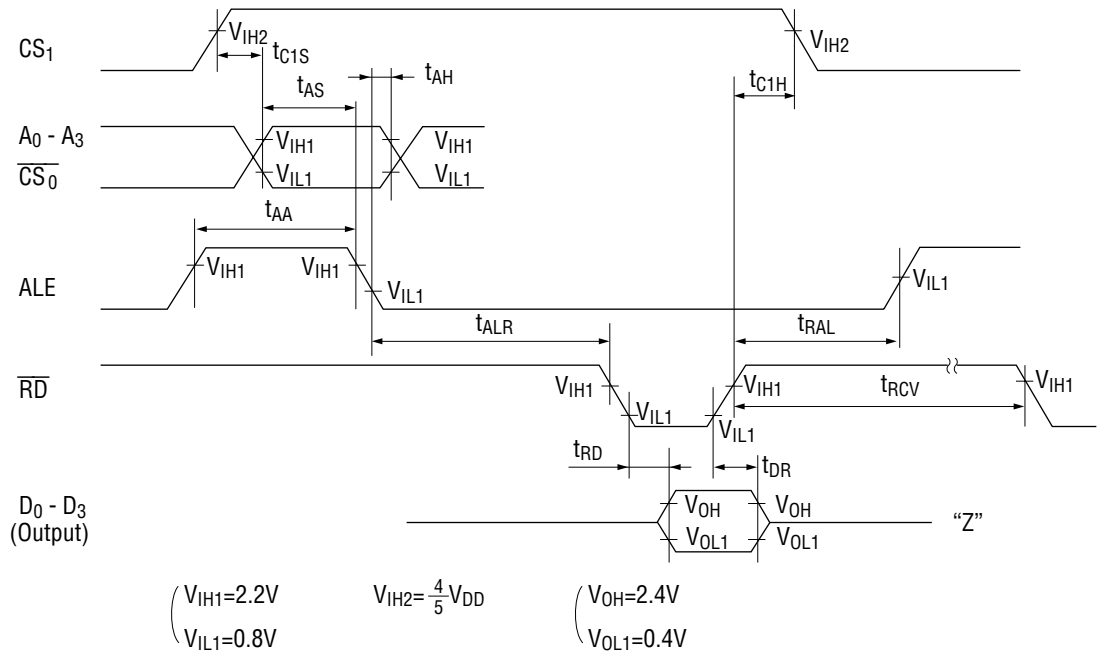
(Note) The ML9070-03 has no $\overline{CS_0}$ input.

● ML9070-02

• READ mode (with use of ALE)

(V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Setup Time	t_{C1S}	—	100	—	ns
Address Setup Time	t_{AS}	—	25	—	
Address Hold Time	t_{AH}	—	25	—	
ALE Pulse Width	t_{AA}	—	40	—	
ALE Before READ	t_{ALR}	—	10	—	
ALE After READ	t_{RAL}	—	10	—	
$\overline{RD}$ to Data	t_{RD}	C_L = 150pF	—	120	
DATA Hold	t_{DR}	—	0	—	
CS_1 Hold Time	t_{C1H}	—	100	—	
$\overline{RD}$ / $\overline{WR}$ Recovery Time	t_{RCV}	—	60	—	



V_{IH1}=2.2V, V_{IL1}=0.8V　　$V_{IH2}=\frac{4}{5}V_{DD}$　　V_{OH}=2.4V, V_{OL1}=0.4V

REGISTER TABLE

Address Input	Address Input				Register Name	Data				Count value	Description
	A_3	A_2	A_1	A_0		D_3 (MSB)	D_2	D_1	D_0 (LSB)		
0	0	0	0	0	S_1	s_8	s_4	s_2	s_1	0 to 9	1-second digit register
1	0	0	0	1	S_{10}	f_0	s_{40}	s_{20}	s_{10}	0 to 5	10-second digit register
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	0 to 9	1-minute digit register
3	0	0	1	1	MI_{10}	*	mi_{40}	mi_{20}	mi_{10}	0 to 5	10-minute digit register
4	0	1	0	0	H_1	h_8	h_4	h_2	h_1	0 to 9	1-hour digit register
5	0	1	0	1	H_{10}	*	PM/AM	h_{20}	h_{10}	0 to 2 or 0 to 1	PM/AM, 10-hour digit register
6	0	1	1	0	D_1	d_8	d_4	d_2	d_1	0 to 9	1-day digit register
7	0	1	1	1	D_{10}	*	*	d_{20}	d_{10}	0 to 3	10-day digit register
8	1	0	0	0	MO_1	mo_8	mo_4	mo_2	mo_1	0 to 9	1-month digit register
9	1	0	0	1	MO_{10}	*	*	*	mo_{10}	0 to 1	10-month digit register
A	1	0	1	0	Y_1	y_8	y_4	y_2	y_1	0 to 9	1-year digit register
B	1	0	1	1	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	0 to 9	10-year digit register
C	1	1	0	0	W	*	w_4	w_2	w_1	0 to 6	Week register
D	1	1	0	1	C_D	30 sec. ADJ	IRQ-F	BUSY	HOLD	—	Control Register D
E	1	1	1	0	C_E	t_1	t_0	INT /STND	MASK	—	Control Register E
F	1	1	1	1	C_F	TEST	24/12	STOP	REST	—	Control Register F

REST = RESET
INT/STND = INTERRUPT/STANDARD

Note 1) — Bit* does not exist (unrecognized during a write and held at "0" during a read).
Note 2) — Be sure to mask the AM/PM bit when processing 10's of hour's data.
Note 3) — BUSY bit is read only. The IRQ-F bit can only be set to a "0". Setting the IRQ-F to a "1" is done by hardware.
Note 4) — PM at 1 and AM at 0 for PM/AM bit.
Note 5) — "1" or "0" may be written to bit *.
Note 6) — The bit fo (OSC FLAG) memorizes that oscillation stops.
This bit is used to monitor the battery.
This bit is cleared by writing a "0". A "1" cannot be written into this bit.

FUNCTIONAL DESCRIPTION OF REGISTERS

S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, D_1, D_{10}, MO_1, MO_{10}, Y_1, Y_{10},W

a) These are abbreviations for SECOND1, SECOND10, MINUTE1, MINUTE10, HOUR1, HOUR10, DAY1, DAY10, MONTH1, MONTH10, YEAR1, YEAR10, and WEEK. These values are in BCD notation.
b) All registers are logically positive. For example, (s_8, s_4, s_2, s_1) = 1001 which means 9 seconds.
c) "1" or "0" may be written to bit* in the Register Table. The bit* automatically reads "0".
d) If data is written which is out of the clock register data limits, it can result in erroneous clock data being read back.

- PM/AM, h_{20}, h_{10}
  a) In 12-hour mode
     The existent time is AM12 : 00 through AM11 : 00 and PM12 : 00 through PM11 : 00.
     It is impossble to write data into the h_{20}, bit which is fixed to "0" unconditionally. The h_{20} bit is not set by clocking.
  b) In 24-hour mode
     The existent time is 0 : 00 clock through 23 : 00 clock.
     The PM/AM bit written is ignored and read out as "0" unconditionally.

- Y_1, Y_{10}, and leap year
  The ML9070 automatically recognizes leap years in either Christian Era calendar or Heisei Era (Japanese) calendar.
  80, 84, 88... Leap year
  When invalid month and day values are set (for instance, February 29, 1983 or November 31), the month and day values will be carried to the next month and day values when the carry pulse to the day digit is generated (for instance, the above dates become March 1, 1983 and December 1).
  The ML9070 recognizes a year whose last two digits can be divided evenly by 4 as leap year. Therefore, year 2100, which does not include a leap day, is excluded from automatic leap year correction. Year 2000 will be corrected automatically since the year contains a leap day. The user must check whether the year is year 2000 or 2100 when Y_{10}, Y_1 = "0, 0".

The Register W data limits are 0 - 6 (The table below shows a possible bit data definition).

W_4	W_2	W_1	Day of Week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

f_0 Flag
The f_0 flag bit memorizes that oscillation stops and is used to monitor the output of the battery. The "1" of this bit indicates stop of oscillation. This bit is cleared by writing "0". It is not permitted to write "1" into this bit.
"0" cannot be written in this bit during stop of oscillation.

C_D REGISTER (Control D Register)

- 30-sec ADJ (D_3) (30-second adjustment bit)
  When a "1" is written to this bit, if the second digits are smaller than 30, the second digits are reset to 00, and if it is larger than 30, the second digits are reset to 00 and a carry into the minute digit is executed. Data cannot be written into the S_1 - W registers and a "1" can not be written into the REST bit of the C_F register 125µs after writing into this bit because internal processing is being executed. This bit holds "1" 125µs after writing, and returns to "0" automatically. Therefore, data should be written into the S_1 - W registers after checking that this bit has returned to "0".

- IRQ-F (D_2) (Interrupt ReQuest Flag)
  This status bit corresponds to the output level of the STD.P output. When STD.P = "L", then IRQ-F = "1", when STD.P = high impedance, then IRQ-F = "0". The IRQ-F indicates that an interrupt has occurred in the microcomputer if IRQ-F = "1". When D_0 of register C_E (MASK) = "0", then the STD.P output changes from high impedance to "L" and IRQ-F changes from "0" to "1" according to the timing set by D_3 (t_1) and D_2 (t_0) of register C_E. When D_1 of register C_E (INT/STND) = "1" (interrupt mode), the STD.P output remains "L" until the IRQ-F is written to a "0". When IRQ-F = "1" and timing for a new interrupt occurs, the new interrupt is ignored. When D_1 (INT/STND) = "0" (Standard Pulse Output mode) the STD.P output remains "L" until either "0" is written to the IRQ-F or the IRQ-F automatically goes to "0" after 7.8125ms.

- BUSY (D_1)
  Internal status bit that indicates whether interface with a microcontroller is enabled or disabled. To write data in registers S_1 to W (addresses 0 to C), the HOLD bit must be set to "1" and the BUSY bit must be set to "0". To read data, the BUSY bit must be set to "0" when the HOLD bit is used. The BUSY bit is kept to "0" while the HOLD bit is "1". When the HOLD bit is set to "0", the BUSY bit is set to "1". The IRQ-F of register C_D, C_E and C_F operations can be performed regardless of the settings of the HOLD bit and the BUSY bit.
  When the HOLD bit is set to "0", the BUSY bit is set to "1" unconditionally and BUSY/non-BUSY can be checked by writing "1" to the HOLD bit. When BUSY = "1" (BUSY status) is read, check BUSY = "0" as follows :
  Repeat the BUSY checking routine by writing "0" and then "1" to the HOLD bit (HOLD ← 0, HOLD ← 1, BUSY check) or write "1" to the HOLD bit again 190 micro seconds after writing "0" to the HOLD bit.
  The BUSY status lasts 190 micro seconds per one second.
  Data cannot be written to the BUSY bit.

- HOLD (D_0)
  Bit used for reading and writing registers S_1 to W (addresses 0 to C), When "1" is written to this bit and the BUSY bit is "0", the clock of one second digit or more is stopped, enabling Read/Write operations. When BUSY is "1" or Read/Write is completed, "0" is written to the HOLD bit. If the writing of "0" is omitted, data may be corrupted.
  By setting this bit to "1", the carry of one-second digit is prohibited inside the IC. However, the carry to the second digit that was generated during the "1" interval will be corrected automatically (+1 second) once only when "0" is written to this bit. However, next and subsequent carry will be ignored and data will not be corrected. (Loss of second) .
  When CS_1 is set to "L", the HOLD bit will become "0" like that "0" is written to the HOLD bit.

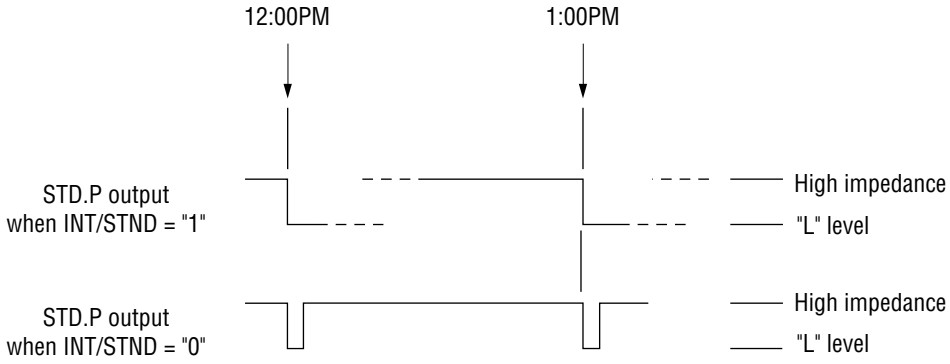
C_E REGISTER (Control E Register)

- t_1 (D_3), T_0 (D_2) (Time 0, 1)
  INT/STND bit = "1" : Setting of interrupt period
  INT/STND bit = "0" : Setting of periodic waveform

t_1	t_0	Period
0	0	1-64 second
0	1	1 second
1	0	1 minute
1	1	1 hour

The duration that the periodic waveform output is at "L" level is about 7.8125ms.
t_1 and t_0 determine the output timing of the STD.P output.

e.g.) When t_1 = "1", t_0 = "1", MASK = "0"



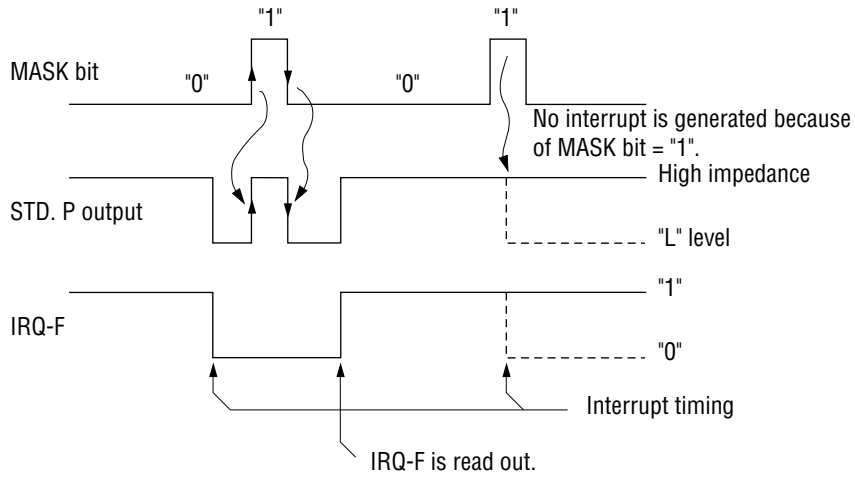
When a "1" is written to the 30-sec ADJ bit, a carry can occur.
Therfore, if (t_1, t_0) = (1, 0), (1, 1), the STD.P output may sometime be at "L" level. When INT/STND = "0", this "L" level is kept for a maximum of 9.8ms after under-second digits in 30-sec ADJ is cleared (the 30-sec ADJ flag returns to "0").
If the selected interrupt period is 1 second, 1 minute, or 1 hour, a carry occurs during the time the S_1, S_{10}, MI_1, MI_{10} registers are overwritten using the HOLD bit, and data written in these registers determines the interrupt timing set by the carry, the STD.P output will go to "L" level after HOLD = "0". (IRQ-F will is set to "1")

In other cases, writing to the S_1, S_{10}, MI_1, MI_{10}, H_1 registers do not change the STD.P output.

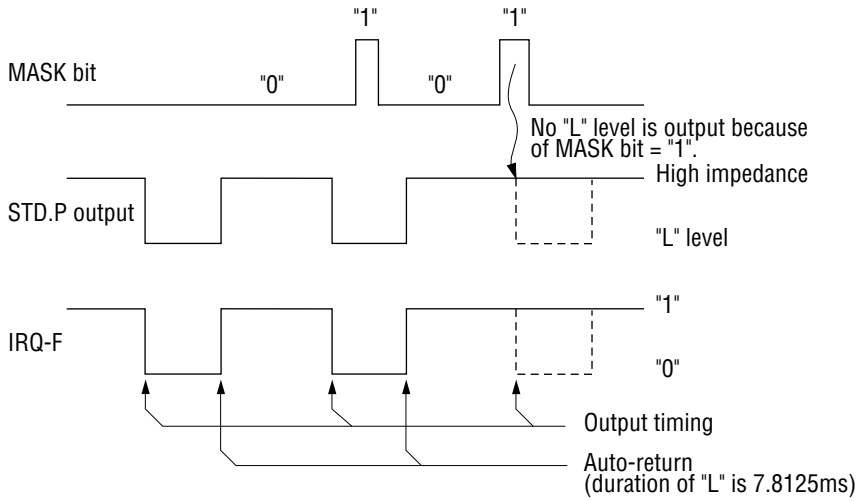
- INT/STND (D_1) (interrupt-to-Standard waveform switching bit)
  INT/STND = "1" : "1" of the IRQ-F bit and "L" level on the STD.P output are kept until IRQ-F (C_D register) is read out.
  INT/STND = "0" : "1" of the IRQ-F bit returns to "0" after a certain time elapses (after about 7.8ms) or when IRQ-F is read out.
  "L" level on the STD.P output returns to high impedance after a certain time elapses.

- MASK (D_0)
  "1" of the MASK bit inhibits the setting of "1" to the IRQ-F flag and sets the STD.P output to the high impedance state.

  Interrupt mode (INT/STND = "1")



  Periodic timing waveform output mode (INT/STND = "0")



  When the IRQ-F bit is read out before auto-return, the IRQ-F bit goes to "0", and the STD.P output keeps "L" level for 7.8125 ms, then goes into the high impedance state.

C_F REGISTER (Control F Register)

- TEST (D_3)
  The TEST bit is used for testing by OKI and should be set to "0".

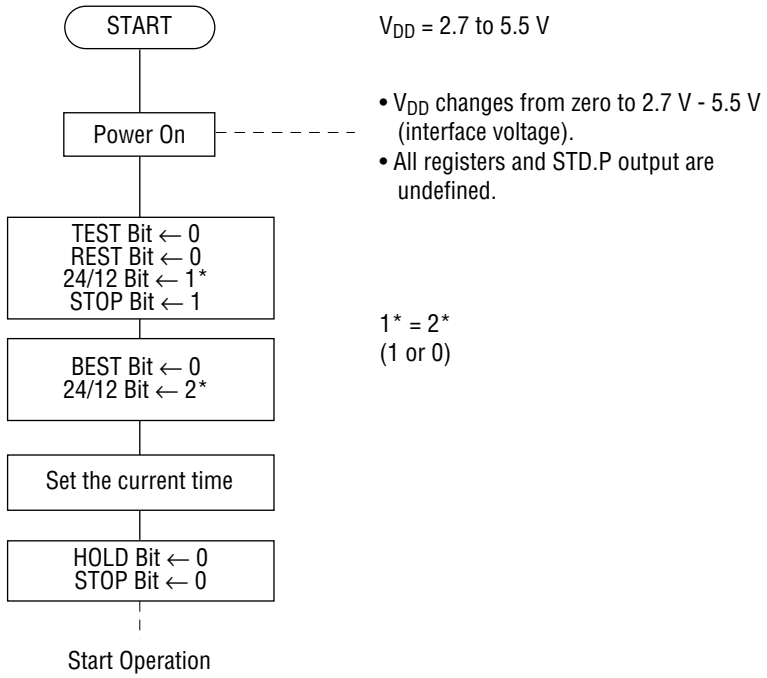
- 24/12 (D_2) (24/12 hour format)
  This bit is used to switch between 24-hour format and 12-hour format.
  24/12 = "1" : 24-hour format without PM/AM
  24/12 = "0" : 12-hour format with PM/AM
  When the 24/12 bit is changed, data in the H_1 - W registers may become undefined. Therefore, it is required to set those registers again.

- STOP (D_1)
  "1" of this bit stops clocking and "0" restarts clocking.

- REST (D_0)
  "1" of this bit clears under-second-time to zero and at the same time stops clocking. "0" of this bit restarts clocking.
  When CS_1 is set to "L", this bet goes to "0" automatically.

APPLICATION NOTE

Power Supply



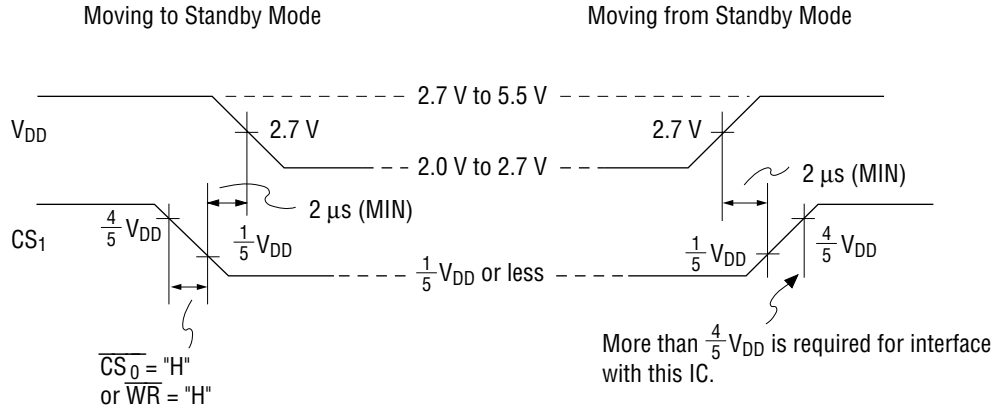
CS_1 (Chip Select)

V_{IH} and V_{IL} of CS_1 has 3 functions.

a) To accomplish the interface with a microcontroller/microprocessor.
b) To inhibit the control bus, data bus and address bus and to reduce input gate pass current in the stand-by mode.
c) To protect internal data when the mode is moved to and from standby mode.

To realize the above functions:

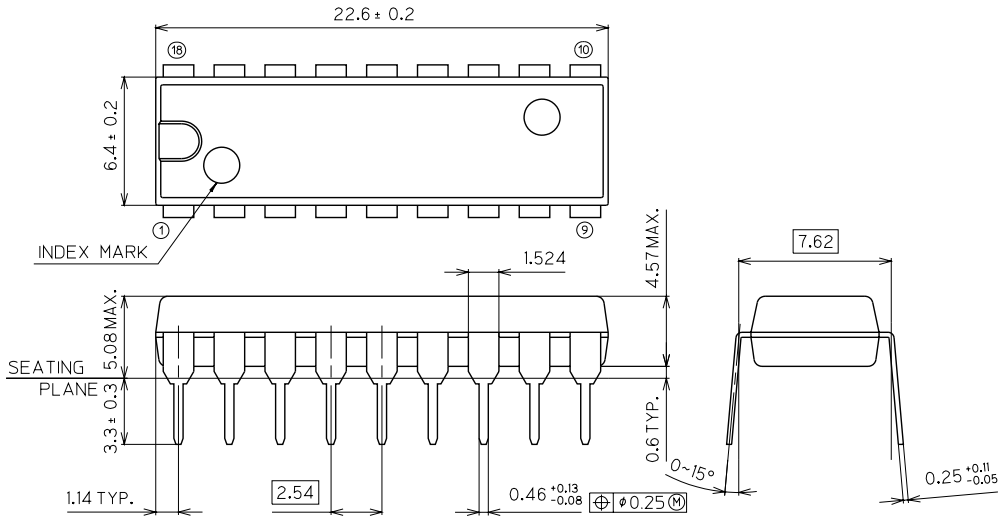
a) More than $\frac{4}{5}$ V_{DD} should be applied to the ML9070 for the interface with a microcontroller/microprocessor.
b) In moving to the standby mode, lessthan $\frac{1}{5}$ V_{DD} should be applied so that all data buses should be disabled. In the standby mode, approx. 0V should be applied.
c) When moving to and from the standby mode, obey the following timing chart.



PACKAGE DIMENSIONS

(Unit : mm)

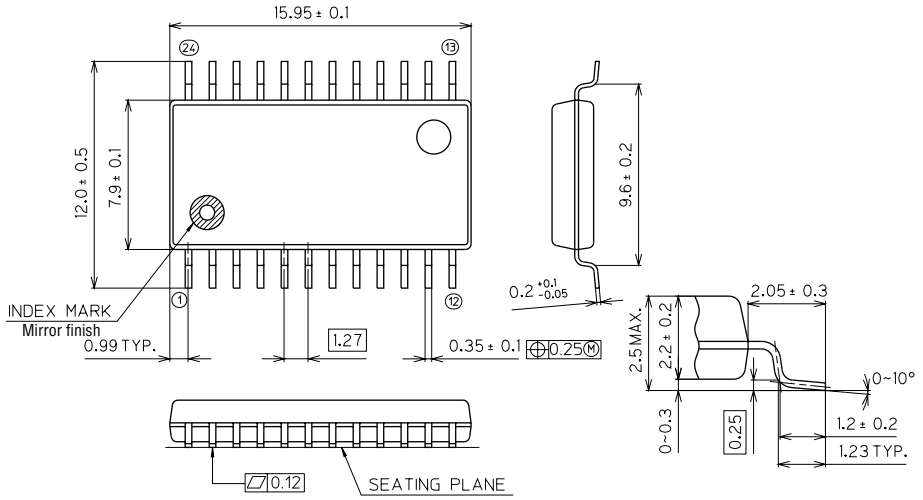
DIP18-P-300-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.30 TYP.

(Unit : mm)

SOP24-P-430-1.27-K



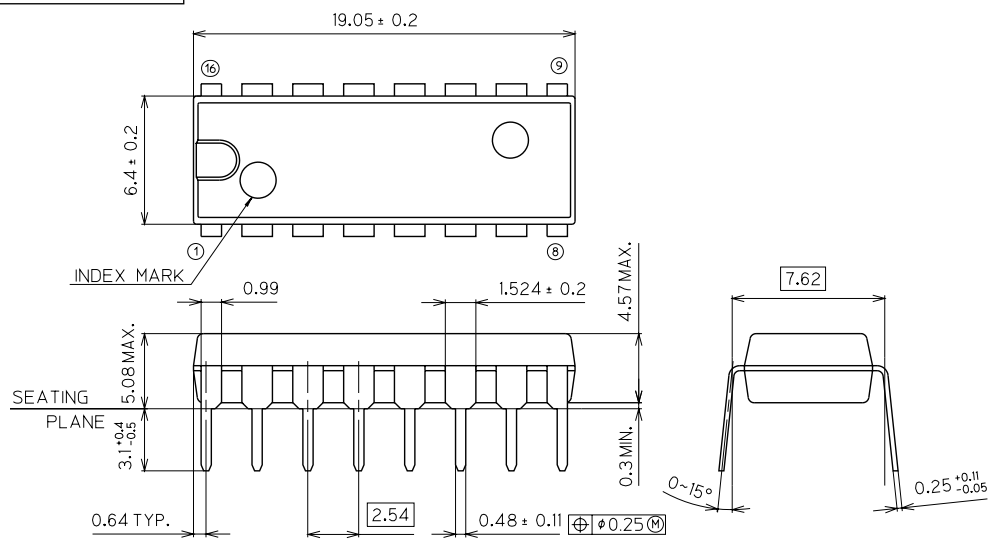
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

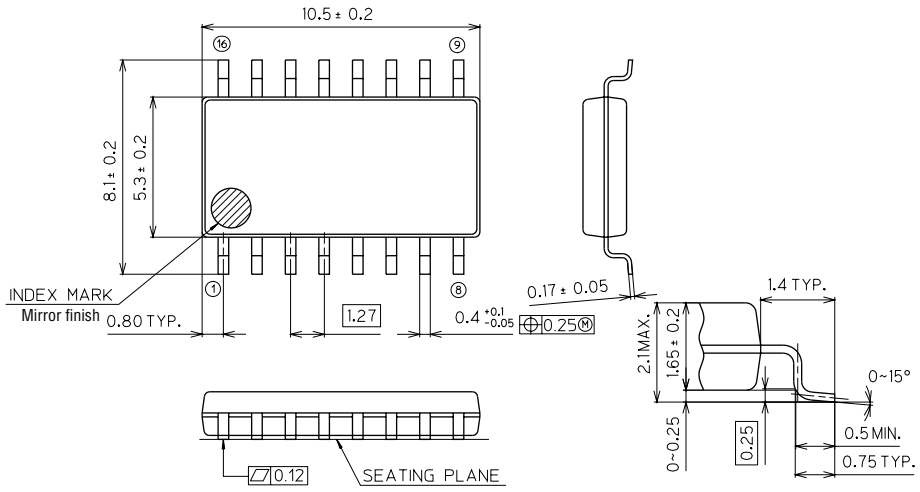
DIP16-P-300-2.54



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.99 TYP.

(Unit : mm)

SOP16-P-300-1.27-K



Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.21 TYP.

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