ML7019

Preliminary

SINGLE RAIL DUAL CHANNEL CODEC

❖ General Description

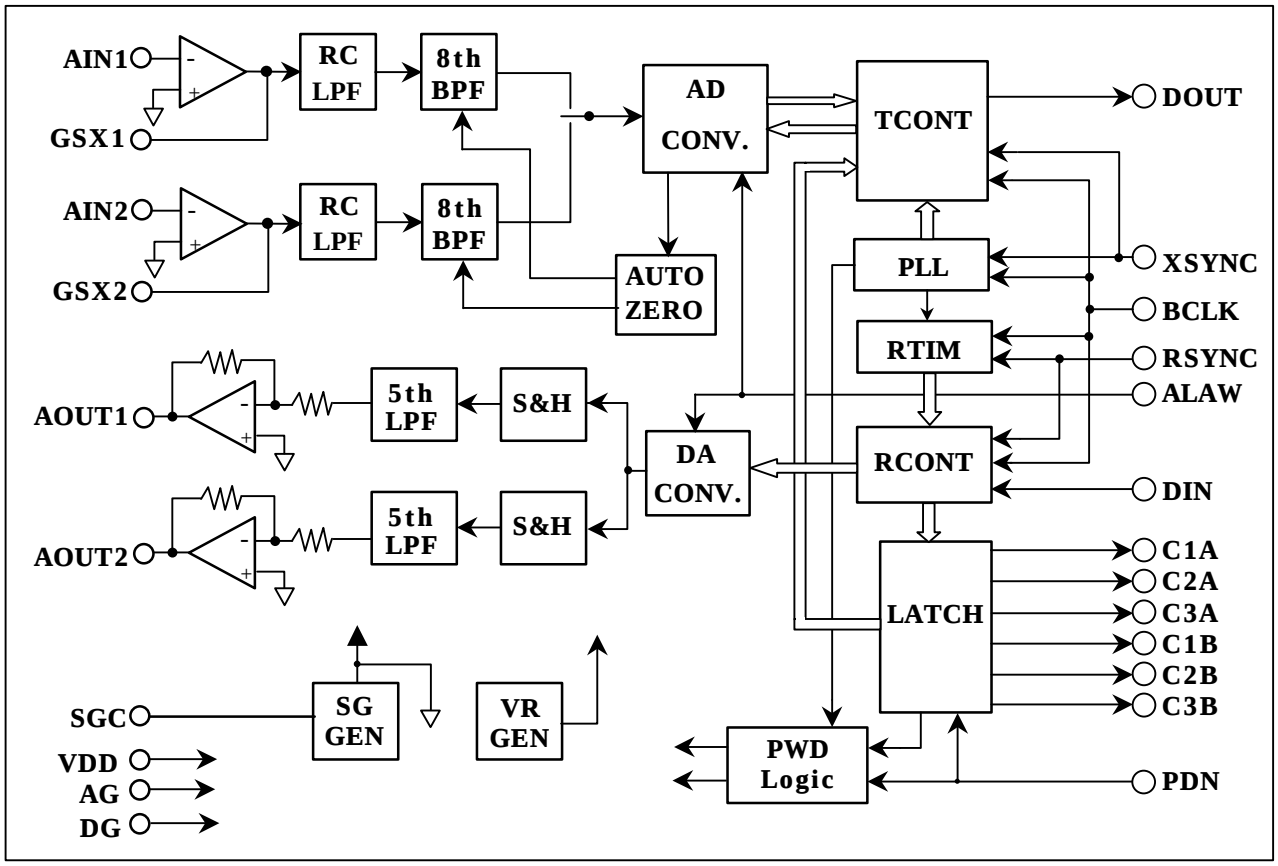
The ML7019 is a two-channel single-rail CODEC CMOS IC for voice signals ranging from 300 to 3400Hz.This device contains two-channel analog-to-digital (A/D) and digital-to-analog (D/A) converters on a single chip. The ML7019 is designed especially for a single power supply and low power applications and achieves a reduced footprint.

The ML7019 is best suited for line card applications with easy interface to subscriber line interface circuits (SLICs). The SLIC interface latches are embedded onto this CODEC, thus eliminating the need for external components and optimizing board space.

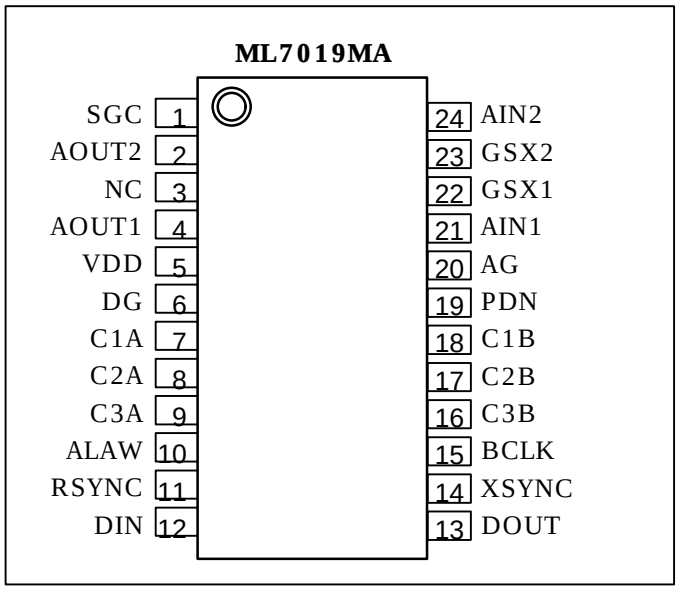
❖ Features

- Single 5-V power supply Operation
- Low power consumption
  - operating mode: typical: 35mW max.: 74mW
  - power save mode: typical: 7.0mW max.: 16mW
  - power down mode: typical: 0.05mW max.: 0.3mW
- ITU-T Companding law
  - μ-law / A-law pin selectable
- Built-in phase-locked loop(PLL) eliminates master clock
- Built-in dual 3-bit latches with CMOS drive capability
- Serial PCM interface
- Transmission clocks:
  - 256 / 384 / 512 / 768 / 1024 / 1536 / 1544 / 2048 / 4096Kbps
- Adjustable Transmit gain
- Built-in reference voltage supply
- Analog output can directly drive a 600Ω line transformer
- Latched content echo-back function
- Packaging:24SOP

❖ FUNCTIONAL BLOCK DIAGRAM



❖ PIN ASSIGNMENT



❖ PIN DESCRIPTION

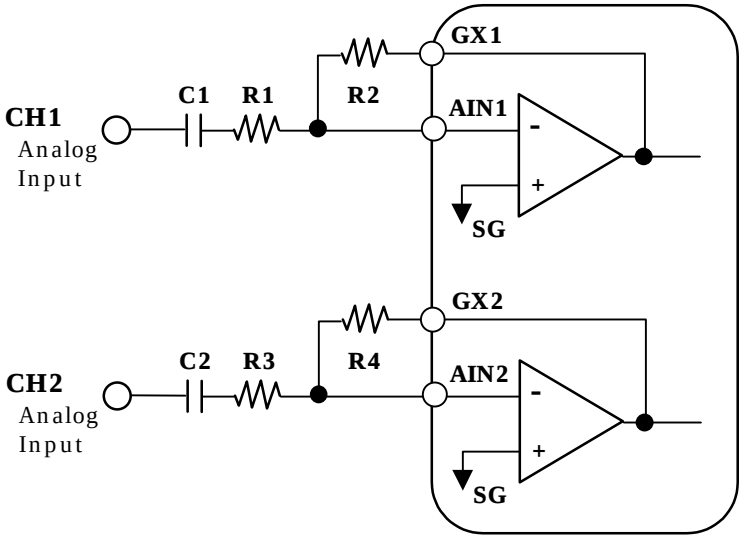
AIN1, AIN2, GSX1, GSX2

AIN1 and AIN2 are the transmit analog inputs for channels 1 and 2.

GSX1 and GSX2 are the transmit level adjustments for channels 1 and 2.

AIN1 and AIN2 are inverting inputs for the op-amp; GSX1 and GSX2 are connected to the output of the op-amp and are used to adjust the level, as shown below.

When not using AIN1 and AIN2, connect AIN1 to GSX1 and AIN2 to GSX2. During power saving and power down mode, the GSX1 and GSX2 outputs are at AG voltage.



CH1 Gain

Gain = R2/R1 ≤ 10
R1: Variable
R2 > 20KΩ
C1 > 1/ (2×3.14×30×R1)

CH2 Gain

Gain = R4/R3 ≤ 10
R3: Variable
R4 > 20KΩ
C2 > 1/ (2×3.14×30×R3)

AOUT1, AOUT2

AOUT1 is the receive analog output for channel1 and AOUT2 is used for channel2.

The output signal has an amplitude of 3.4Vpp above and below the signal ground voltage(SG).When the digital signal of +3dBm0 is input to DIN, it can drive a load of 600 Ω or more.

During power saving or power down mode, these outputs are at the voltage level of SG with a high impedance.

VDD

Power supply for +5V.

A power supply for an analog circuit of the system which the device is applied should be used a bypass capacitor of 0.1µF with excellent high frequency characteristics and a capacitor of 10µF to 20µF should be connected between this pin and the AG pin if needed.

AG

Analog signal ground.

DG

Ground for the digital signal circuits.

This ground is separate from the analog signal ground. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground.

SGC

Used to generate the signal ground voltage level by connecting a bypass capacitor. Connect a 0.1µF capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

BCLK

Shift clock signal input for the DIN signals.

The frequency, equal to the data rate, is 256, 384, 512, 768, 1024, 1536, 1544, 2048, 4096KHz.Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

RSYNC

Receive synchronizing signal input.

Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK (generated from the same clock source as BCLK). The frequency should be 8KHz ± 50ppm to guarantee the AC characteristics which are mainly the frequency characteristic of the receive section.

However, if the frequency characteristic of the system used is not strictly specified, this device can operate in the range of 6KHz to 9KHz, but the electrical characteristics in this specifications are not guaranteed.

XSYNC

Transmit synchronizing signal input.

The PCM output signal from the DOUT pin is output in synchronization with this transmit synchronizing signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section. This synchronizing signal must be synchronized in phase with the BCLK. The frequency should be 8KHz ± 50ppm to guarantee the AC characteristics which are mainly the frequency characteristic of the transmit section.

However, if the frequency characteristic of the system used is not strictly specified, this device can operate in the range of 6KHz to 9KHz, but the electrical characteristics in this specifications are not guaranteed.

Setting this signal to logic "1" or "0" drives both CH1 and CH2 circuits to power saving state.

DIN

DIN is a data input pin.

Signals which consist of a total 28 bits configured by the voice band PCM signal(16 bits for 2CH), the general-purpose latch signal(6 bits for both channel), the power down control signal for each channel(2 bits) and empty bit(4 bits),

The signal is shifted at a falling edge of the BCLK signal and latched into the internal register when shifted by 28 bits.

The voice band signal is converted to an analog signal in synchronization with the RSYNC signal and BCLK. The analog signal of channel 1 is output from AOUT1 pin and the analog signal of channel 2 is output from AOUT2 pin.

The general purpose latch signal(C3A,C2A,C1A,C3B,C2B,C1B) are output from six latch output pins.

When the PD1 bit of DIN is at logic "0" level, CH1 block is in a power down state. When the PD2 bit of DIN is at logic "0" level, CH2 block is in a power down state.

DOUT

DOUT is a data output pin.

Signal which consist of a total 28 bits configured by the voice band PCM signal(16 bits for 2CH), the echo bit(6 bits for latch signal and 2 bits for power down state indication), and empty bit(4 bits),

The output signal is output from CH1's MSD bit in a sequential order, synchronizing with the rising edge of the BCLK signal.

The first bit of DOUT may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.

This pin is in a high impedance state during power saving state or power down state.

A pull-up resistor must be connected to this pin because it is an open drain output.

This device is compatible with ITU-T recommendation on coding law and output coding format.

INPUT / OUTPUT Level	PCMIN / PCMOUT	
	ALOW = 0 (μ-law)	ALOW = 1 (A-law)
+ Full scale	MSD 1 0 0 0 0 0 0 0	MSD 1 0 1 0 1 0 1 0
+ 0	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1
- 0	0 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1
- Full scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

PDN

Power down control signal.

When PDN is at logic "0" level, both CH1 and CH2 circuits are in a power down state. Also the all internal latches are in initial state(logic "0" level).

ALAW

Control signal input of the companding law selection.

The CODEC will operate in the μ -law when this pin is at a logic "0" level and the CODEC will operate in the A-law when this pin is at a logic "1" level. The CODEC operates in the μ -law if the pin is left open, as this pin is internally pulled down.

C1A, C2A, C3A, C1B, C2B, C3B

General-purpose Latched output signal.

C1A, C2A, C3A, C1B, C2B, C3B bits of DIN are latched at internal timing.

These outputs can drive a LSTTL/CMOS device without external resistor.

❖ ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Conditions	Ratings	Unit
Power Supply Voltage	V_{DD}	-	- 0.3 ~ 7.0	V
Analog Input Voltage	V_{AIN}	AG=0V, DG=0V	- 0.3 ~ V_{DD}+0.3	
Digital Input Voltage	V_{DIN}	AG=0V, DG=0V	- 0.3 ~ V_{DD}+0.3	
Operating Temperature	T_{OP}	-	- 40 ~ 85	°C
Storage Temperature	T_{STG}	-	- 55 ~ 150	

❖ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	4.75	5.0	5.25	V
Analog Input Voltage	V_{AIN}	Gain = 1	-	-	3.4	V_{PP}
Digital Input High Voltage	V_{IH}	XSYNC, RSYNC, BCLK, DIN, PDN	2.2	-	V_{DD}	V
Digital Input Low Voltage	V_{IL}		0	-	0.8	V
Clock Frequency	F_{CLK}	BCLK	256 768 1544	384 1024 2048	512 1536 4096	KHz
Sync Pulse Frequency	F_{SYNC}	XSYNC, RSYNC	-	8	-	KHz
Clock Duty Ratio	D_{CLK}	BCLK	40	50	60	%
Digital Input Rise Time	T_{IR}	XSYNC, RSYNC, BCLK, DIN, PDN	-	-	50	ns
Digital Input Fall Time	T_{IF}		-	-	50	ns
Transmit Sync Pulse Setting Time	T_{XS}	BCLK to XSYNC	50	-	-	ns
	T_{SX}	XSYNC to BCLK	50	-	-	ns
Receive Sync Pulse Setting Time	T_{RS}	BCLK to RSYNC	50	-	-	ns
	T_{SR}	RSYNC to BCLK	50	-	-	ns
Sync Pulse Width	T_{WS}	XSYNC, RSYNC	1 BCLK	-	100	μs
DIN set-up Time	T_{DS}	DIN	50	-	-	ns
DIN Hold Time	T_{DH}	DIN	50	-	-	ns
Digital Output Load	R_{DL}	Pull-up register, DOUT	0.5	-	-	KΩ
	C_{DL}	DOUT	-	-	50	pF
		C1A, C2A, C3A, C1B, C2B, C3B	-	-	50	pF
Analog Input Allowable DC offset	V_{OFF}	Transmit gain stage, Gain = 1	$V_{DD}/2$ -100	-	$V_{DD}/2$ +100	mV
		Transmit gain stage, Gain = 10	$V_{DD}/2$ -10	-	$V_{DD}/2$ +10	mV
Allowable Jitter Width		XSYNC, RSYNC	-	-	500	ns

❖ ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics V_{DD}=5V±5%, Ta= -40 ~ 85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating mode, No signal	-	7.0	14.0	mA
	I_{DD2}	Power saving mode, PDN=1, XSYNC or BCLK OFF	-	1.3	3.0	mA
	I_{DD3}	Power down mode, PDN=0	-	0.01	0.05	mA
Input High Voltage	V_{IH}	XSYNC, RSYNC, BCLK, DIN	2.2	-	V_{DD}	V
Input Low Voltage	V_{IL}	PDN, ALAW	0	-	0.8	V
High Level Input leakage current	I_{IH}	XSYNC, RSYNC, BCLK, DIN	-	-	2	µA
Low Level Input leakage current	I_{IL}	PDN, ALAW	-	-	0.5	µA
Digital Output low voltage	V_{OL}	DOUT R pull-up: 0.5K	0	0.2	0.4	V
		C1A, C2A, C3A, C1B, C2B, C3B I_{OL} = 0.4mA	0	0.2	0.4	V
Digital Output High Voltage	V_{OH}	C1A,C2A,C3A, C1B,C2B,C3B I_{OH} = 0.4mA	2.5	-	-	V
		C1A,C2A,C3A, C1B,C2B,C3B I_{OH} = 10uA	4.5	-	-	V
Digital Output leakage current	I_O	DOUT high impedance state	-	-	10	µA
Input capacitance	C_{IN}		-	5	-	pF

Transmit Analog interface Characteristics V_{DD}=5V±5%, Ta= -40 ~ 85°C

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AIN1, AIN2		10	-	-	MΩ
Output Load Resistance	R_{LGX}	GSX1, GSX2		20	-	-	KΩ
Output Load Capacitance	C_{LGX}	With respect to SG		-	-	30	pF
Output Amplitude	V_{OGX}			- 1.7	-	1.7	V
Offset Voltage	V_{OSGX}		Gain = 1	- 20	-	20	mV

Receive Analog interface Characteristics V_{DD}=5V±5%, Ta= -40 ~ 85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Load Resistance	R_{LAO}	AOUT1, AOUT2 (each) With respect to SG	0.6	-	-	KΩ
Output Load Capacitance	C_{LAO}	AOUT1, AOUT2	-	-	50	PF
Output Amplitude	V_{OAO}	AOUT1, AOUT2,RL=0.6KΩ With respect to SG	- 1.7	-	1.7	V
Offset Voltage	V_{OSAO}	AIN1, AIN2 With respect to SG	- 100	-	100	mV

AC Characteristics

V_{DD}=5V±5%, Ta= -40 ~ 85°C

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
		freq. (Hz)	level (dBmO)					
Transmit Frequency Response	**Loss T1**	60	0	GSXn to DOUT (attenuation)	20	26	-	dB
	Loss T2	300			- 0.15	0.07	0.2	
	Loss T3	1020			Reference			
	Loss T4	2020			- 0.15	- 0.04	0.2	
	Loss T5	3000			- 0.15	0.06	0.2	
	Loss T6	3400			0	0.4	0.8	
Receive Frequency Response	**Loss R1**	300		DIN to AOUTn (attenuation)	- 0.15	- 0.03	0.2	dB
	Loss R2	1020			Reference			
	Loss R3	2020			- 0.15	- 0.02	0.2	
	Loss R4	3000			- 0.15	0.15	0.2	
	Loss R5	3400			0	0.56	0.8	
Transmit Signal to Distortion Ratio	**SDT1**	1020	3	GSXn to DOUT *1	35	43	-	dB
	SDT2		0		35	41	-	
	SDT3		- 30		35	38	-	
	SDT4		- 40		29	31.5	-	
	SDT5		- 45		24	27	-	
Receive Signal to Distortion Ratio	**SDR1**	1020	3	DIN to AOUTn *1	36	43	-	dB
	SDR2		0		36	41	-	
	SDR3		- 30		36	40	-	
	SDR4		- 40		30	33.5	-	
	SDR5		- 45		25	30	-	
Transmit gain Tracking	**GTT1**	1020	3	GSXn to DOUT	- 0.3	0.01	0.3	dB
	GTT2		- 10		Reference			
	GTT3		- 40		- 0.3	0	0.3	
	GTT4		- 50		- 0.5	- 0.03	0.5	
	GTT5		- 55		- 1.2	0.15	1.2	
Receive gain Tracking	**GTR1**	1020	3	DIN to AOUTn	- 0.3	- 0.06	0.3	dB
	GTR2		- 10		Reference			
	GTR3		- 40		- 0.3	- 0.02	0.3	
	GTR4		- 50		- 0.5	- 0.02	0.5	
	GTR5		- 55		- 1.2	- 0.27	1.2	

*1 psophometric filter is used

AC Characteristics (Continued)

V_{DD}=5V±5%, Ta= -40 ~ 85°C

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
		freq. (Hz)	level (dB_{mO})					
Idle channel noise	**NIDLET**	-	-	AIN=SG *1	-	- 73.5	- 70	dB_{mOp}
				AIN to DOUT *2	-	- 71.5	- 68	
	NIDLER	-	-	DIN:0 code *1 DIN to AOUT	-	- 78	- 75	
Absolute level (Initial Difference)	**AVT**	1020	0	GSXn to DOUT V_{DD}=5V,Ta=25°C	0.82	0.85	0.88	V_{rms}
	AVR			DIN to AOUTn V_{DD}=5V,Ta=25°C	0.82	0.85	0.88	
Absolute level (Deviation of Temp-erature and Power)	**AVTt**			V_{DD}=5V±5, Ta= -40 ~ 85°C	- 0.3	-	0.3	dB
	AVRt				- 0.3	-	0.3	
Absolute Delay	**T_D**	1020	0	A to A mode BCLK=2048KHz	-	-	0.6	ms
Transmit group delay	**Tgd T1**	500	0	*3		0.19	0.75	ms
	Tgd T2	600			-	0.11	0.35	
	Tgd T3	1000			-	0.02	0.125	
	Tgd T4	2600			-	0.05	0.125	
	Tgd T5	2800			-	0.07	0.75	
Receive group delay	**Tgd R1**	500	0	*3	-	0.00	0.75	ms
	Tgd R2	600			-	0.00	0.35	
	Tgd R3	1000			-	0.00	0.125	
	Tgd R4	2600			-	0.09	0.125	
	Tgd R5	2800			-	0.12	0.75	
Cross talk attenuation	**CRT**	1020	0	Trans to Recv.	75	80		dB
	CRR			Recv to Trans	70	76	-	
	CRCH			channel to channel	75	78	-	

*1 Psophometric filter is used

*2 Upper is specified for the μ-law, lower for the A-law

*3 Minimum value of the group delay distortion

AC Characteristics (Continued)

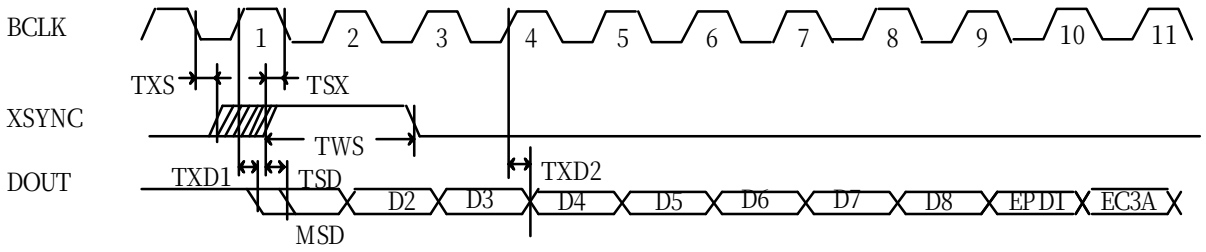
V_{DD}=5V±5%, Ta= -40 ~ 85°C

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
		freq. (Hz)	level (dBmO)					
Discrimination	**DIS**	4.6K to 72K	0	0 to 4000Hz	30	32	-	dB
Out of band spurious	**S**	300 to 3400	0	4.6KHz to 100KHz	-	-37.5	-35	dBmOp
Intermodulation Distortion	**IMD**	fa=470 fb=320	- 4	2 fa - fb	-	- 52	- 35	dBmO
Power Supply Noise Rejection Ratio	**PSRT**	0 to 50K	50mV$_{PP}$	* 4	-	30	-	dB
	PSRR							
Digital output delay time	**Tsd**	DOUT			20	-	100	ns
	Txd1	Pull-up register = 0.5K			20	-	100	
	Txd2	CL = 50pF and 1 LSTTL			20	-	100	
	Txd3				20	-	100	
	TpdC	C1A, C2A, C3A, C1B, C2B, C3B CL = 50pF and 1 LSTTL			20	-	1000	ns

*4 The measurement under idle channel noise

❖ TIMING DIAGRAM

TRANSMIT SIDE



RECEIVE SIDE

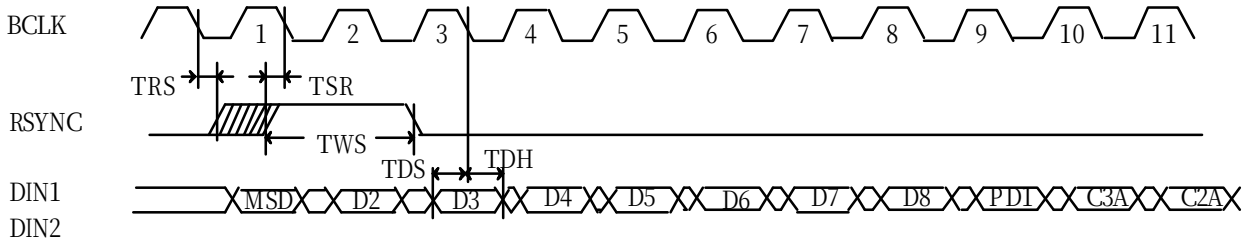
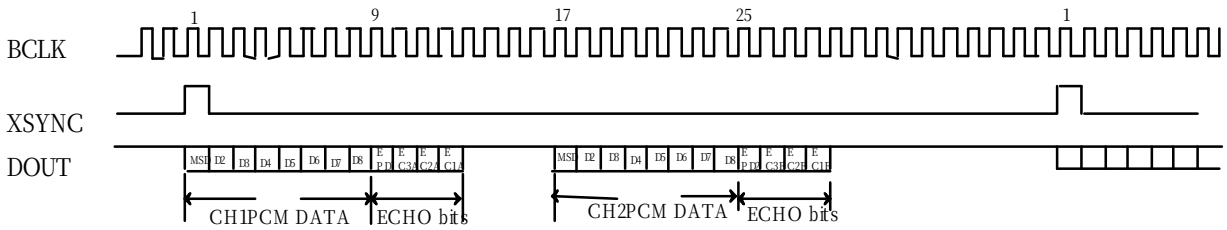


Figure 1 TIMING DIAGRAM

TRANSMIT SIDE



RECEIVE SIDE

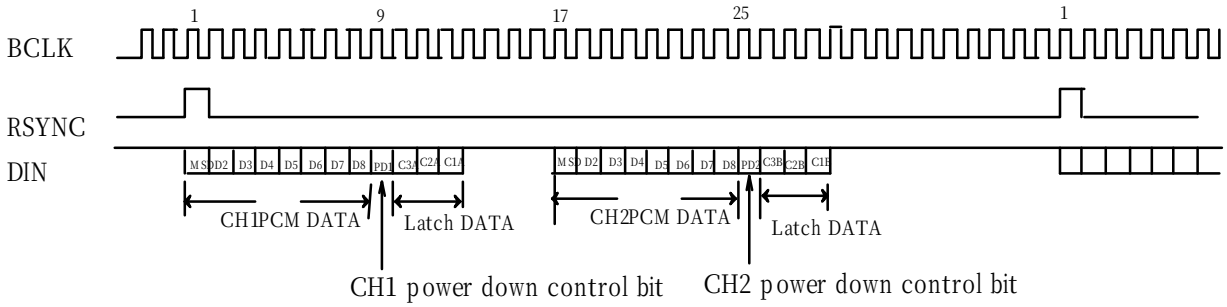


Figure 2 BIT CONFIGURATION

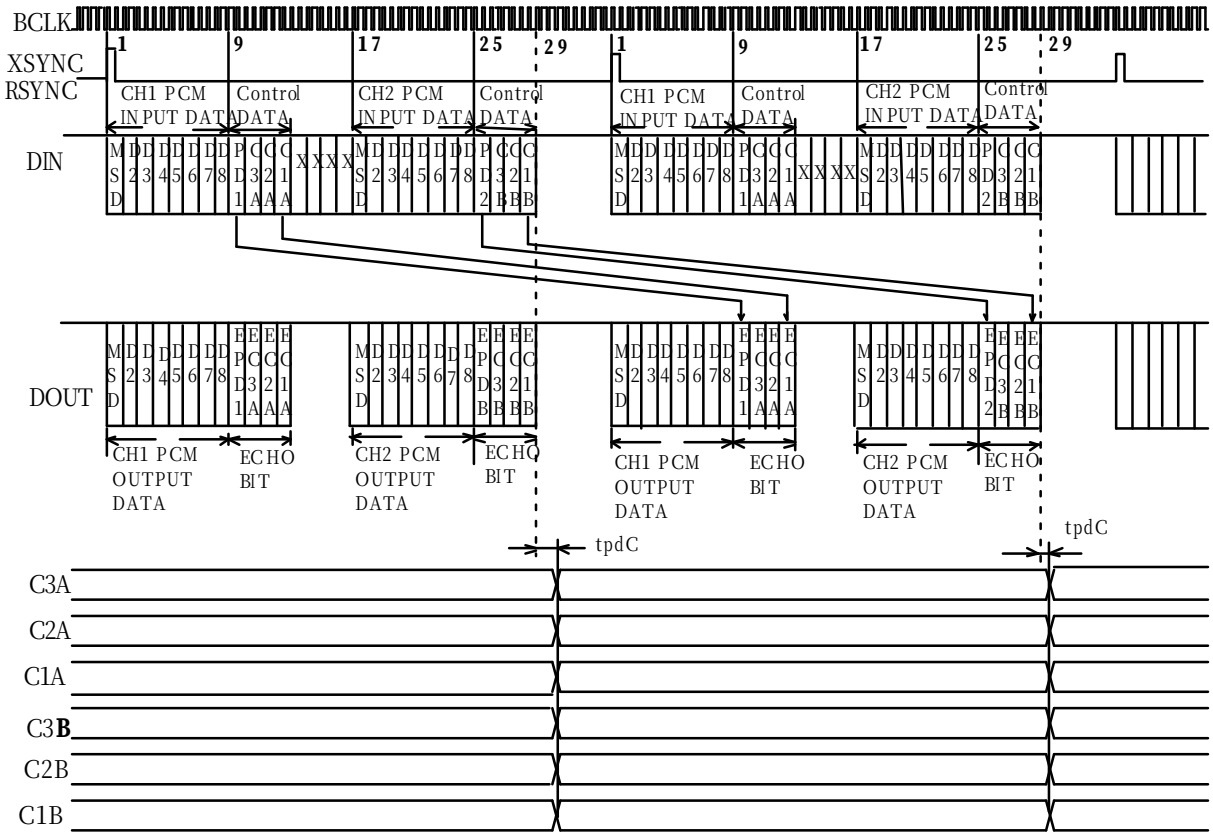
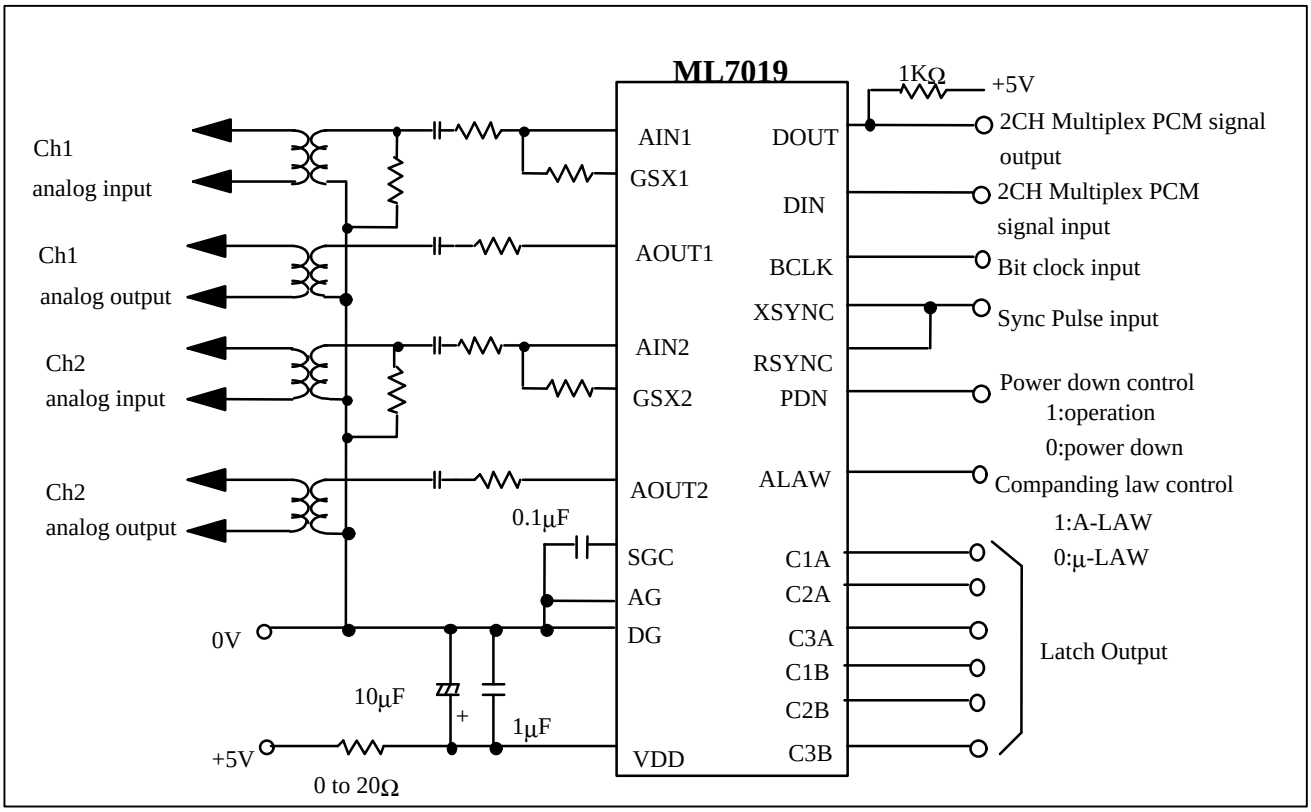


Figure 3 CONTROL BIT TIMING and ECHO BACK TIMING

❖ Application circuit



❖ RECOMMENDATIONS FOR ACTUAL DESIGN

- To assure electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and DG pin each other as close as possible. Connect to the system ground with low impedance.
- unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers surround the device.
- Keep the voltage on the VDD pin not lower than -0.3V even instantaneously to avoid latch-up phenomenon when turning the power on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these device.