ML6429 DEMO Evaluation Kit User's Guide

User Selectable Quad/Octal Video Filters with SCART and EVC Interface

Description

The ML6429 Evaluation Kit is a fully functional octal (2-quads) multi-video standard filter operating from a single 5V ±10% power source. To reduce setup time the Evaluation Board is configured with quick connect female BNCs (for all video inputs and outputs) and female banana plugs for input power. For designs requiring compliance to current video connector standards the ML6429 Evaluation Board video signals are provided to a SCART (Peritel) and an Enhanced Video Connector (EVC) connector.

Note: This Evaluation Board was designed to exhibit all the ML6429 features available. The user can choose only that portion of the circuit required for a cost-effective solution.

The ML6429 is packaged in a 24 pin SOIC. It is a quad 4th order filter for applications requiring capacitive coupling of inputs and outputs. In addition to providing DAC output filtering of virtually any video signal (Composite, Y/C, RGB, etc.), the ML6429 includes a 5th wideband channel for use with the device's channel multiplexing and swapping features. These features are detailed in the Additional Features section. All outputs include 2X gain amps for driving $2V_{P-P}$ into a 150Ω load or $1V_{P-P}$ into a 75Ω load. Additional features of the ML6429 include SYNCOUT and SYNCIN pins for synchronization with SLAVE units or for external synchronization to an HSYNC signal for component video signals lacking embedded sync. Additional filtering of video signals is possible with the ML6429 by cascading a filtered output to an unused input.

For minimal noise and cross-coupling the ML6429 was laid out on a double sided printed circuit board with an extensive solder-side ground plane. The board demonstrates performance and illustrates critical layout practices necessary for reliable operation. See Figure 11 for the evaluation board schematic and Figures 8 through 10 for the layout.

Block Diagram

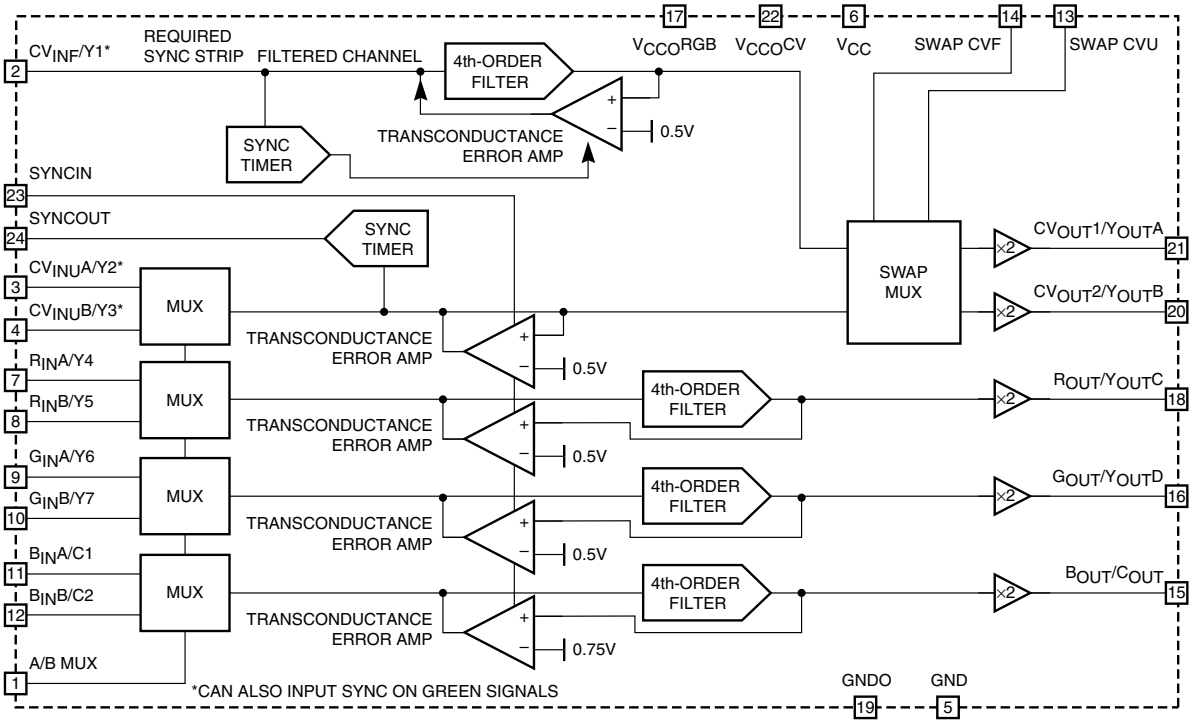


Figure 1. ML6429 Block Diagram

Evaluation Kit Contents

The evaluation package contains the following items:

1. ML6429 Demo User's Guide
2. ML6429 Evaluation Board
3. The latest revision of the ML6429 Data Sheet can be obtained from Fairchild Semiconductor's web site at http://www.fairchildsemi.com or on the CD Catalog.

Testing Functionality

Table 1. ML6429Eval Kit Operating Specifications at 5V

Input Coupling	Output Coupling	fC (–3dB) filtered/ unfiltered	Typical I_{CC} (No Load)
AC	AC	6.7MHz / 40MHz	200mA

Setup

Note: Due to the large number of possible Video input and output permutations (see Tables 2 and 3), a complete testing procedure of the Evaluation Board is outside the scope of this document. General guidelines for setting up the board are provided, along with a list of minimal testing equipment required. To fully evaluate the board requires at least 2 dissimilar synchronized Video Sources and their corresponding HSYNC (TTL or CMOS) signal.

The following test equipment is necessary to test the ML6429 Evaluation Board:

One Power Supply: 5V ±10%, 250mA max

One 4 inch (or larger) High Resolution CRT monitor: Sony PVM-14M2U

One NTSC Composite Video Signal: Magni 2021 Programmable Signal Generator (or an equivalent Composite Video Source, e.g., VCR, TV baseband Video Out)

Assorted video cables

Test

Use the following procedure to verify that the ML6429 Evaluation Board is functional. Do not turn the power supply on until all connections are completed.

1. Set the power supply for 0.0V. Connect the power supply to the input voltage terminals of the Evaluation Board.
2. Make the video connections. Note: Use the shortest possible cables (75Ω suggested, 50Ω acceptable) for all video connections.
3. Ensure all jumpers and switches are in their default position. See Figure 11 and Table 2.
4. Connect the Magni video out to CVIN2
5. Connect one of the CVOUT2/YOUT1 outputs from the Evaluation Board to Input A of the CRT monitor. Select Channel A of the monitor. A high quality video test pattern will appear on the monitor screen.
6. Use the remaining CVOUT2/YOUT1 as a Video Signal Source to test the remaining channels of the Evaluation Board. See Tables 2, 3 and 4.

Table 2. Switch and Header Shunt Settings

Switch/Header	Default	Composite	Y/C	RGB	CV_{OUT}+, Y+
SW1 - A	open (Note 1)	open (Note 1)	open (Note 1)	open (Note 1)	open (Note 1)
SW1 - B	open (Note 1)	open (Note 1)	open (Note 1)	open (Note 1)	open (Note 1)
SW1 - C	open (Note 1)	open (Note 1)	open (Note 1)	open (Note 1)	open (Note 1)
JP1	2, 3	2, 3	2, 3	2, 3	2, 3
JP2	1, 2	1, 2	1, 2	2, 3	1, 2
JP3	1, 2 (Note 2)	1, 2 (Note 2)	1, 2 (Note 2)	1, 2 (Note 2)	1, 2 (Note 2)
JP4	1, 2	1, 2	1, 2	1, 2	1, 2
JP5	2, 3	2, 3	2, 3	1, 2	2, 3
JP6	1, 2	1, 2	1, 2	1, 2	1, 2
HSYNCIN	2, 3	2, 3	2, 3	2, 3	2, 3
VIDEO IN	MASTER (U1)	MASTER (U1)	MASTER (U1)	SLAVE (U2) (Note 3)	MASTER (U1)

Note:

1. The positions of SW1 - A and SW1 - B are set according to the user's discretion as to which output scheme is desired from U1 (MASTER) pins 21 and 22. See Tables 3 and 4 for A/B MUX, SWAP CVU and SWAP CVF function definition settings.
2. For SCART (Peritel) applications requiring HSYNC on pin 16 move the header shunt on JP3 to pins 2 and 3.
3. The ML6429 Evaluation Board was designed to accept RGB video with a composite or Y video signal applied to U1 pin 3 or 4, respectively, to obtain sync for U2 and U3. If these signals are unavailable use one of the following two methods to ensure U2 is provided with a sync signal:

   3a. Apply the GREEN channel to CVIN2 or YIN1 (U1) of the Evaluation Board instead of GIN (U2).

   3b. If an HSYNC signal is available apply it to HSYNCIN of the Evaluation Board and move the header shunt on JP1 to pins 1 and 2. Move the header shunt on JP4 to pins 2 and 3. Connect the three RGB video lines to their respective Evaluation Board inputs.

Table 3. Inputs and Outputs

Inputs		Outputs			
A/B MUX (SW1-C)	**VIDEO**	**$CV_{OUT}1$**	**$CV_{OUT}2/Y_{OUT}1$ (2X)**	**$Y_{OUT}1$**	**$C_{OUT}2$**
1/0 (SW1-C open/ closed)	$CV_{IN}1$	$CV_{IN}1/CV_{IN}1$	$CV_{IN}2/Y_{IN}1$	$Y_{IN}2/Y_{IN}2$	$C_{IN}1/C_{IN}1$

Slave filter (U2) Output vs. Input is functionally identical to Master. Note the different input and output call-outs on the Evaluation Board for the Slave filter (U2). Note: SWAP CVU & SWAP CVF are at logic low levels.

Table 4. Inputs and Outputs

Inputs			Outputs		
Swap CVF SW1 - A	**Swap CVU SW1 - B**	**A/B Mux SW1 - C**	**$CV_{OUT}1$**	**CVOUT2 / YOUT1**	**Remaining Outputs**
0 (open)	0 (open)	1 (open)	$CV_{IN}1$	$CV_{IN}2$	Note 1
0 (open)	0 (open)	0 (closed)	$CV_{IN}1$	$Y_{IN}1$	Note 1
0 (open)	1 (closed)	1 (open)	$CV_{IN}1$	$CV_{IN}1$	Note 1
0 (open)	1 (closed)	0 (closed)	$CV_{IN}1$	$CV_{IN}1$	Note 1
1 (closed)	0 (open)	1 (open)	$CV_{IN}2$	$CV_{IN}2$	Note 1
1 (closed)	0 (open)	0 (closed)	$Y_{IN}1$	$Y_{IN}1$	Note 1
1 (closed)	1 (closed)	1 (open)	$CV_{IN}2$	$CV_{IN}1$	Note 1
1 (closed)	1 (closed)	0 (closed)	$Y_{IN}1$	$CV_{IN}1$	Note 1

Additional Features

The ML6429 DEMO Evaluation Board was designed to exhibit all the capabilities of the ML6429. This section describes these functions and shows how to properly implement them. An example of a real application using a single ML6429 is shown in Figure 2.

Filtered Input

The ML6429 contains a separate channel (CV_{INF}/Y1) complete with sync clamp/restore for DAC generated signals requiring 4th order reconstruction filtering. This channel is completely independent of the remaining channels and requires an embedded SYNC video signal to function properly.

Unfiltered (Wideband) Inputs

The ML6429 provides 2 channels (CV_{INU}A/Y2, CV_{INU}B/Y3) with wideband frequency response (f_C = 40MHz) to buffer and amplify signals requiring no additional filtering, such as from an RCA video jack (baseband video) available on many televisions and VCRs. These channels contain the SYNC detect/restore required by the remainder of the ML6429 for sync clamp/restore. Both signals must contain embedded sync if sync is not otherwise supplied externally to the SYNCIN pin.

SYNCOUT and SYNCIN

For proper operation the ML6429 requires either an embedded sync signal on one of the CV_{INU} channels, or the application of an external HSYNC signal (TTL or CMOS compatible) to pin 23 if the video to these two channels lacks

embedded sync. The sync signals control all internal timing of the ML6429 and provide sync restoration for establishing the proper voltage level of the sync tip of all the video output signals from the part. Whether the sync is embedded or externally applied (HSYNC), the ML6429 generates an output signal, SYNCOUT, for use in cascading additional filters or general system timing. When the sync is embedded in the video input signal the SYNCOUT pin must be tied to the SYNCIN pin for proper operation. When the signal is externally applied to SYNCIN, a SYNCOUT signal is generated by the ML6429. This pin can be left open or used for synchronization of other ML6429s or as a general system timing signal.

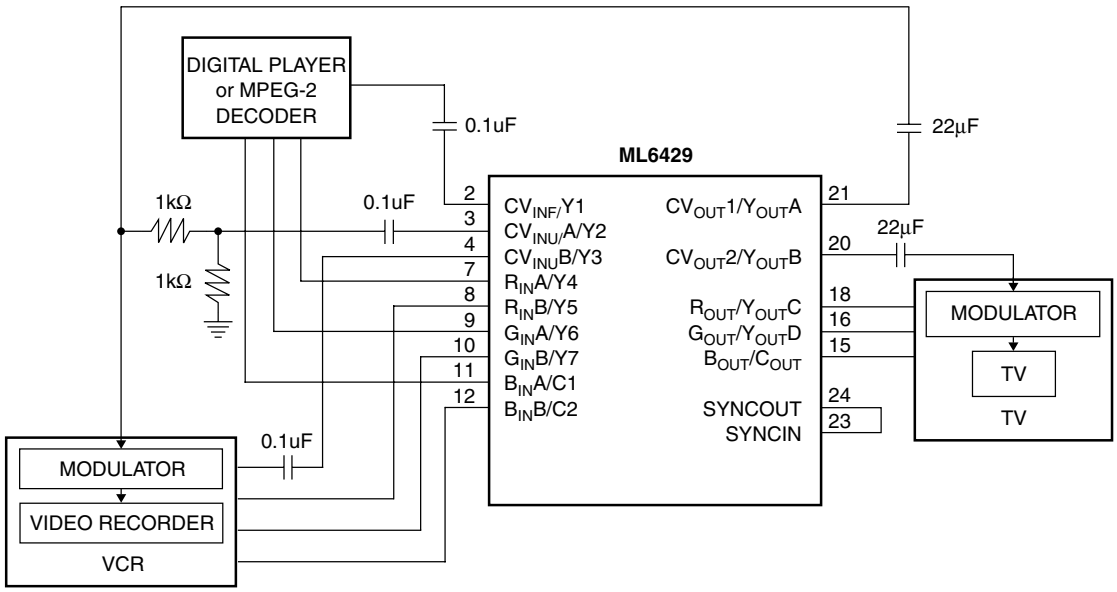


Figure 2. ML6429 Application

Y/C Video and the Chroma Input

Ensure that the chroma video signal(s) are applied to the correct input(s) — pins 11 and 12 — when S-Video is applied to the ML6429. These inputs differ from the other channels in the amount of DC offset applied during sync restoration. Chroma signals have bi-directional voltage swings and require a higher input offset to avoid swinging below ground.

Video Output Drivers

All video outputs drive $2V_{P-P}$ into a 150Ω load or $1V_{P-P}$ into a 75Ω load. Figure 11 displays the ML6429 driving two 150Ω loads from one of the SWAP MUX outputs. All ML6429 outputs are capable of driving two 150Ω or two 75Ω loads. Ensure the total package power dissipation limit is not exceeded as the number of loads is increased. Another feature of the ML6429 is that the outputs can be DC coupled to the load(s). DC coupling of the outputs draws more power than AC coupling, and the total device dissipation must be monitored for reliable operation well below the maximum operating junction temperature. The user must take into account the tolerance of the sync tip voltage, particularly when the load is a D to A converter, when DC coupling the loads. Note that the offset voltage of the chroma inputs (pins 11 and 12) makes these channels unusable for composite video signals. These 2 inputs must be fed with Blue (RGB) and/or chroma signals only.

Cascading Channels for Increased Filtering

In applications where the video signal is under-sampled or requires a steeper roll-off see Figures 4 and 11. Two filters are cascaded for an 80dB/decade roll-off. Note the use of 1kΩ termination resistors on the output of U1. This is done to reduce the loading on U1 and preserve the DC restoration capability of U2. Do not increase the termination resistor values above 1kΩ. This cascading technique can be used with additional filters to obtain even steeper roll-offs.

Measured Performance

The ML6429 filtering action is demonstrated in the graph shown in Figure 3. A network analyzer is connected to a filtered input channel with a 200mV RMS test signal and a plot is made of the frequency response. The resulting amplitude versus frequency plot demonstrates the accuracy of the ML6429 regarding flatness of response, -3dB cutoff point, and linear 40dB/decade rolloff above cutoff. Time domain measurements can be made using the output of DACs to feed the filter, but the information is not as useful as a Bode plot. To obtain this measurement it is necessary to apply a current limited DC offset voltage (1.4V, 4.7kΩ) directly to the ML6429 input pin.

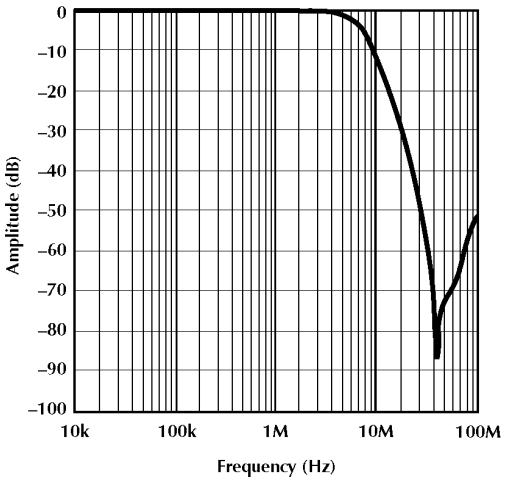


Figure 3. Filtered Channel

This allows the internal sync restore circuitry to establish the correct sync tip value. Refer to the ML6429 data sheet for additional graphs and waveforms.

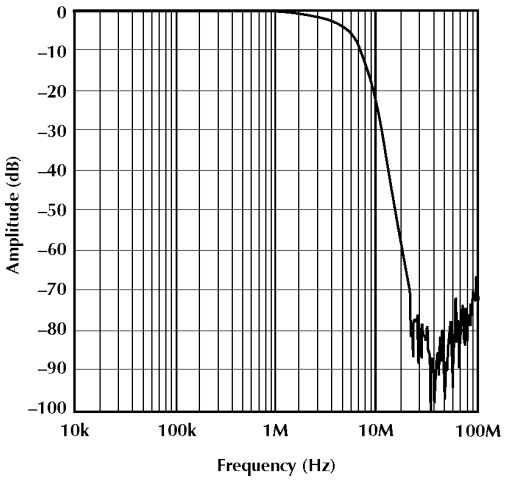


Figure 4. Two Cascaded Filtered Channels

Figure 4 illustrates the performance of the ML6429 Evaluation Board using the output of one filtered channel as the input to another filtered channel (2 cascaded filters). Note the increased roll-off above f_C of 80dB/decade. This application can be applied to unfiltered video signals which have been under-sampled, or when an anti-aliasing filter is required. Refer to Figure 11 and Table 2 for implementation of this 4-pole filter. Note that it is unnecessary to terminate the output of the first filter into 150Ω. The use of 1kΩ termination resistors reduces the power consumption of the ML6429.

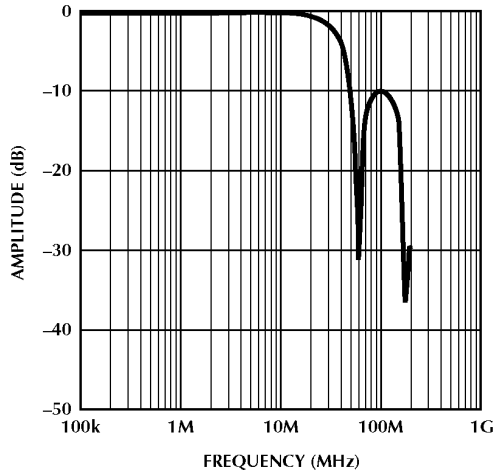


Figure 5. Unfiltered Channel

The unfiltered channels of the ML6429 are intended as buffers for video signals requiring no filtering. Figure 5 displays the high frequency bandwidth of these channels. The high frequency cutoff and response flatness guarantees no degradation of the video signal output of this channel.

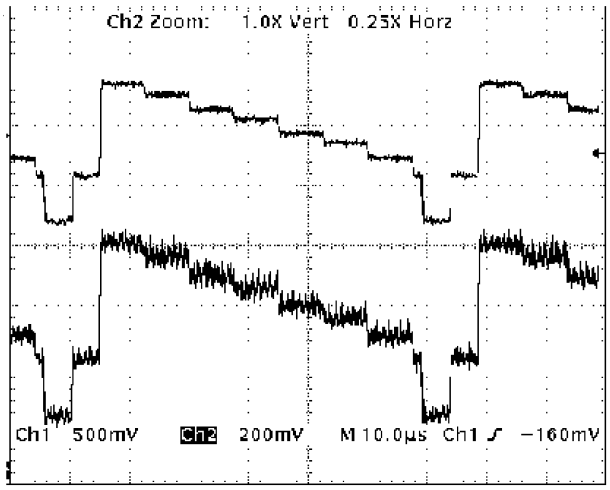


Figure 6. Filtered Channel Response to DAC Generated Luma Video Signals

Test Equipment: Tektronix TDS 540 Digitizing Scope
Test Conditions: V_{IN} = 5.0V
CH1: V_{OUT} @ 500mV/DIV
CH2: V_{DAC} @ 200mV/DIV
Horiz: 10µs/DIV

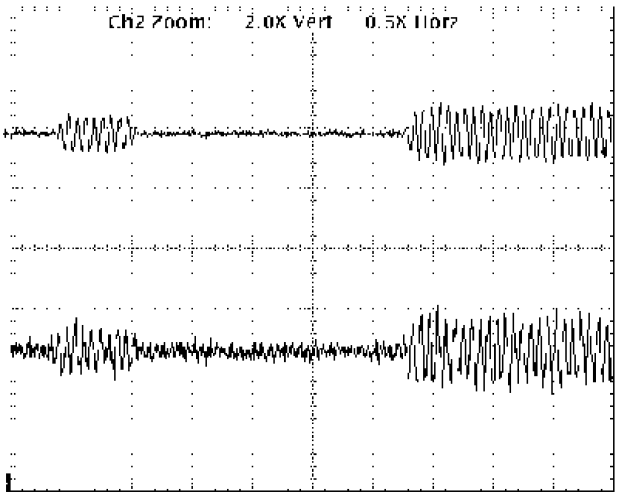


Figure 7. Filtered Channel Response to DAC Generated Chroma Video Signals
Test Equipment: Tektronix TDS 540 Digitizing Scope
Test Conditions: V_{IN} = 5.0V
CH1: V_{OUT} @ 500mV/DIV
CH2: V_{DAC} @ 250mV/DIV
Horiz: 2µs/DIV

Layout Considerations

Figure 11 is the Evaluation board schematic. Figures 8 through 10 show the board layout. Note the proximity of bypass capacitors C10 through C13 to U1 and C29 through C32 to U2. Notice also the use of ferrite beads FB1 and FB2 to provide separate filtered power to the VCC pins. This bypassing minimizes the cross-talk between power and analog circuitry. In addition, the solder side of the Evaluation Board is a large ground plane resulting in low channel to channel cross-talk, and completes the high quality V_{CC} bypassing of the Master and Slave filters. The ML6429 will provide nearly equal performance if carefully laid out on a single-sided P.C. board. Also, the use of the ferrite beads may be unnecessary providing the part is locally bypassed with 2 capacitors (0.1µf and 1µF) located as near to the IC as possible, with direct connections to the V_{CC} and GND pins.

Minimize video input and output trace lengths for the lowest possible P.C. trace inductance and capacitance.

Using the ML6429 Evaluation Board for system evaluation is possible providing the size of the board allows for low noise connections. The video and power connectors can be removed and direct solder connections made to the board.

Take advantage of the SCART and EVC connectors when evaluating the board. This can save a lot of set-up time.

ML6429 Evaluation Kit Parts List

Item	Qty	Description	Vendor/Parts	Designation
Resistors				
1	18	75Ω, ±5% 1206 surface mount	Any	R1-R5, R10-R17, R20-R24
2	4	1kΩ, ±5% 1206 surface mount	Any	R6-R9
Capacitors				
3	9	220µF, 6.3V or 10V, tantalum, 7343 surface mount	AVX / TPSE227M010R0100 Sprague / 593D227X06R3E2W NEMCO / LSR 220/10HK100	C1-C9
4	4	1µF, 50V, ceramic, 1206 surface mount	Any	C10, C12, C29, C31
5	19	0.1µF, 50V, Ceramic, 1206 surface mount	Any	C11, C13-C28, C30, C32
ICs				
6	2	S-Video Filter, 24 pin SOIC	Micro Linear / ML6429CS	U1, U2
Hardware				
7	18	Female BNC connectors	A/D Electronics / 580-002-00	B_{IN}, B_{OUT}, C_{IN1}, C_{IN2}, C_{OUT1}, CV_{IN1}, CV_{IN2}, CV_{OUT1}, CV_{OUT2}/Y_{OUT1}, CV_{OUT2}/Y_{OUT1}, $CV_{OUT}+/Y_{OUT}+$, G_{IN}, G_{OUT}, R_{IN}, R_{OUT}, Y_{IN1}, Y_{IN2}, Y_{OUT2}
8	1	VESA EVC female right angle connector	Molex / 71182-1000	P2
9	1	SCART female right angle connector	Power Dynamics, Inc. / EI-022	P1
10	1	Switch, 4 position J-Lead slide DIP SMD	Digi-Key / GH1302	SW1
11	2	Ferrite bead, SMD	Digi-Key / 240-1030-1-ND	FB1, FB2
12	2	Female banana plug	Digi-Key / 108-0740-001	+5V, GND
13	6	Jumper header, 3 pin	Digi-Key / J147-ND	JP1-JP6
14	2	Header pin, 0.025 inch dia., gold plating.	Digi-Key / 929647-02-36-ND	HSYNCIN, GND
15	6	Header shunt	Digi-Key / 929950-00-ND	JP1-JP6 (Ref)
16	4	Threaded standoffs, 0.875 inch lg.	Digi-Key / J215	
17	4	Hex nuts, 6-32	Digi-Key / H220	
18	1	Printed Circuit Board, ML6429Eval, Rev. A	3 Day Protos / ML6429 Eval, Rev. A	

Vendor List

1. AVX	(207) 282-5111	6. NEMCO	
2. Sprague	(207) 324-4140	7. 3 Day Protos, Inc.	(408) 894-0130
3. Digi-Key	(800) 344-4539	8. GTI, Inc.	(800) 275-4884
4. 3M	(800) 321-9668	9. Powell Electronics	(408) 943-6442
5. A/D Electronics	(206) 851-8005	10.Eric Electronics	(408) 432-1111 (800) 406-3743

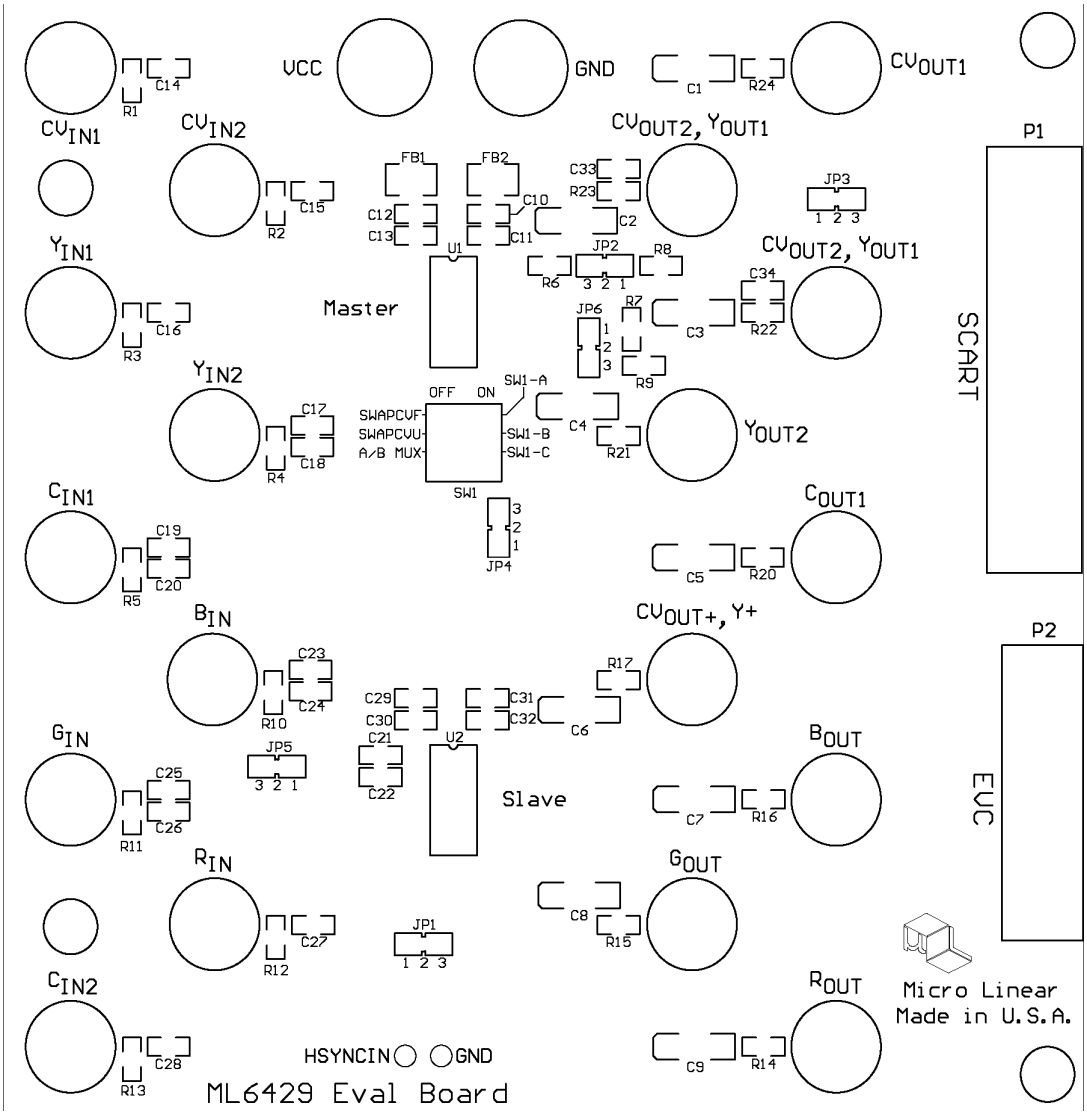


Figure 8. Top Silk

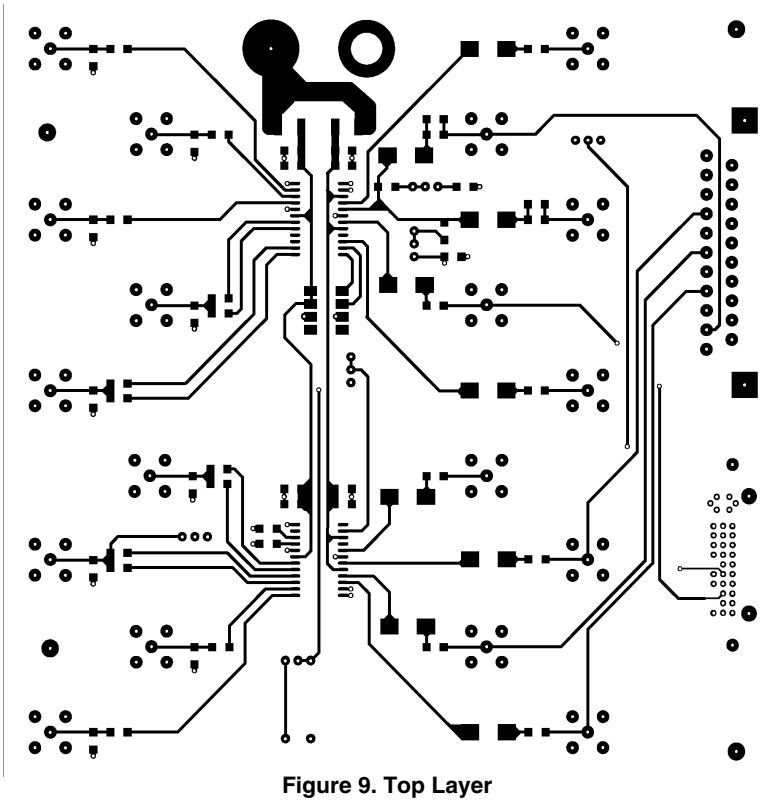


Figure 9. Top Layer

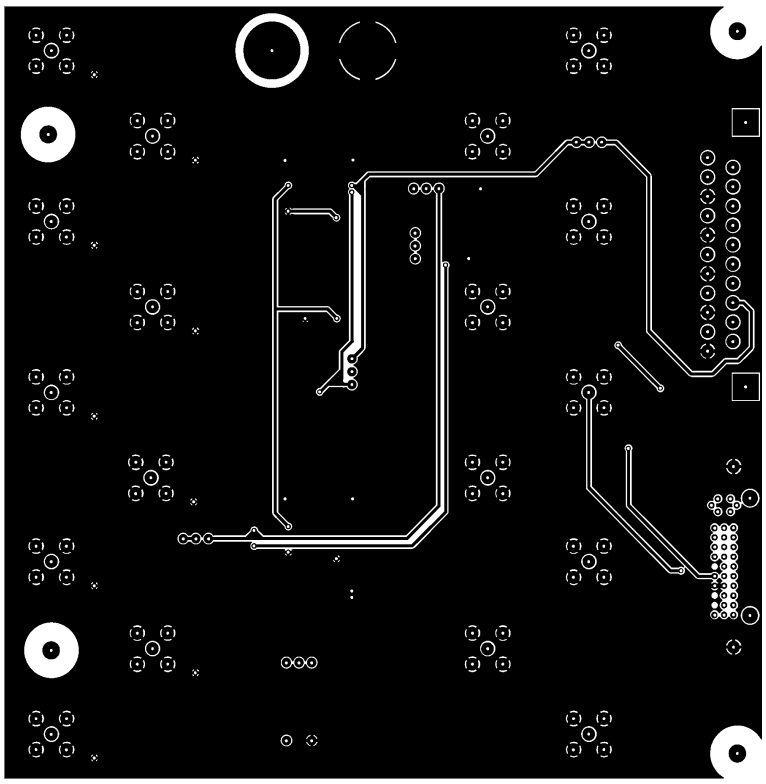
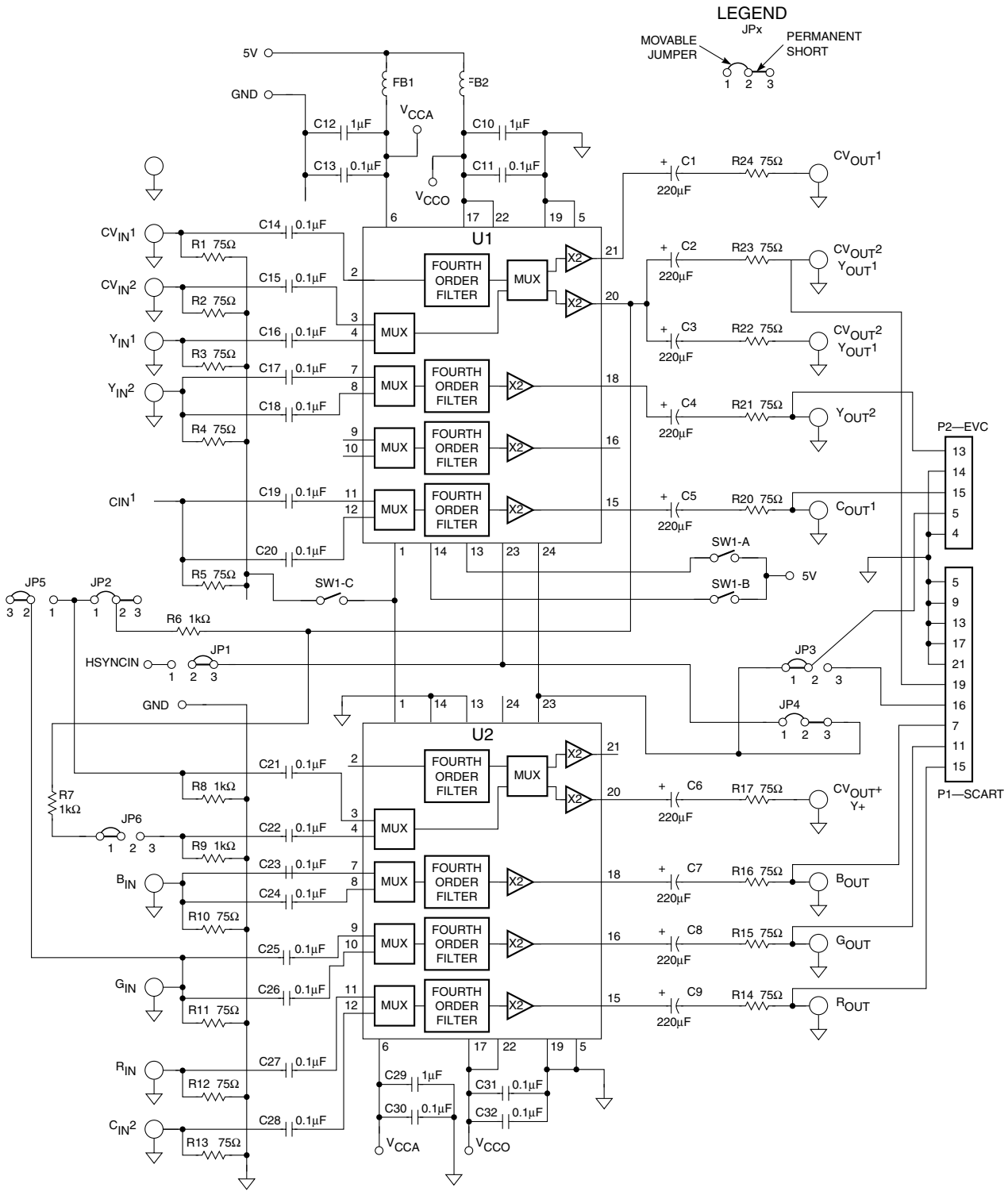


Figure 9. Bottom Layer


LEGEND
JPx
MOVABLE JUMPER
PERMANENT SHORT
5V
GND
FB1
FB2
VCCA
VCCO
C12 1µF
C13 0.1µF
C10 1µF
C11 0.1µF
U1
U2
FOURTH ORDER FILTER
MUX
X2
CVIN1
CVIN2
YIN1
YIN2
CIN1
BIN
GIN
RIN
CIN2
R1 75Ω
R2 75Ω
R3 75Ω
R4 75Ω
R5 75Ω
R6 1kΩ
R7 1kΩ
R8 1kΩ
R9 1kΩ
R10 75Ω
R11 75Ω
R12 75Ω
R13 75Ω
C14 0.1µF
C15 0.1µF
C16 0.1µF
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C25 0.1µF
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C27 0.1µF
C28 0.1µF
C29 1µF
C30 0.1µF
C31 0.1µF
C32 0.1µF
C1 220µF
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C6 220µF
C7 220µF
C8 220µF
C9 220µF
R24 75Ω
R23 75Ω
R22 75Ω
R21 75Ω
R20 75Ω
R17 75Ω
R16 75Ω
R15 75Ω
R14 75Ω
CVOUT1
CVOUT2 YOUT1
CVOUT2 YOUT1
YOUT2
COUT1
CVOUT+ Y+
BOUT
GOUT
ROUT
SW1-A
SW1-B
SW1-C
JP1
JP2
JP3
JP4
JP5
JP6
HSYNCIN
P2—EVC
P1—SCART

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