Low Power 5V RS232 Dual Driver/Receiver with 0.1µF Capacitors

FEATURES

- ESD Protection over ±**10kV**
- Low Cost
- Uses Small Capacitors: 0.1µF
- CMOS Comparable Low Power: 40mW
- Operates from a Single 5V Supply
- 120kBaud Operation for R_L = 3k, C_L = 2500pF
- 250kBaud Operation for R_L = 3k, C_L = 1000pF
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Powered Down
- Absolutely No Latch-Up
- Available in Narrow SO Package

APPLICATIONS

- Portable Computers
- Battery-Powered Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

The LT1381 is a dual RS232 driver/receiver pair with integral charge pump to generate RS232 voltage levels from a single 5V supply. The circuit features rugged bipolar design to provide operating fault tolerance and ESD protection unmatched by competing CMOS designs. Using only 0.1µF external capacitors, the circuit consumes only 40mW of power and can operate to 120k baud even while driving heavy capacitive loads. New ESD structures on the chip allow the LT1381 to survive multiple ±10kV strikes, eliminating the need for costly TransZorbs® on the RS232 line pins. Driver outputs are protected from overload and can be shorted to ground or up to ±25V without damage. During power-off conditions, driver and receiver outputs are in a high impedance state, allowing line sharing.

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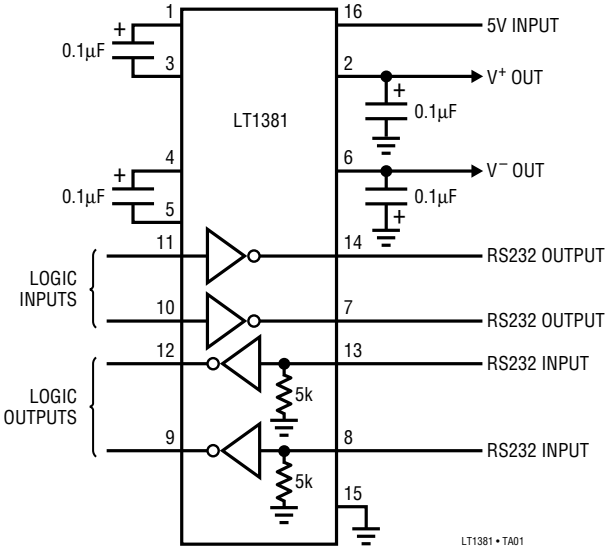
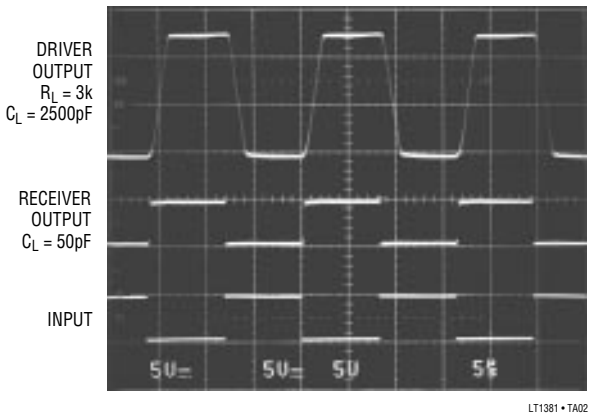
TYPICAL APPLICATION



Output Waveforms



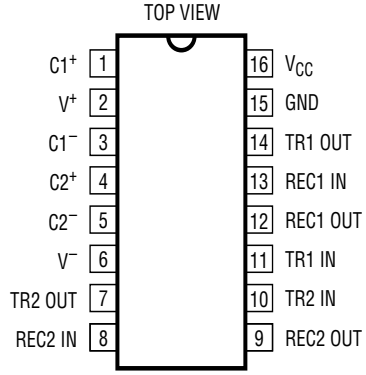
LT1381 • TA02

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
V^+ 13.2V
V^- ..... –13.2V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... –30V to 30V
  ON/$\overline{OFF}$ ..... –0.3V to 12V
Output Voltage
  Driver ..... V^+ – 30V to V^- + 30V
  Receiver ..... –0.3V to V_{CC} + 0.3V
Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1381C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PLASTIC DIP

S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 90°C/W, θ_{JC} = 46°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W, θ_{JC} = 34°C/W (S)

ORDER PART NUMBER
LT1381CN LT1381CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS **(Note 2)**

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output				7.9		V
V^- Output				–7.0		V
Supply Current (V_{CC})	(Note 3), T_A = 25°C			8	14	mA
		●			16	mA
Supply Rise Time	C1 = C2 = C3 = C4 = 0.1µF			0.2		ms
Oscillator Frequency				130		kHz
Driver						
Output Voltage Swing	Load = 3k to GND	Positive ●	5.0	7.5		V
		Negative ●		–6.3	–5.0	V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)	●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)	●	2.0	1.4		V
Logic Input Current	0.8V ≤ V_{IN} ≤ 2.0V	●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V		9	17		mA
Output Leakage Current	Power Off V_{OUT} = ±15V	●		10	100	µA
Data Rate	R_L = 3k, C_L = 2500pF		120			kBaud
	R_L = 3k, C_L = 1000pF		250			kBaud
Slew Rate	R_L = 3k, C_L = 51pF			15	30	V/µs
	R_L = 3k, C_L = 2500pF		4	6		V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 4)			0.6	1.3	µs
	Output Transition t_{LH} Low to High			0.5	1.3	µs

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver						
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High) Input High Threshold (V_{OUT} = Low)		0.8	1.3 1.7	 2.4	V V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = –1.6mA Output High, I_{OUT} = 160µA (V_{CC} = 5V)	● ●	 3.5	0.2 4.2	0.4	V V
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC} Sourcing Current, V_{OUT} = 0V		 10	–20 20	–10	mA mA
Propagation Delay	Output Transition t_{HL} High-to-Low (Note 5) Output Transition t_{LH} Low-to-High			250 350	600 600	ns ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V, unless otherwise specified.

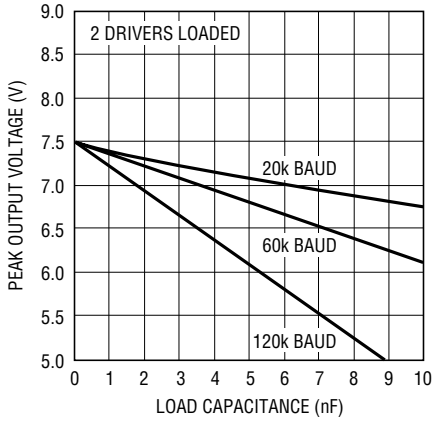
Note 3: Supply current is measured as the average over several charge pump cycles. $C^+ = C^- = C1 = C2 = 0.1\mu F$. All outputs are open, with all driver inputs tied high.

Note 4: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

Note 5: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

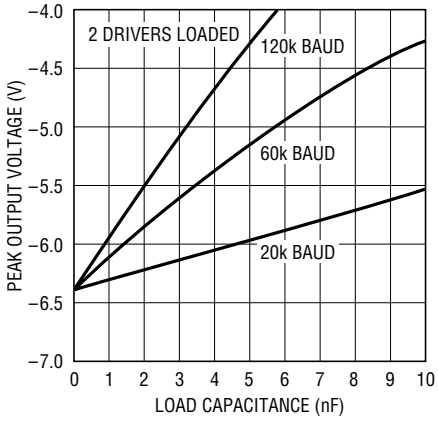
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Maximum Output Voltage vs Load Capacitance



LT1381 • TPC01

Driver Minimum Output Voltage vs Load Capacitance



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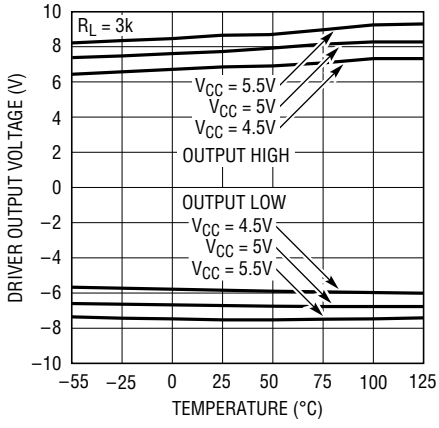
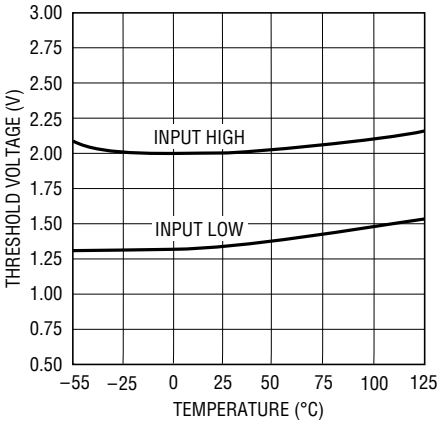
Driver Output Voltage



LT1381 • TPC03

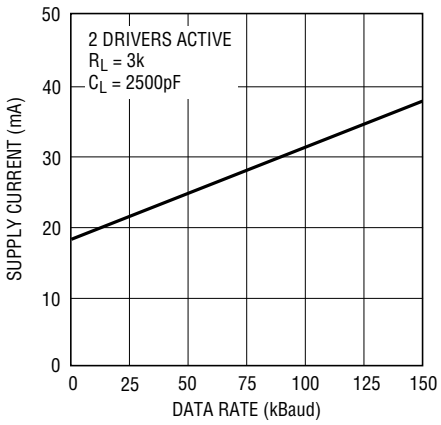
TYPICAL PERFORMANCE CHARACTERISTICS

Receiver Input Threshold



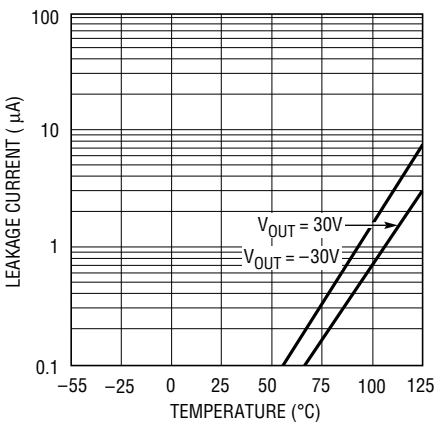
LT1381 • TPC04

Supply Current vs Data Rate



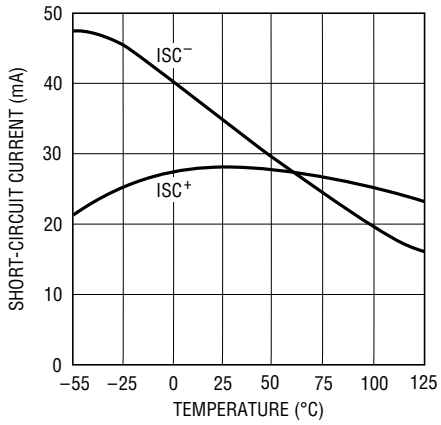
LT1381 • TPC05

Driver Leakage in Shutdown



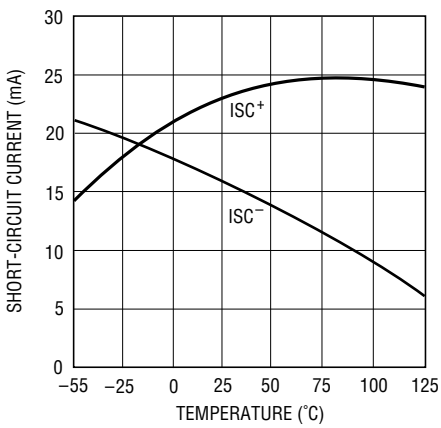
LT1381 • TPC06

Receiver Short-Circuit Current



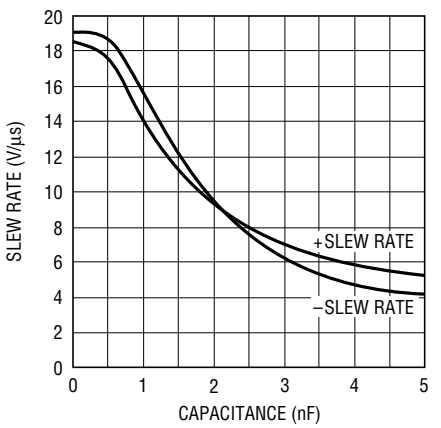
LTLT1381 • TPC07

Driver Short-Circuit Current



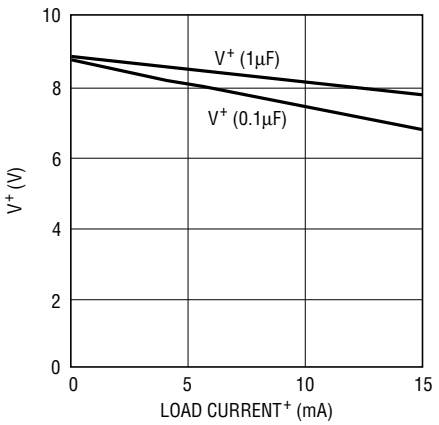
LT1381 • TPC08

Slew Rate vs Load Capacitance



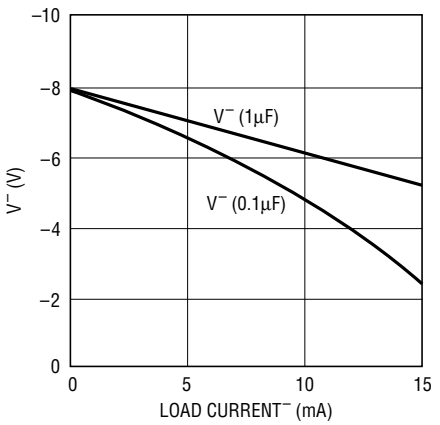
LT1381 • TPC09

V+ Compliance Curve



LT1381 • TPC10

V– Compliance Curve



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PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. This pin should be decoupled with a 0.1μF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

GND: Ground Pin.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$, tied to ground or V_{CC}. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors.

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors.

TR1 IN, TR2 IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT, TR2 OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when V_{CC} = 0V. Outputs are fully short-circuit protected from $V^- + 25V$ to $V^+ - 25V$. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

REC1 IN, REC2 IN: Receiver Inputs. These pins accept RS232 level signals (±30V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

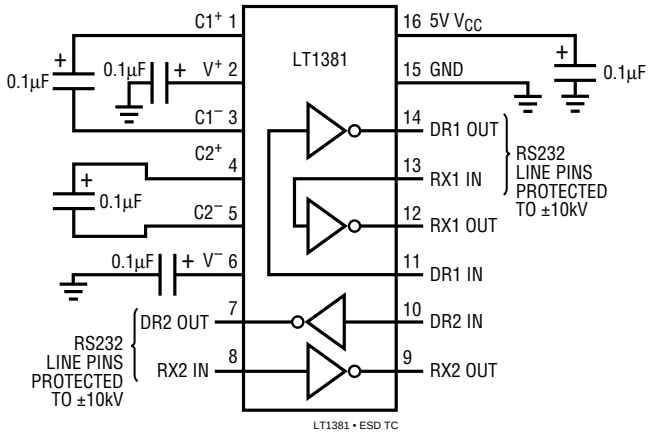
REC1 OUT, REC2 OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are fully short-circuit protected to ground or V_{CC} with the power ON or OFF.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.1\mu F$: one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. C1 may be deleted if a separate 12V supply is available and connected to pin $C1^+$.

ESD PROTECTION

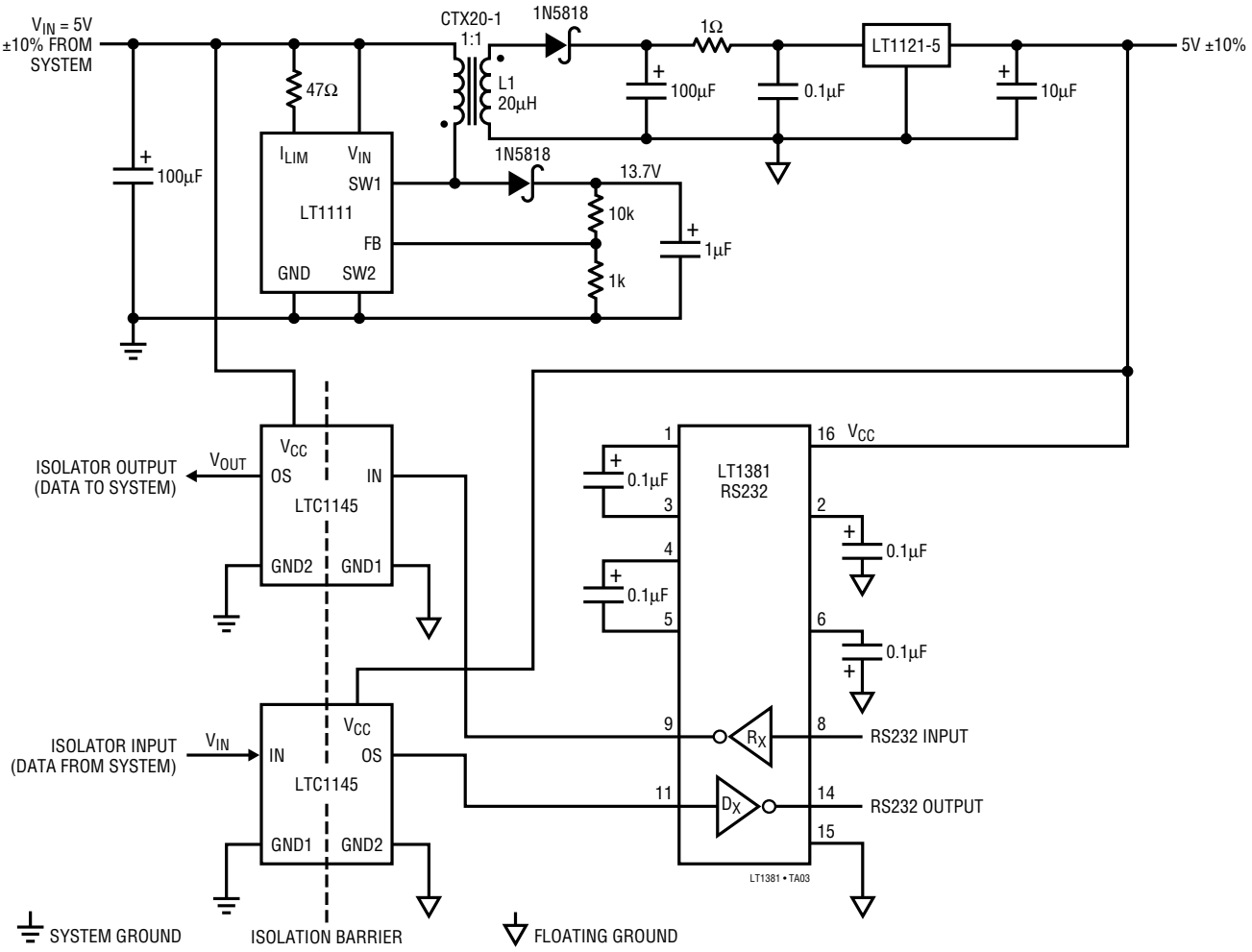
The RS232 line inputs of the LT1381 have on-chip protection from ESD transients up to ±10kV. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the circuit must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V^+, V^- and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit

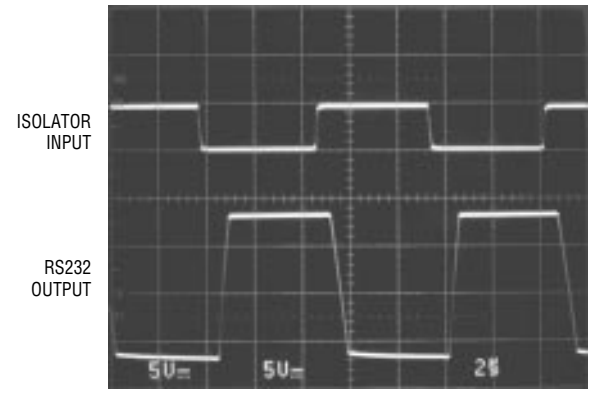


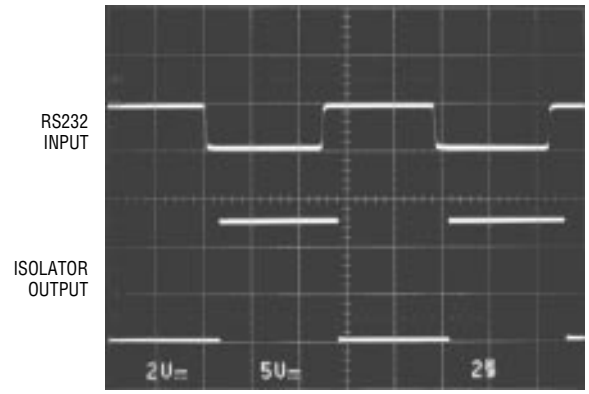
TYPICAL APPLICATIONS

Isolated RS232 Driver/Receiver



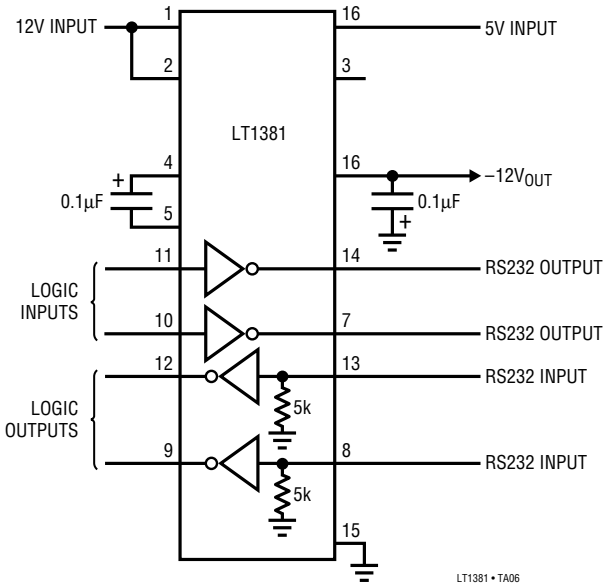
Data Transmission Across Isolation Barrier



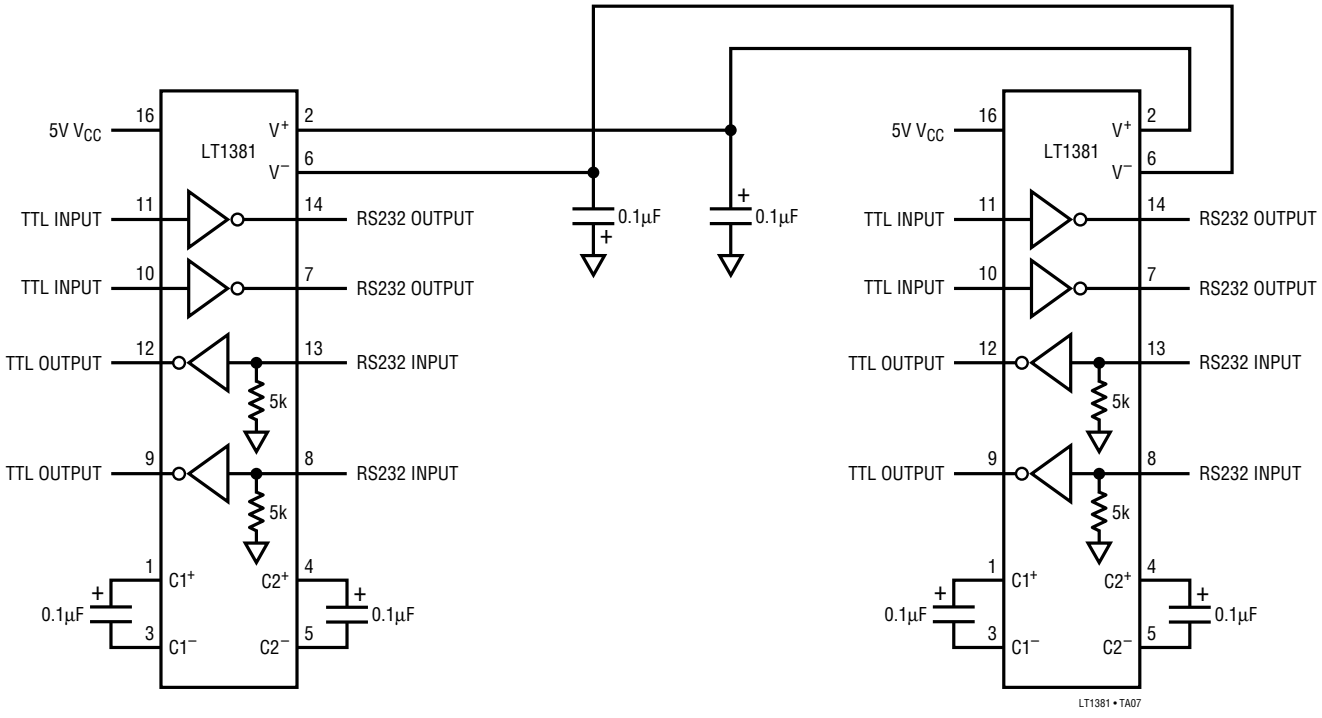


TYPICAL APPLICATIONS

Operation Using 5V and 12V Power Supplies



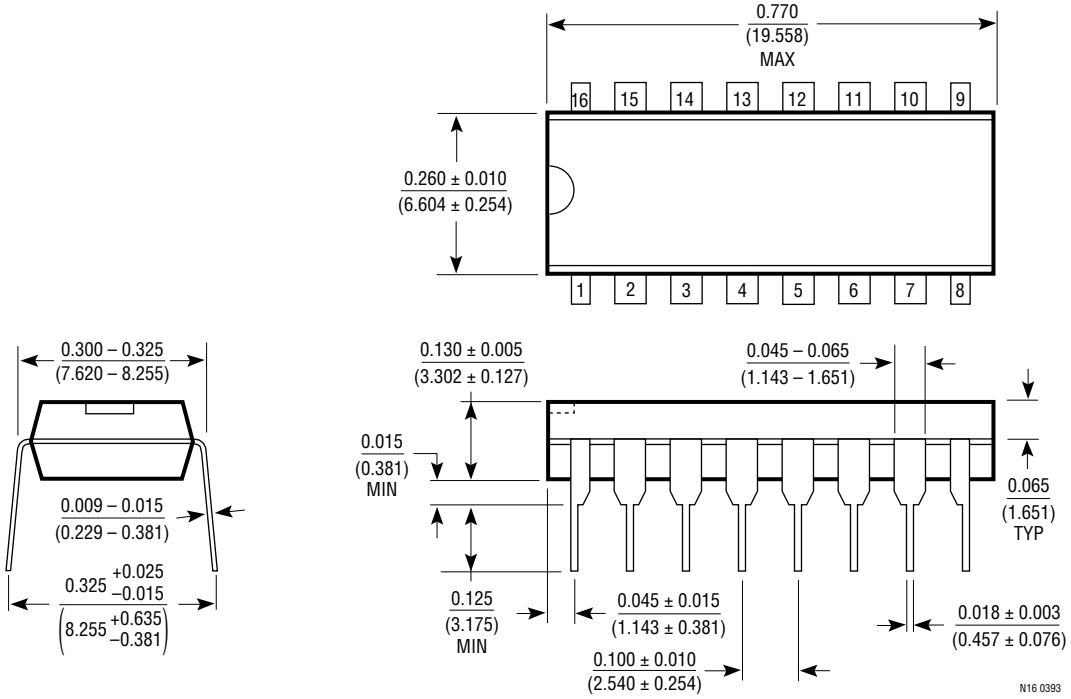
Sharing Capacitors



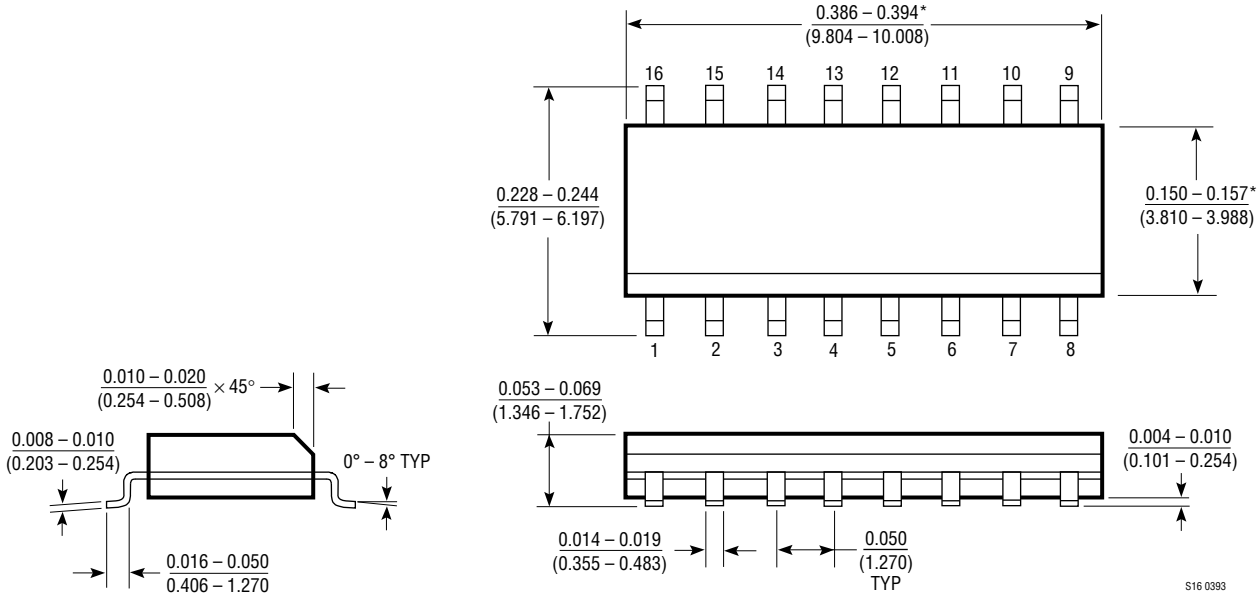
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead Plastic DIP



S Package
16-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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LT/GP 0593 10K REV 0