Integrated
Circuit
Systems, Inc.

ICS8701

LOW SKEW, ÷1, ÷2
LVCMOS CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS8701 is a low skew, ÷1, ÷2 LVCMOS Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 20 to 40 by utilizing the ability of the outputs to drive two series terminated lines.

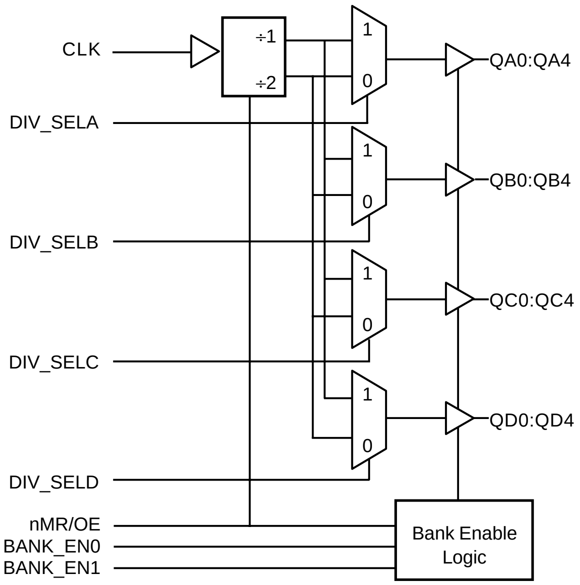
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The bank enable inputs, BANK_EN0:1, support enabling and disabling each bank of outputs individually. The master reset input, nMR/OE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS8701 is characterized at 3.3V and mixed 3.3V input supply, and 2.5V output supply operating modes. Guaranteed bank, output and part-to-part skew characteristics make the ICS8701 ideal for those clock distribution applications demanding well defined performance and repeatability.

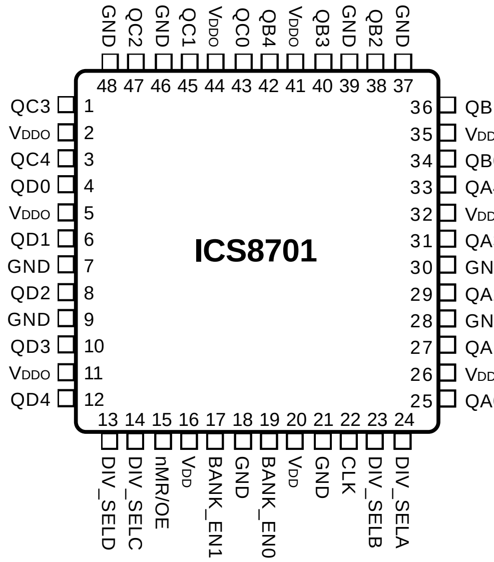
FEATURES

- 20 LVCMOS outputs, 7Ω typical output impedance
- 1 LVCMOS clock input
- Maximum output frequency: 250MHz
- Bank enable logic allows unused banks to be disabled in reduced fanout applications
- Output skew: 250ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Bank skew: 200ps (maximum)
- Multiple frequency skew: 300ps (maximum)
- 3.3V or mixed 3.3V input, 2.5V output operating supply modes
- 0°C to 70°C ambient operating temperature
- Other divide values available on request

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Pin LQFP
7mm x 7mm x 1.4mm
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
2, 5, 11, 26, 32, 35, 41, 44	V_{DDO}	Power		Output supply pins.
7, 9, 18, 21, 28, 30, 37, 39, 46, 48	GND	Power		Power supply ground.
16, 20	V_{DD}	Power		Positive supply pins.
25, 27, 29, 31, 33	QA0, QA1, QA2, QA3, QA4	Output		Bank A outputs.LVCMOS / LVTTLinterface levels. 7Ω typical output impedance.
34, 36, 38, 40, 42	QB0, QB1, QB2, QB3, QB4	Output		Bank B outputs.LVCMOS / LVTTLinterface levels. 7Ω typical output impedance.
43, 45, 47, 1, 3	QC0, QC1, QC2, QC3, QC4	Output		Bank C outputs.LVCMOS / LVTTLinterface levels. 7Ω typical output impedance.
4, 6, 8, 10, 12	QD0, QD1, QD2, QD3, QD4	Output		Bank D outputs. LVCMOS / LVTTLinterface levels. 7Ω typical output impedance.
22	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
13	DIV_SELD	Input	Pullup	Controls frequency division for Bank D outputs. LVCMOS / LVTTLinterface levels.
14	DIV_SELC	Input	Pullup	Controls frequency division for Bank C outputs. LVCMOS / LVTTLinterface levels.
23	DIV_SELB	Input	Pullup	Controls frequency division for Bank B outputs. LVCMOS / LVTTLinterface levels.
24	DIV_SELA	Input	Pullup	Controls frequency division for Bank A outputs. LVCMOS / LVTTLinterface levels.
17, 19	BANK_EN1, BANK_EN0	Input	Pullup	Enables and disables outputs by banks. LVCMOS / LVTTLinterface levels.
15	nMR/OE	Input	Pullup	Master Reset and output enable. When HIGH, output drivers are enabled. Whe LOW, output drivers are in HiZ and dividers are reset. LVCMOS / LVTTLinterface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V			15	pF
R_{OUT}	Output Impedance			7		Ω

TABLE 3. FUNCTION TABLE

Inputs				Outputs				
nMR/OE	**BANK_EN1**	**BANK_EN0**	**DIV_SELx**	**QA0:QA4**	**QB0:QB4**	**QC0:QC4**	**QD0:QD4**	**Qx Frequency**
0	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	zero
1	0	0	0	Active	Hi Z	Hi Z	Hi Z	fIN/2
1	1	0	0	Active	Active	Hi Z	Hi Z	fIN/2
1	0	1	0	Active	Active	Active	Hi Z	fIN/2
1	1	1	0	Active	Active	Active	Active	fIN/2
1	0	0	1	Active	Hi Z	Hi Z	Hi Z	fIN
1	1	0	1	Active	Active	Hi Z	Hi Z	fIN
1	0	1	1	Active	Active	Active	Hi Z	fIN
1	1	1	1	Active	Active	Active	Active	fIN

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DDx}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V\pm5\%$, TA =0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				95	mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V\pm5\%$, TA =0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE		2		V_{DD} + 0.3	V
		CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE		-0.3		0.8	V
		CLK		-0.3		1.3	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	$V_{DD} = V_{IN} = 3.465V$			5	µA
		CLK	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
		CLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage		$V_{DD} = V_{DDO} = 3.135V$ $I_{OH} = -36mA$	2.6			V
V_{OL}	Output Low Voltage		$V_{DD} = V_{DDO} = 3.135V$ $I_{OL} = 36mA$			0.5	V

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, TA =0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 200MHz	2.2		3.4	ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDO}/2$			200	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDO}/2$			250	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDO}/2$			300	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDO}/2$			600	ps
t_R	Output Rise Time; NOTE 6	30% to 70%	280		850	ps
t_F	Output Fall Time; NOTE 6	30% to 70%	280		850	ps
odc	Output Duty Cycle	f ≤ 200MHz	tCYCLE/2 - 0.5	tCYCLE/2	tCYCLE/2 + 0.5	ns
		f = 200MHz	2	2.5	3	ns
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz			6	ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz			6	ns

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{DDO}/2$.

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				95	mA

TABLE 4D. LVCMOS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE		2		V_{DD} + 0.3	V
		CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE		-0.3		0.8	V
		CLK		-0.3		1.3	V
I_{IH}	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	V_{DD} = V_{IN} = 3.465V			5	µA
		CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage		V_{DD} = 3.135V, V_{DDO} = 2.375 I_{OH} = -27mA	1.8			V
V_{OL}	Output Low Voltage		V_{DD} = 3.135V, V_{DDO} = 2.375 I_{OL} = 27mA			0.5	V

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 200MHz	2.6		3.6	ns
*t*sk(b)	Bank Skew; NOTE 2, 7	Measured on rising edge atV_{DDO}/2			225	ps
*t*sk(o)	Output Skew; NOTE 3, 7	Measured on rising edge atV_{DDO}/2			250	ps
*t*sk(w)	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge atV_{DDO}/2			300	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 5, 7	Measured on rising edge atV_{DDO}/2			600	ps
t_R	Output Rise Time; NOTE 6	30% to 70%	280		850	ps
t_F	Output Fall Time; NOTE 6	30% to 70%	280		850	ps
odc	Output Duty Cycle	f ≤ 200MHz	tCYCLE/2 - 0.5	tCYCLE/2	tCYCLE/2 + 0.5	ns
		f = 200MHz	2	2.5	3	ns
t_{EN}	Output Enable Time; NOTE 6	f = 10MHz			6	ns
t_{DIS}	Output Disable Time; NOTE 6	f = 10MHz			6	ns

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.

NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.

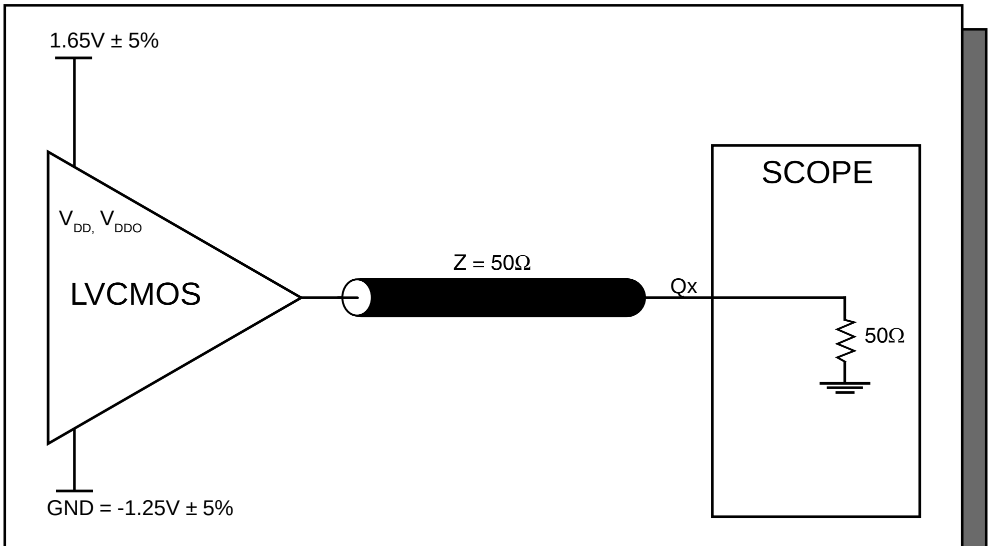
NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at V_{DDO}/2.

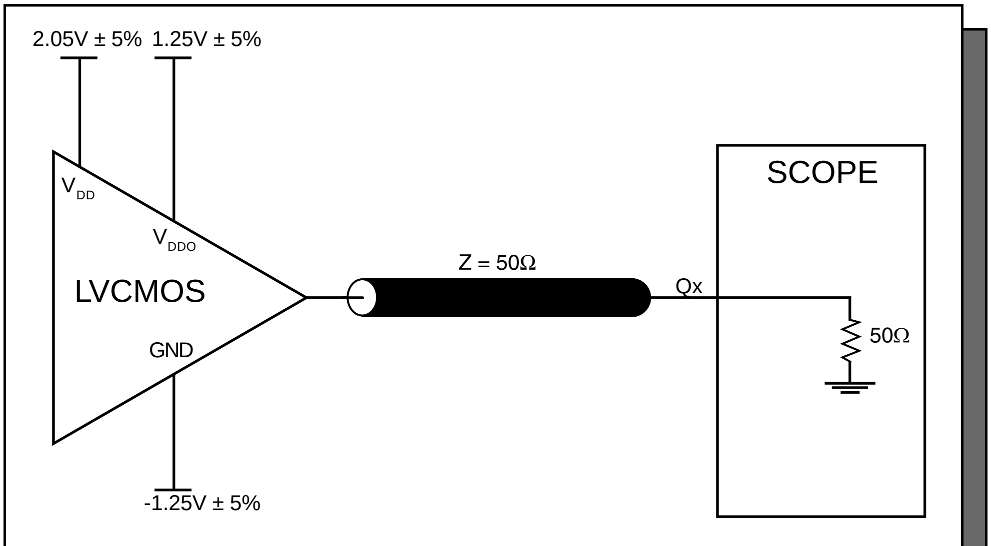
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

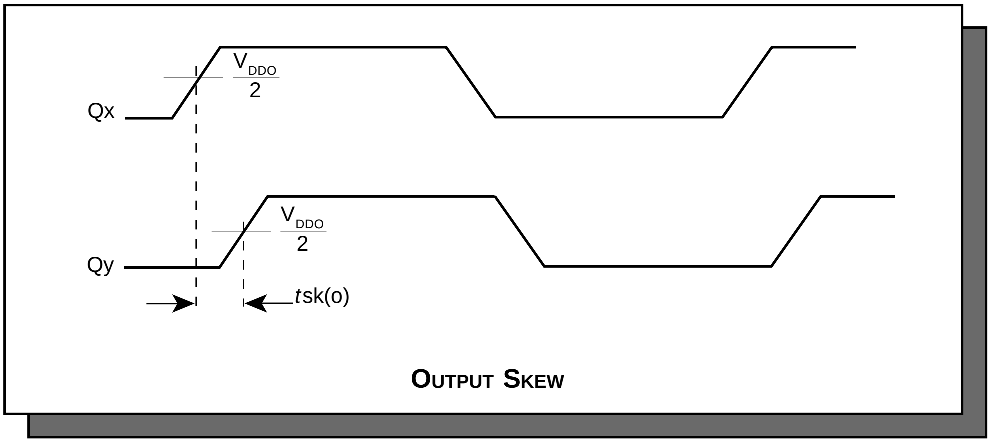
PARAMETER MEASUREMENT INFORMATION



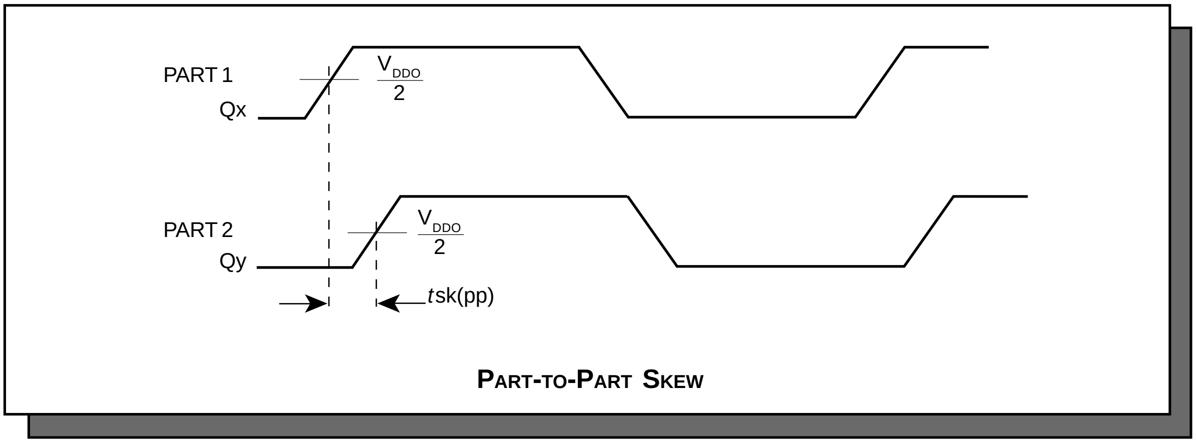
3.3V OUTPUT LOAD TEST CIRCUIT



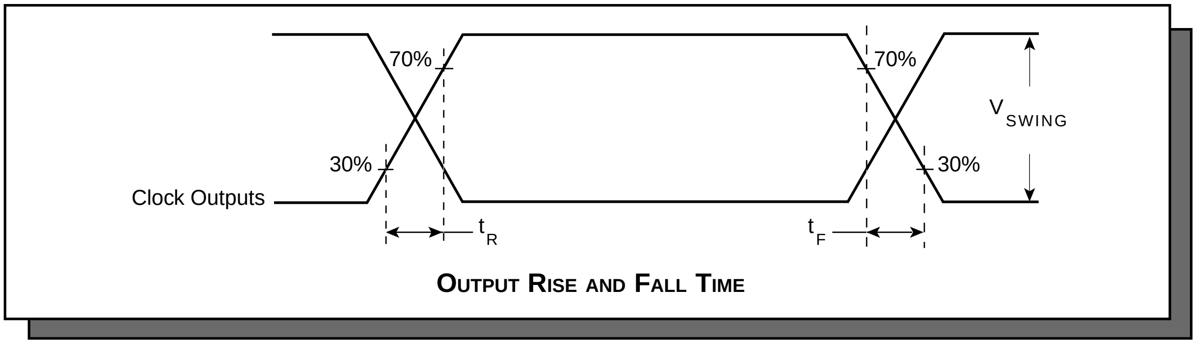
3.3V/2.5 OUTPUT LOAD TEST CIRCUIT



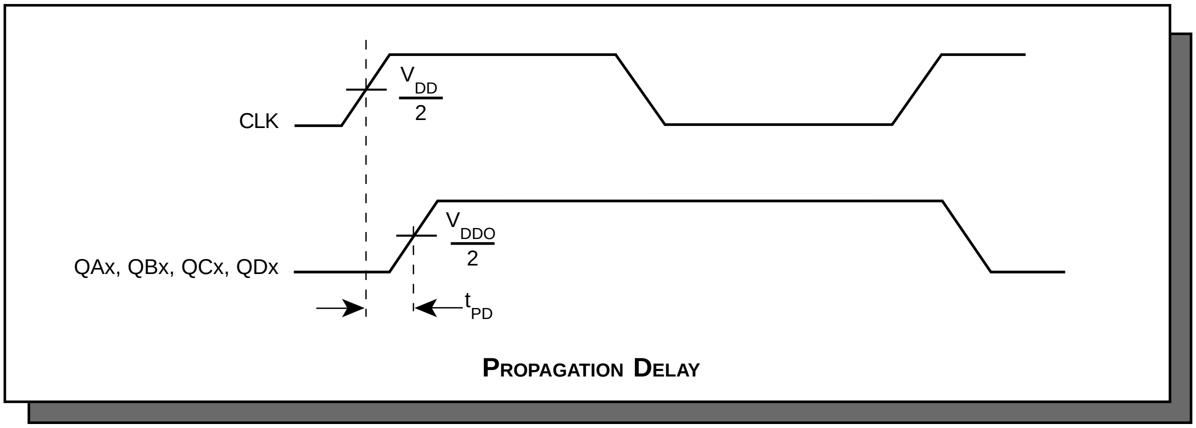
OUTPUT SKEW



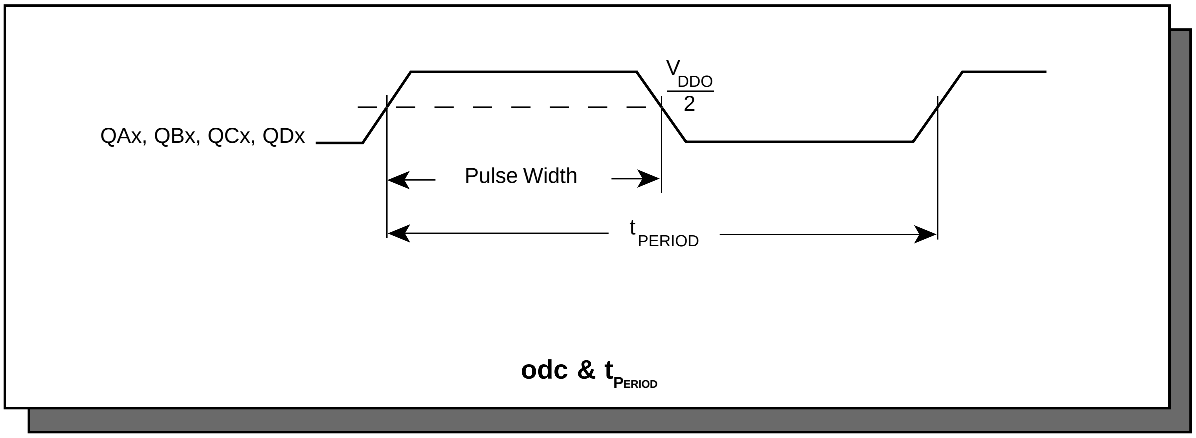
PART-TO-PART SKEW



OUTPUT RISE AND FALL TIME



PROPAGATION DELAY



odc & t_{PERIOD}

POWER CONSIDERATIONS

For Power Dissipation, please refer to a separate Application Note: *Power Dissipation for LVCMOS Buffer.*

DRIVER TERMINATION

For LVCMOS Output Termination, please refer to a separate Application Note: *LVCMOS Driver Termination.*

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS8701 is: 1743

PACKAGE OUTLINE - Y SUFFIX

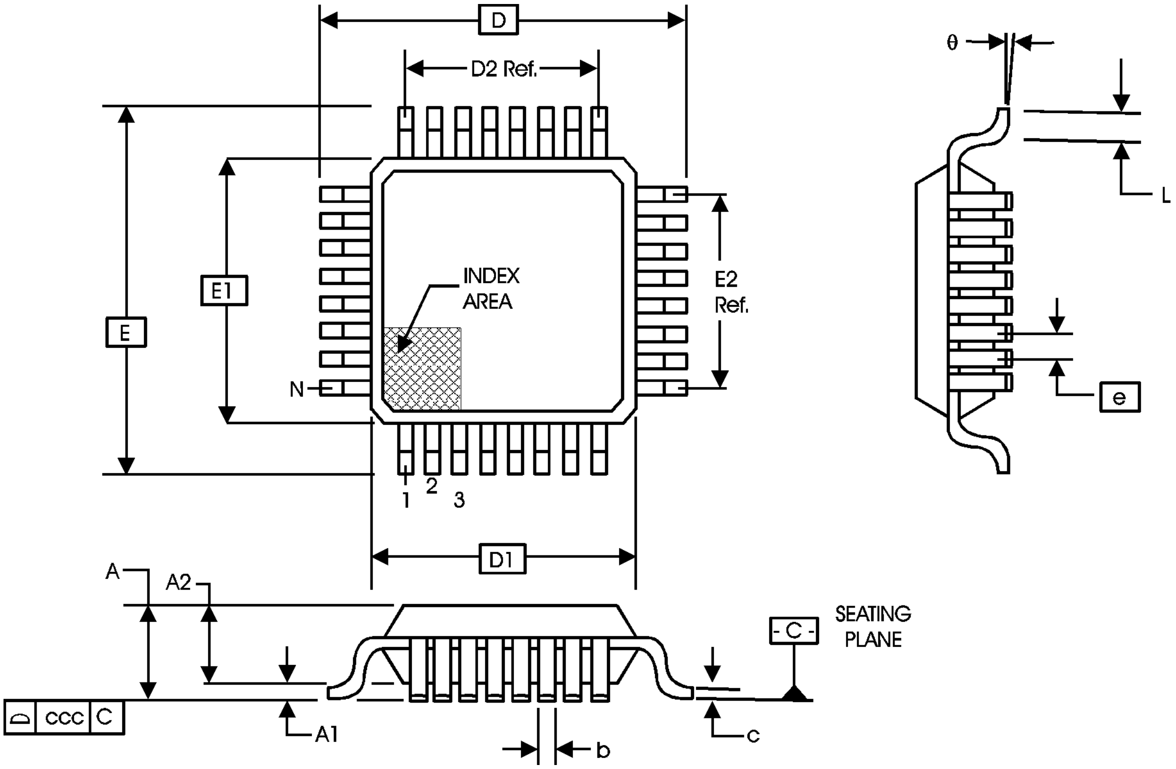


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	**BBC**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N	48		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 Ref.		
e	0.50 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8701CY	ICS8701CY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8701CYT	ICS8701CY	48 Lead LQFP on Tape and Reel	1000	0°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	5A 5B	5 7 8 - 10	Updated notes. Updated notes. Updated drawings.	10/4/01
C	4B 4D	4 6 11	Revised V_{IH} rows from 3.8 Maximum to V_{DD} + 0.3 Maximum. Revised V_{IH} rows from 3.8 Maximum to V_{DD} + 0.3 Maximum. Added Power Dissipation and Driver Termination notes.	11/28/01
C	1	2 9	Pin Description Table, revised nMR/OE description. Updated Output Rise/Fall Time Diagram.	8/19/02