PRELIMINARY

Integrated Circuit Systems, Inc.

ICS84426
CRYSTAL-TO-LVDS SERIAL ATTACHED SCSI CLOCK SYNTHESIZER/FANOUT BUFFER

GENERAL DESCRIPTION

HiPerClockS™

The ICS84426 is a Crystal-to-LVDS Clock Synthesizer/Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The VCO and output frequency can be programmed using the frequency select pins. The low jitter characteristics of the ICS84426 make it an ideal clock source for Serial Attached SCSI applications.

FUNCTION TABLE

Inputs		Output Frequency
MR	F_SEL	F_OUT
1	X	LOW
0	0	75MHz
0	1	150MHz

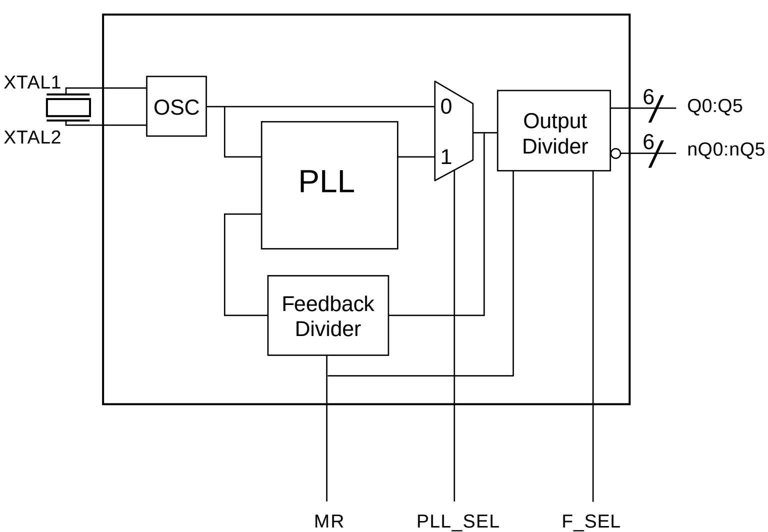
FEATURES

- 6 LVDS outputs
- Crystal oscillator interface
- Output frequency range: 75MHz to 150MHz
- Crystal input frequency: 25MHz
- Cycle-to-cycle jitter: 20ps (typical)
- RMS phase jitter at 150MHz, using a 25MHz crystal (899.9KHz to 20MHz): TBD
- Phase noise: TBD

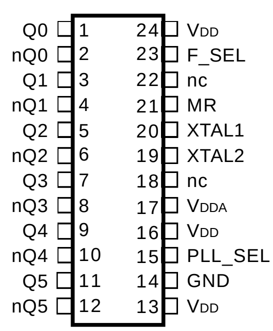
Offset	Noise Power
100Hz	TBD
1KHz	TBD
10KHz	TBD
100KHz	TBD

- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS84426
24-Lead, 300-MIL SOIC
7.5mm x 15.33mm x 2.3mm body package
M Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVDS interface levels.
5, 6	Q2, nQ2	Output		Differential output pair. LVDS interface levels.
7, 8	Q3, nQ3	Output		Differential output pair. LVDS interface levels.
9, 10	Q4, nQ4	Output		Differential output pair. LVDS interface levels.
11, 12	Q5, nQ5	Output		Differential output pair. LVDS interface levels.
13, 16, 24	V_{DD}	Power		Core supply pins.
14	GND			Power supply ground.
15	PLL_SEL	Input	Pullup	Selects between the PLL and crystal inputs as the input to the dividers. When HIGH, selects PLL. When LOW, selects XTAL1, XTAL2. LVCMOS / LVTTL interface levels.
17	V_{DDA}	Power		Analog supply pin.
18, 22	nc	Unused		No connect.
19, 20	XTAL2, XTAL1	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
21	MR	Input	Pulldown	Active High Master Reset. When logic LOW, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic HIGH, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
23	F_SEL	Input	Pullup	Output frequency select pin. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	50°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V\pm5\%$, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			242		mA
I_{DDA}	Analog Supply Current			19		mA

TABLE 3B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V\pm5\%$, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	PLL_SEL, MR, F_SEL		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	PLL_SEL, MR, F_SEL		-0.3		0.8	V
I_{IH}	Input High Current	MR	$V_{DD} = V_{IN} = 3.465V$			150	µA
		PLL_SEL, F_SEL	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	MR	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL, F_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA

TABLE 3C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V\pm5\%$, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250	400	600	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage			1.4		V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 4. CRYSTAL CHARACTERISTICS

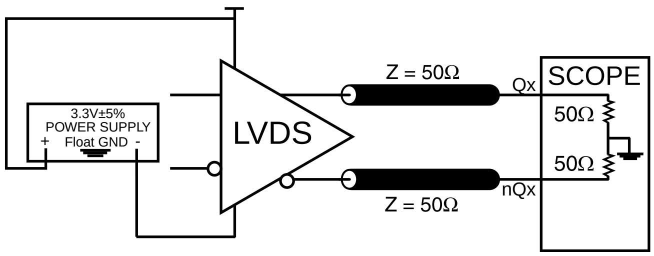
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance				7	pF

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

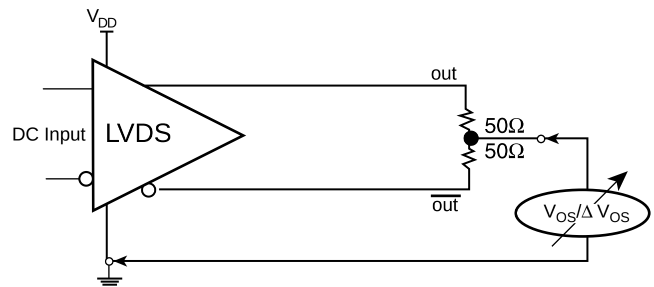
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		75		150	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2			20		ps
*t*jit(per)	Period Jitter, RMS			TBD		ps
*t*sk(o)	Output Skew; NOTE 1, 2			40		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				1	ms

See Parameter Measurement Information section.
NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crossing points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

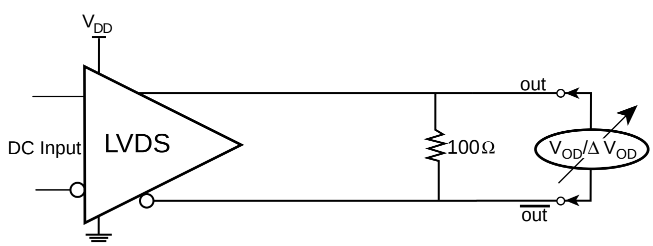
PARAMETER MEASUREMENT INFORMATION



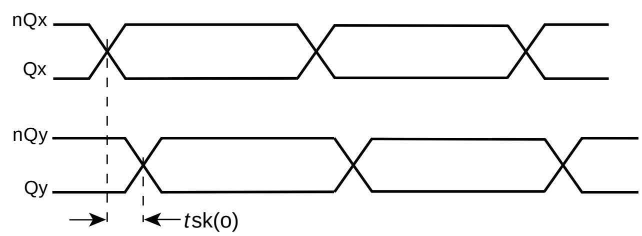
3.3V OUTPUT LOAD AC TEST CIRCUIT



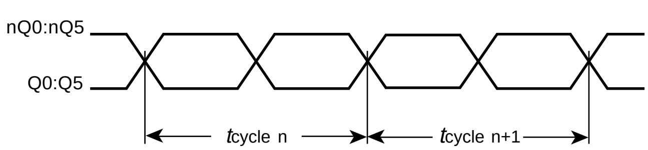
V_{OS} / ΔVOS SETUP



V_{OD} / ΔVOD SETUP



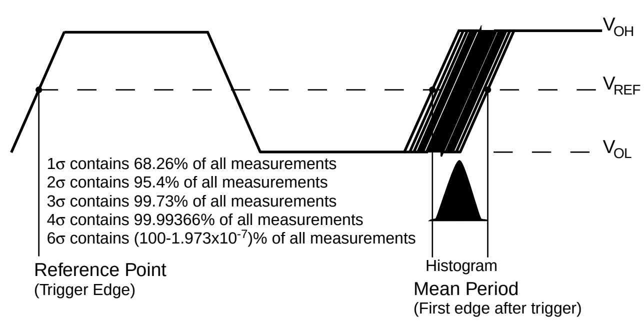
OUTPUT SKEW



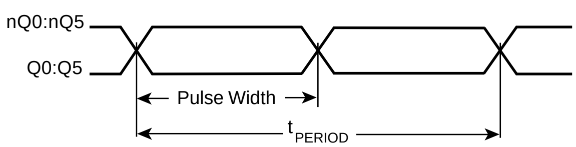
$$t_{jit}(cc) = t_{cycle\ n} - t_{cycle\ n+1}$$

1000 Cycles

CYCLE-TO-CYCLE JITTER

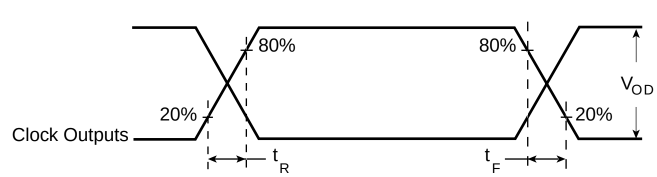


PERIOD JITTER



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

odc & t_{PERIOD}



OUTPUT RISE/FALL TIME

APPLICATIONS INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS84426 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 24Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

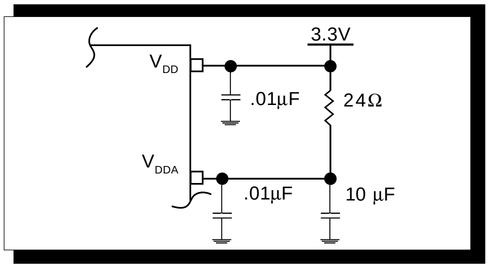


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS84426 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

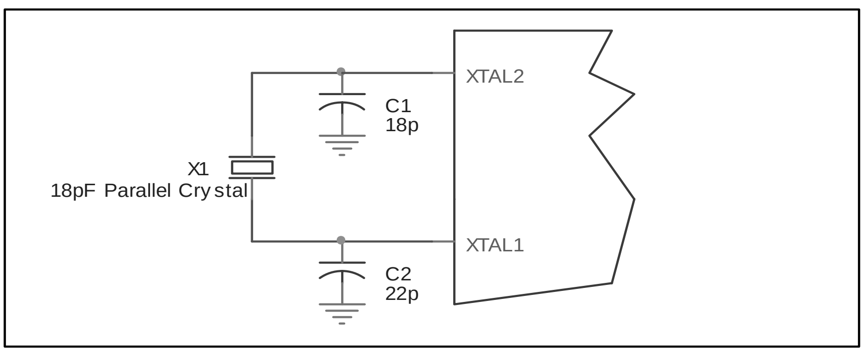


Figure 2. CRYSTAL INPUT INTERFACE

LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

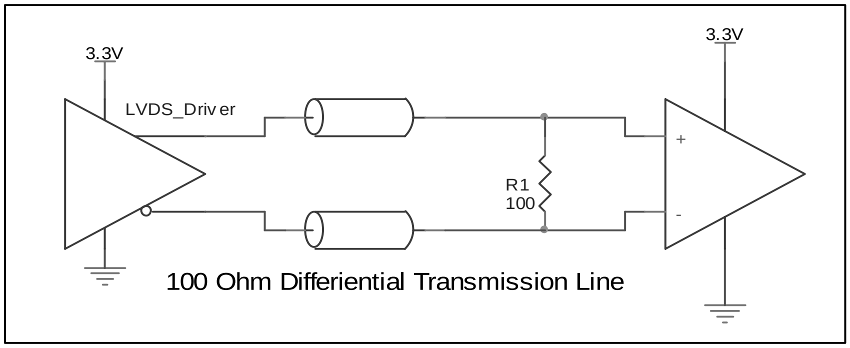


FIGURE 3. TYPICAL LVDS DRIVER TERMINATION

SCHEMATIC EXAMPLE

Figure 4A shows a schematic example of using an ICS84426. In this example, the input is a 25MHz parallel resonant crystal with load capacitor CL=18pF. The frequency fine tuning capacitors C1 and C2 is 22pF and 18pF respectively. This example also shows logic control input handling. The configuration is set at F_SEL=1, therefore, the output frequency is 75MHz. It is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as possible to the power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the V_{DDA} pin as possible. For LVDS driver, the unused output pairs should be terminated with a 100Ω resistor across.

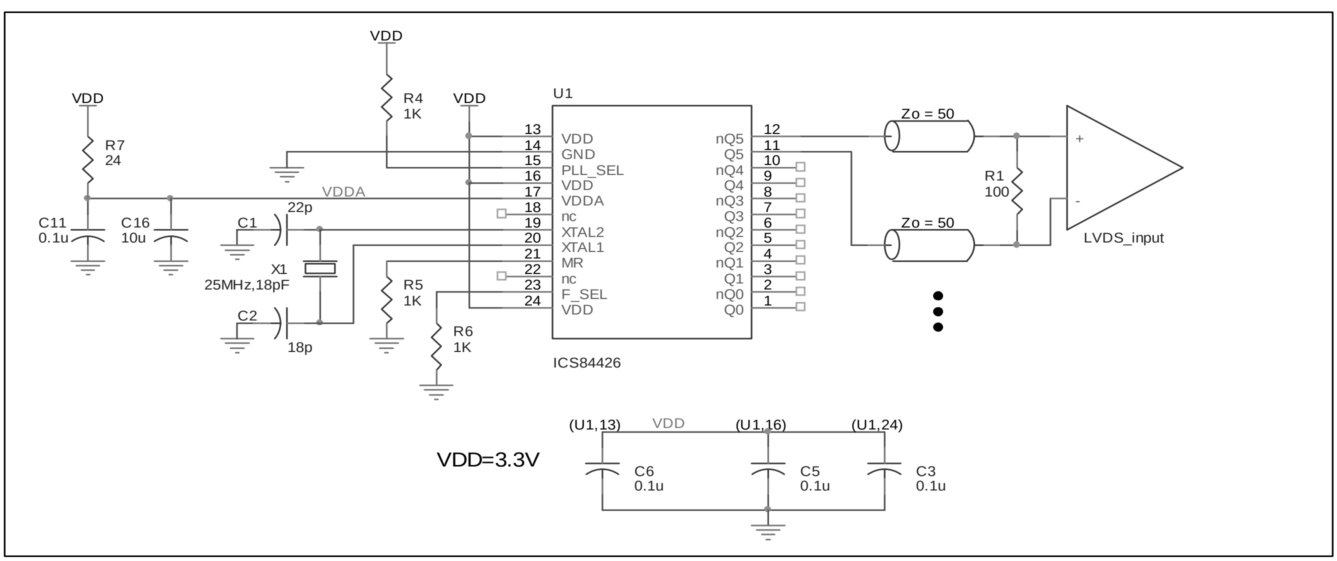


FIGURE 4A. ICS84426 SCHEMATIC EXAMPLE

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors C3, C5 and C6, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

CRYSTAL

The crystal X1 should be located as close as possible to the pins 20 (XTAL1) and 19 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

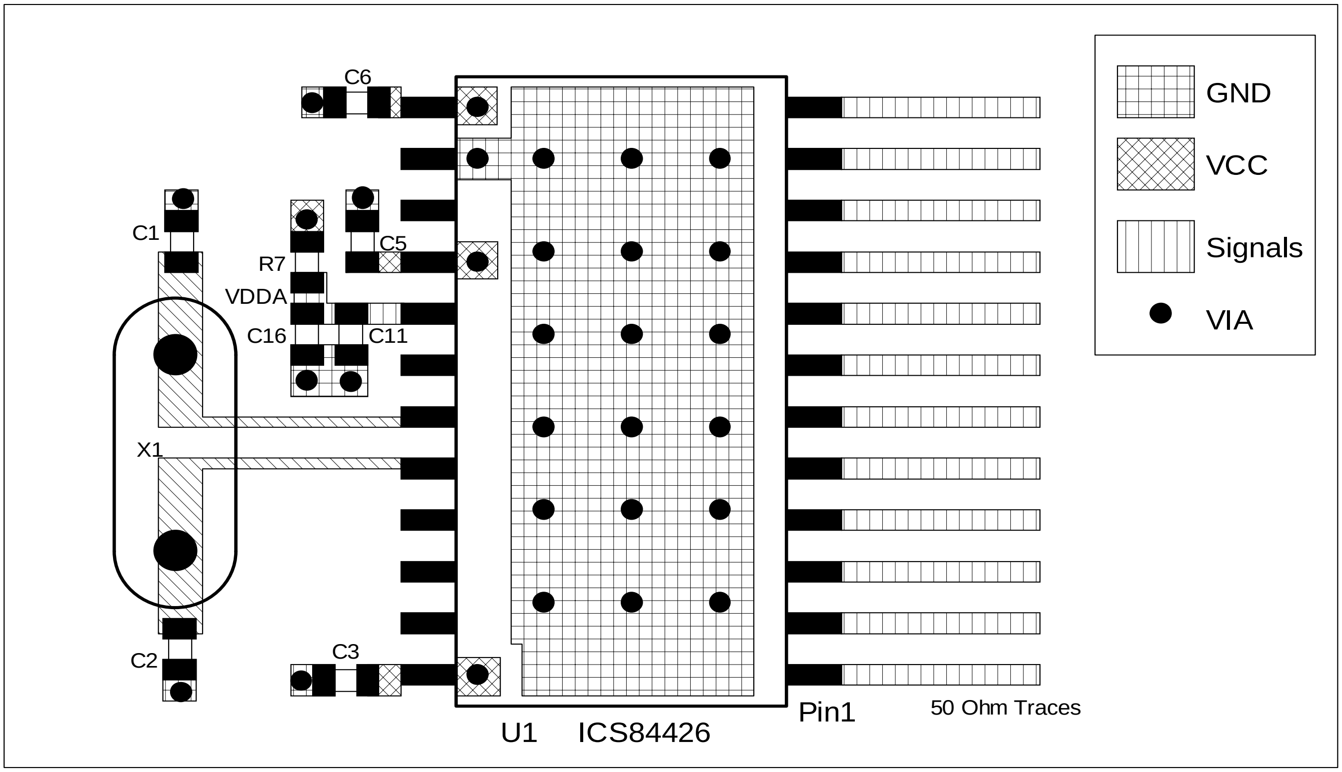


FIGURE 4B. PCB BOARD LAYOUT FOR ICS84426

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	50°C/W	43°C/W	38°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS84426 is: 2804

PACKAGE OUTLINE - M SUFFIX

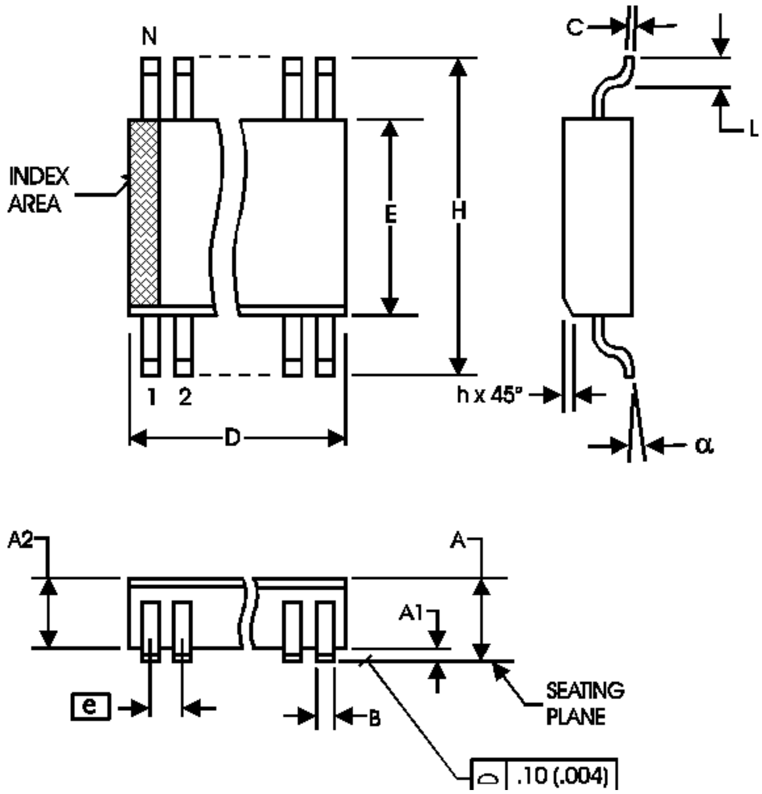


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	15.20	15.85
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS84426BM	ICS84426BM	24 Lead SOIC	30 per tube	0°C to 70°C
ICS84426BMT	ICS84426BM	24 Lead SOIC on Tape and Reel	1000	0°C to 70°C

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