PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8431I-21

350MHz, Low Jitter, Crystal Oscillator-to-3.3V LVPECL Frequency Synthesizer

General Description

The ICS8431I-21 is a general purpose clock frequency synthesizer for IA64/32 application and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The VCO operates at a frequency range of 250MHz to 700MHz providing an output frequency range of 62.5MHz to 350MHz. The output frequency can be programmed using the parallel interface, M0 through M8 to the configuration logic, and the output divider control pin, DIV_SEL. Spread spectrum clocking is programmed via the control inputs SSC_CTL0 and SSC_CTL1.

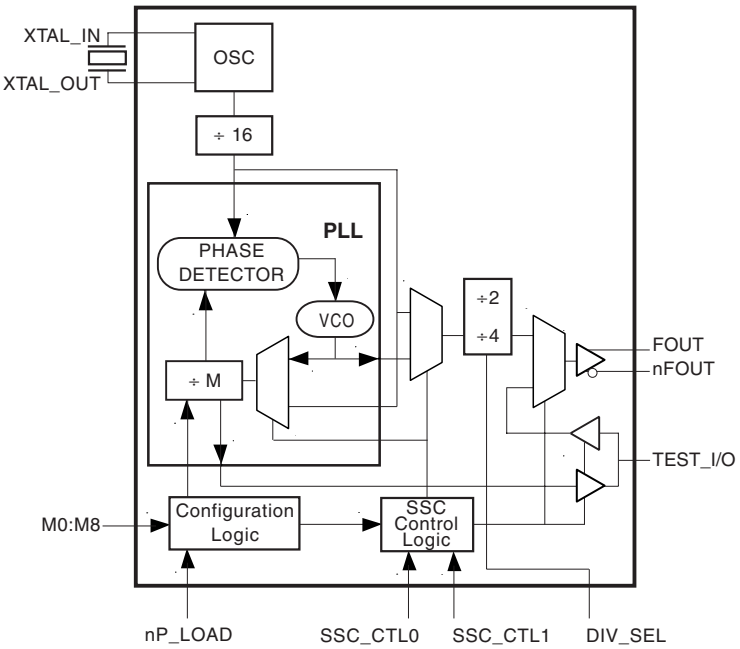
Programmable features of the ICS8431I-21 support four operational modes. The four modes are spread spectrum clocking (SSC), non-spread spectrum clock and two test modes which are controlled by the SSC_CTL[1:0] pins. Unlike other synthesizers, the ICS8431I-21 can immediately change spread-spectrum operation without having to reset the device.

In SSC mode, the output clock is modulated in order to achieve a reduction in EMI. In one of the PLL bypass test modes, the PLL is disconnected as the source to the differential output allowing an external source to be connected to the TEST_I/O pin. This is useful for in-circuit testing and allows the differential output to be driven at a lower frequency throughout the system clock tree. In the other PLL bypass mode, the oscillator divider is used as the source to both the M and the Fout divide by 2. This is useful for characterizing the oscillator and internal dividers.

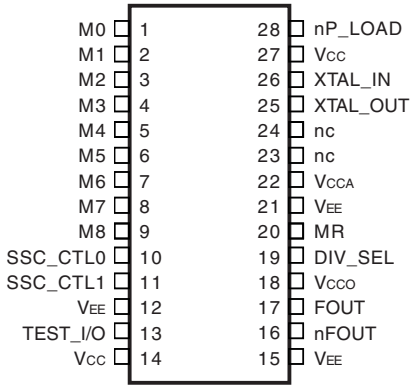
Features

- Fully integrated PLL
- Differential 3.3V LVPECL output
- Crystal oscillator interface
- Output frequency range: 62.5MHz to 350MHz
- Crystal input frequency range: 14MHz to 25MHz
- VCO range: 250MHz to 700MHz
- Programmable PLL loop divider for generating a variety of output frequencies
- Spread Spectrum Clocking (SSC) fixed at 1/2% modulation for environments requiring ultra low EMI
- PLL bypass modes supporting in-circuit testing and on-chip functional block characterization
- Cycle-to-cycle jitter: 19ps (typical)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Replaces ICS8431I-01

Block Diagram



Pin Assignment



ICS8431I-21
28-Lead SOIC
7.5mm x 18.05mm x 2.25mm package body
M Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

Functional Description

The ICS8431I-21 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 250MHz to 700MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to the LVPECL output buffer. The divider provides a 50% output duty cycle.

The programmable features of the ICS8431I-21 support four output operational modes and a programmable M divider and output divider. The four output operational modes are spread spectrum clocking (SSC), non-spread spectrum clock and two test modes and are controlled by the SSC_CTL[1:0] pins.

The PLL loop divider or M divider is programmed by using inputs M0 through M8. While the nP_LOAD input is held LOW, the data present at M0:M8 is transparent to the M divider. On the LOW-to-HIGH transition of nP_LOAD, the M0:M8 data is latched into the M divider and any further changes at the M0:M8 inputs will not be seen by the M divider until the next LOW transition on nP_LOAD.

The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fxtal}{16} \times M$$

The M value and the required values of M0:M8 for programming the VCO are shown in *Table 3B*, Programmable VCO Frequency Function Table. The frequency out is defined as follows:

$$FOUT = \frac{fVCO}{N} = \frac{fxtal \times M}{16 \times N}$$

For the ICS8431I-21, the output divider may be set to either ÷2 or ÷4 by the DIV_SEL pin. For an input of 16 MHz, valid M values for which the PLL will achieve lock are defined as: $250 \leq M \leq 511$.

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 3, 4, 5, 6, 7	M0-M6	Input	Pulldown	M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS / LVTTL pins interface levels.
8, 9	M7-M8	Input	Pullup	
10, 11	SSC CTL0, SSC CTL1	Input	Pullup	SCC control pins. LVTTL / LVCMOS interface levels.
12, 15, 21	V_{EE}	Power		Negative supply pins. Connect all V_{EE} pins to board ground.
13	TEST I/O	Input / Output		Programmed as defined in Table 3A Function Table.
14, 27	V_{CC}	Power		Core supply pin.
16, 17	nFOUT, FOUT	Output		Differential outputs for the synthesizer. 3.3V LVPECL interface levels.
18	V_{CCO}	Power		Output supply pin.
19	DIV_SEL	Input	Pulldown	Determines the output divide value for FOUT. LVCMOS / LVTTL interface levels.
20	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output FOUT to go low and the inverted output nFOUT to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not effect loaded M and T values. LVCMOS / LVTTL interface levels.
22	V_{CCA}	Power		Analog supply pin.
23, 24	nc	Unused		No connect.
25, 26	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
28	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider. LVTTL / LVCMOS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Pin Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. SSC Control Input Function Table

Inputs		TEST_I/O Source	SSC	Outputs			Operational Modes
				FOUT, nFOUT		TEST_I/O	
SSC_CTL1	SSC_CTL0			DIV_SEL0	DIV_SEL1		
0	0	Internal	Disabled	fXTAL ÷ 32	fXTAL ÷ 64	fXTAL ÷ 16 ÷ M	PLL bypass; oscillator, M and N dividers test mode. NOTE 1
0	1	PLL	Enabled	fXTAL x M / 32	fXTAL x M / 64	Hi-Z	Default SSC; Modulation Factor = ½ Percent
1	0	External	Disabled	Test Clk	Test Clk	Input	PLL Bypass Mode, NOTE 1; (1MHz≤ Test Clk ≤ 200MHz)
1	1	PLL	Disabled	fXTAL x M / 32	fXTAL x M / 64	Hi-Z	No SSC Modulation

NOTE 1: Used for in house debug and characterization.

Table 3B. Programmable VCO Frequency Function Table (NOTE 1)

VCO Frequency (MHz)	M Count	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	250	0	1	1	1	1	1	0	1	0
251	251	0	1	1	1	1	1	0	1	1
252	252	0	1	1	1	1	1	1	0	0
253	253	0	1	1	1	1	1	1	0	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
508	508	1	1	1	1	1	1	1	0	0
509	509	1	1	1	1	1	1	1	0	1
510	510	1	1	1	1	1	1	1	1	0
511	511	1	1	1	1	1	1	1	1	1

NOTE 1: Assumes a 16MHz crystal.

Table 3C. Function Table

Inputs	N Divider Value	Output Frequency (MHz)	
DIV_SEL		Minimum	Maximum
0	2	125	350
1	4	62.5	175

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	46.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				155	mA
I_{CCA}	Analog Supply Current				16	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	M0:M8, SSC_CTL0, SSC_CTL1, MR, DIV_SEL, TEST_I/O, nP_LOAD		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	M0:M8, SSC_CTL0, SSC_CTL1, MR, DIV_SEL, TEST_I/O, nP_LOAD		-0.3		0.8	V
I_{IH}	Input High Current	M7, M8, SSC_CTL0, SSC_CTL1, TEST_IO	$V_{CC} = V_{IN} = 3.465V$			5	µA
		M0:M6, DIV_SEL nP_LOAD, MR	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	M7, M8, SSC_CTL0, SSC_CTL1, TEST_IO	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
		M0:M6, DIV_SEL nP_LOAD, MR	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Output terminated with 50Ω to V_{CCO} - 2V. See Parameter Measurement Section, 3.3V Output Load Test Circuit.

Table 5. Crystal Characteristics

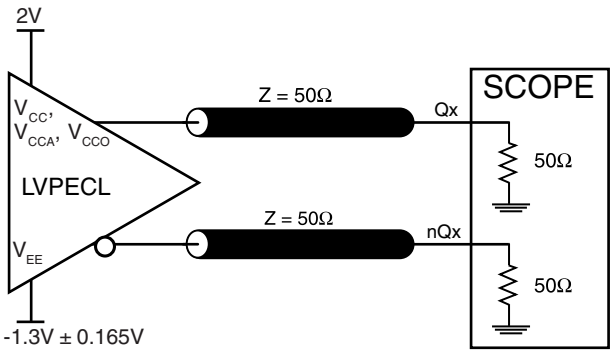
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		14	16	25	MHz
Equivalent Series Resistance (ESR)				40	Ω
Shunt Capacitance		3		7	pF

Table 6. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = -40°C to 85°C

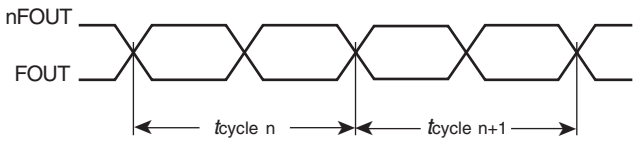
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		62.5		350	MHz
$t$jit(cc)	Cycle-to-Cycle Jitter; NOTE 1, 5	$F_{OUT} \geq 100MHz$		19		ps
odc	Output Duty Cycle			50		%
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
F_{xtal}	Crystal Input Range; NOTE 2, 3		14	16	25	MHz
F_M	SSC Modulation Frequency; NOTE 4	F_{OUT} = 200MHz	29		33.33	KHz
F_{MF}	SSC Modulation Factor; NOTE 4	F_{OUT} = 200MHz		0.4		%
SSC_{red}	Spectral Reduction; NOTE 4	F_{OUT} = 200MHz		10		dB
t_{STABLE}	Power-up to Stable Clock Output				10	ms

See Figures in the Parameter Measurement Information section.
NOTE 1: Jitter performance using XTAL inputs.
NOTE 2: Only valid within the VCO operating range.
NOTE 3: For XTAL input, refer to Application Note.
NOTE 4: Spread Spectrum clocking enabled.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Parameter Measurement Information



3.3V Output Load AC Test Circuit

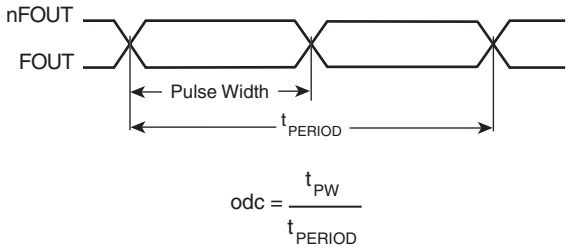


$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$

1000 Cycles

Cycle-to-Cycle Jitter

Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8431I-21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, better power supply isolation is required. *Figure 3* illustrates how a 10Ω along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

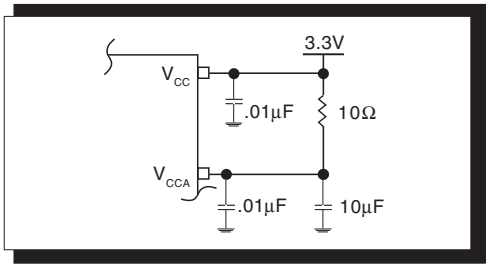


Figure 3. Power Supply Filtering

Termination for LVPECL Outputs

The clock layout topology shown below is typical for IA64/32 platforms. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

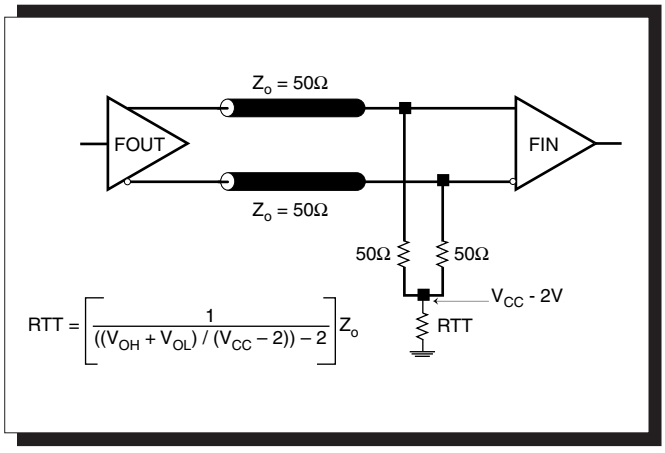


Figure 2A. LVPECL Output Termination

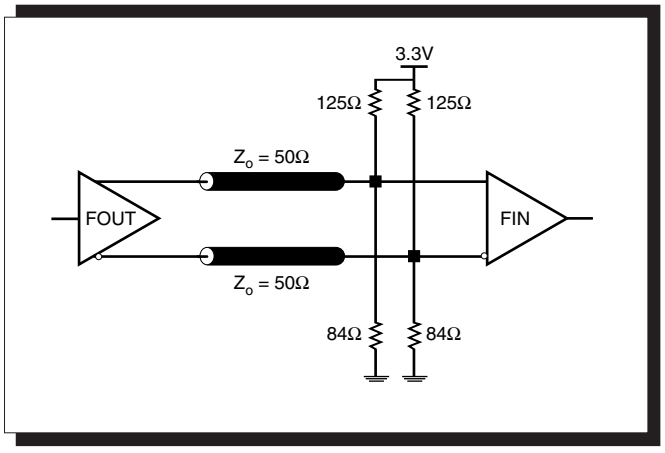


Figure 2B. LVPECL Output Termination

Crystal Input Interface

The ICS8431I-21 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

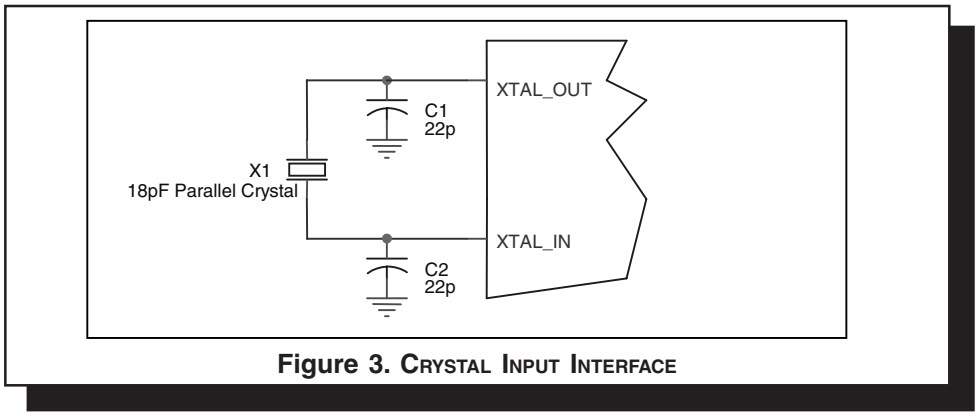


Figure 3. Crystal Input Interface

Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 30kHz triangle waveform is used with 0.5% down-spread (+0.0% / -0.5%) from the nominal 200MHz clock frequency. An example of a triangle frequency modulation profile is shown in *Figure 4A* below. The ramp profile can be expressed as:

- Fnom = Nominal Clock Frequency in Spread OFF mode (200MHz with 16MHz IN)
- Fm = Nominal Modulation Frequency (30kHz)
- δ = Modulation Factor (0.5% down spread)

$(1 - \delta)$ fnom + 2 fm x δ x fnom x t when $0 < t < \frac{1}{2\,fm}$,

$(1 - \delta)$ fnom - 2 fm x δ x fnom x t when $\frac{1}{2\,fm} < t < \frac{1}{fm}$

The ICS8431I-21 triangle modulation frequency deviation will not exceed 0.6% down-spread from the nominal clock frequency (+0.0% / -0.5%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 4B.* The ratio of this width to the fundamental frequency is typically 0.4%, and will not exceed 0.6%. The resulting spectral reduction will be greater than 7dB, as shown in *Figure 4B*. It is important to note the ICS8431I-21 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

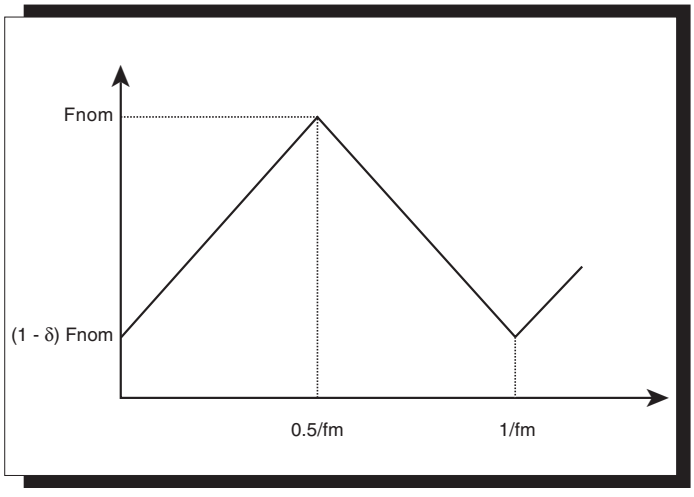


Figure 4A. Triangle Frequency Modulation

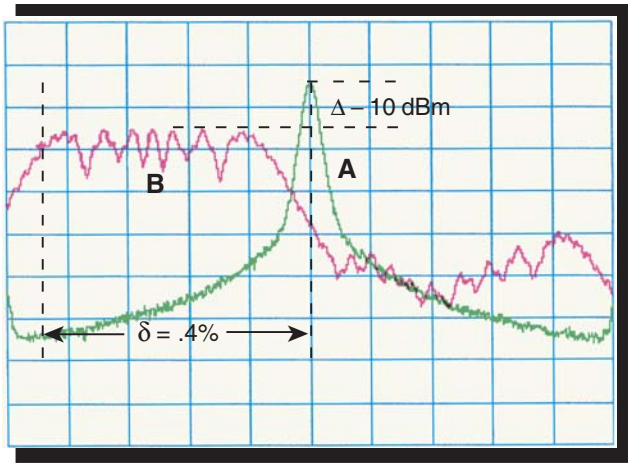


Figure 4B. 200MHz Clock Output in Frequency Domain

(A) Spread-Spectrum OFF (B) Spread-Spectrum ON

Layout Guideline

The schematic of the ICS8431I-21 layout example used in this layout guideline is shown in *Figure 5A.* The ICS8431I-21 recommended PCB board layout for this example is shown in *Figure 5B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types and the density of the P.C. board.

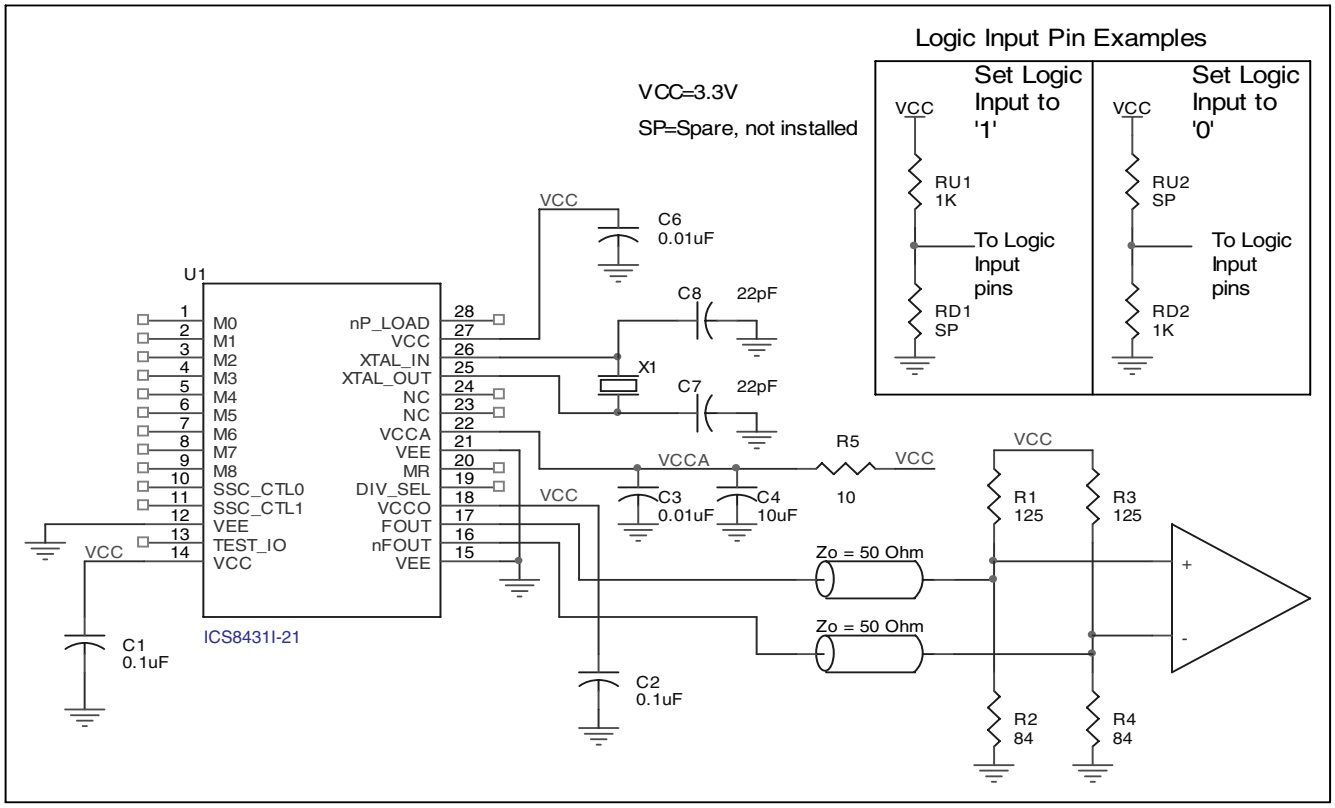


Figure 5A. Schematic Example

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C1, C2 and C6, as close as possible to the power pins. If space allows, placment of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin generated by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R5, C3, and C4 should be placed as close to the V_{CCA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The 50Ω output trace pair should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

The matching termination resistors R1, R2, R3 and R4 should be located as close to the receiver input pins as possible. Other termination scheme can also be used but is not shown in the example.

Crystal

The crystal X1 should be located as close as possible to the pins 25 (XTAL_OUT) and 26 (XTAL_IN). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

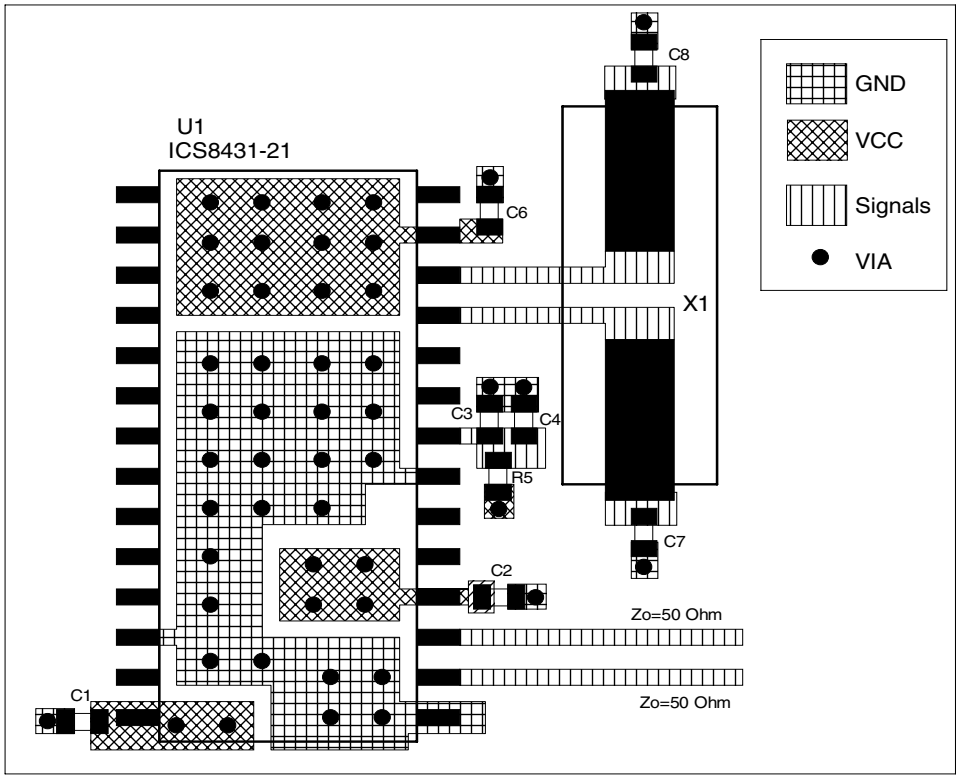


Figure 5B. PCB Board Layout For ICS8431I-21

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8431I-21. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8431I-21 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 155mA = **537.1mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 1 * 30mW = **30mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 537.1mW + 30mW = **567.1mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.567W * 39.7°C/W = 107.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 28-pin SOIC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	76.2°C/W	60.8°C/W	53.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

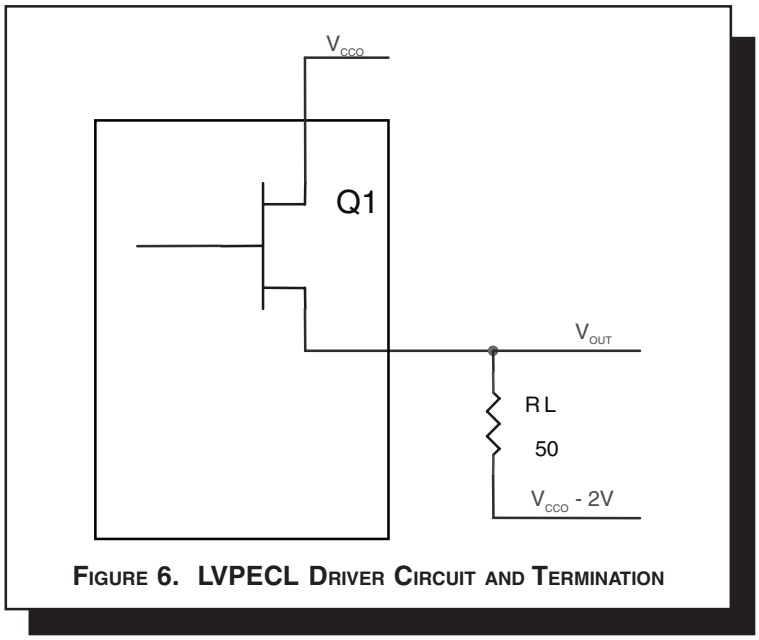


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 28 Lead SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	76.2°C/W	60.8°C/W	53.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS8431I-21 is: 4790

Package Outline - M Suffix for 28 Lead SOIC

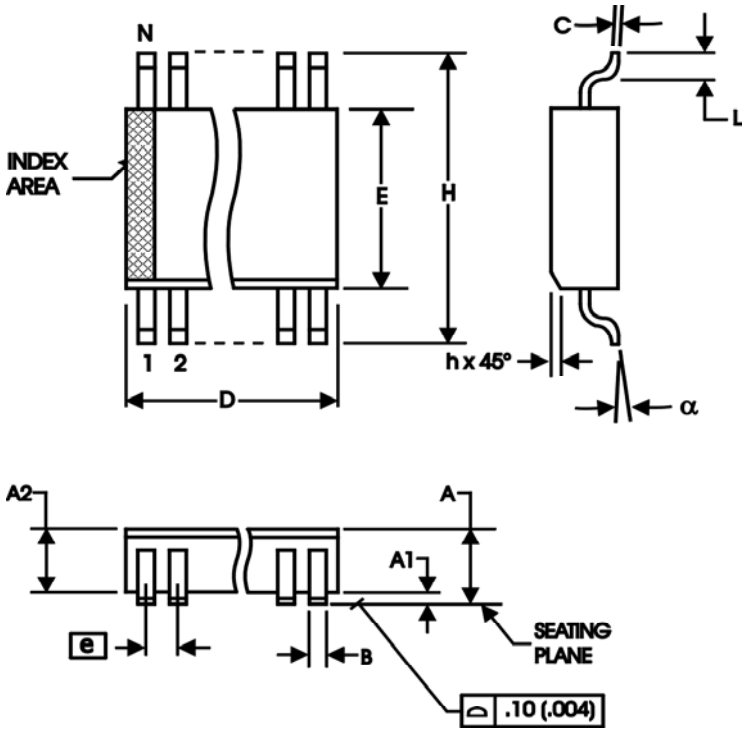


Table 9. Package Dimensions

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	28	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	17.70	18.40
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8431AMI-21	ICS8431AMI-21	28 Lead SOIC	Tube	-40°C to 85°C
ICS8431AMI-21T	ICS8431AMI-21	28 Lead SOIC	1000 tape & reel	-40°C to 85°C