



NJU25102

Digital Karaoke Audio Processor

Description

The NJU25102 is a dedicated audio processor IC which supports all of the popular functions needed to implement a high performance Karaoke sound system. The NJU25102 is a complete DSP-based system, including 16-bit Digital Signal Processor, DSP firmware contained in on-chip ROM, and all interface and logic circuits necessary to design a Karaoke audio system. No DSP system design is required.

The NJU25102 introduces valuable Karaoke feature enhancements such as expanded capability to select or remove the vocal track from Multiplexed VCD recordings, Auto Fader and Auto Multiplex functions activated by the singer's voice, and high-quality microphone echo with settable echo delay, repeat, and magnitude. Including the standard complement of Medianix Karaoke features such as Key Control, Vocal Harmony, Graphic Equalizer, Soundfields, and Bass Boost, the NJU25102 is completely circuit compatible and command set compatible with earlier generation parts. With its rich feature set the NJU25102 is ideal for VCD players, Karaoke Amplifiers and Karaoke mixing systems.

Features

- ◆ Improved 16-bit Digital Microphone Echo
Full control of Echo Level and Repeat
Echo Delay up to 215ms
Superior Audio Quality
- ◆ Expanded Multiplex and Auto Multiplex features
Auto Multiplex Activated by Singer
0% to 100% pan-pot control of vocal track
Reverse Multiplex for right-channel recordings
- ◆ Vocal Fader with Voice-Activated Auto Mode
- ◆ Key Control Adjusts from -8 to +7 semitones
- ◆ Vocal Harmony Creates Singer Duet
- ◆ Dynamic Bass Boost
- ◆ 7-Band Graphic Equalizer
- ◆ Front Soundfield Simulation

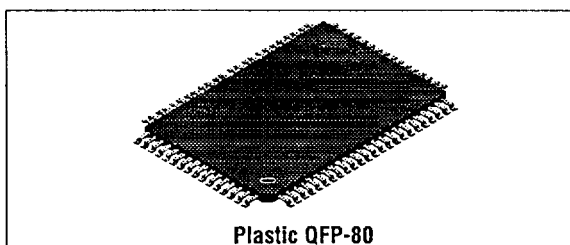
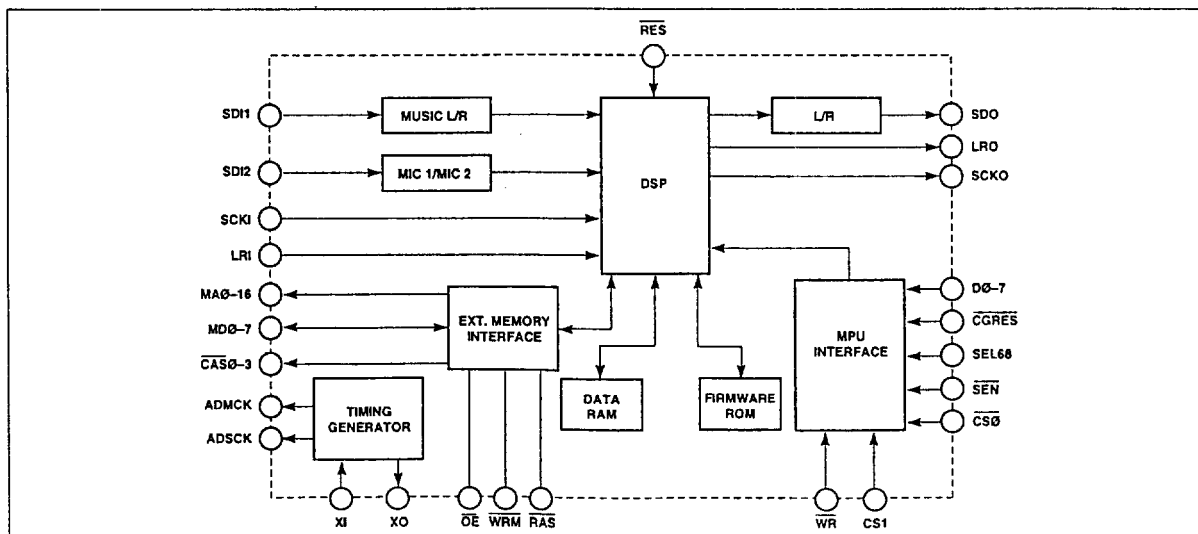


Figure 1. Block Diagram



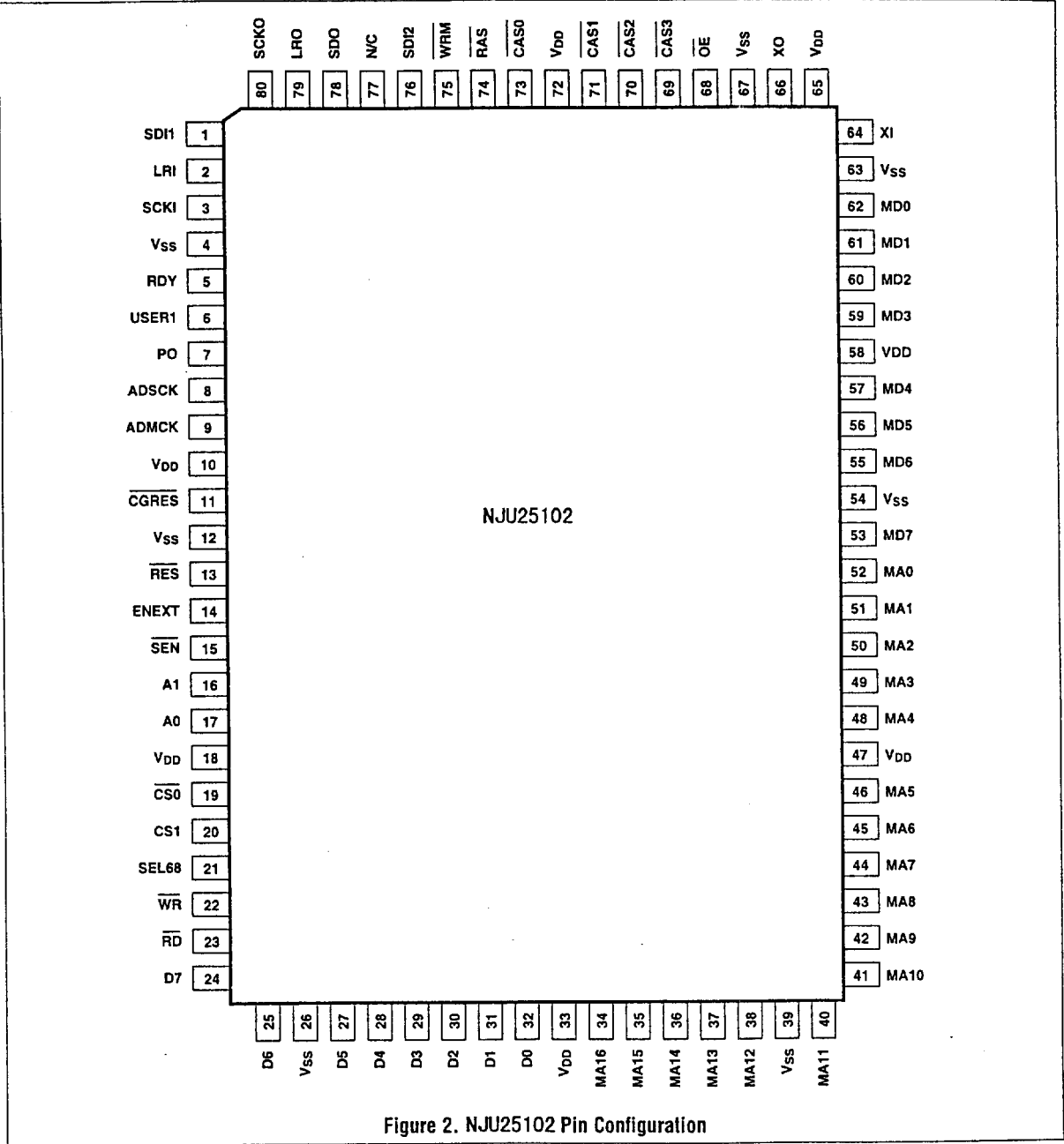


Figure 2. NJU25102 Pin Configuration

**Pin Description**

No.	Symbol	I/O	Function
1	SDI1	I	Digital audio serial data input
2	LRI	I	Left/Right frame clock input
3	SCKI	I	Digital audio serial clock input
4	VSS	I	Ground
5	RDY	I	Test pin, High for normal operation
6	USER1	I	Test pin, Low for normal operation
7	PO	O	Test pin
8	ADSCK	O	32Fs/64Fs Serial clock for A/D, D/A converter (default 32Fs)
9	ADMCK	O	384Fs/256Fs Master clock for A/D, D/A converter (default 384Fs)
10	VDD	I	Power supply, +5V
11	$\overline{\text{CGRES}}$	I	Test pin, High for normal operation
12	VSS	I	Ground
13	$\overline{\text{RES}}$	I	Reset. Must be held Low for at least 2 clock cycles after power on
14	ENEXT	I	Test pin
15	$\overline{\text{SEN}}$	I	MPU serial interface enable. Serial: Low, Parallel: High
16	A1	I	Test pin. Low for normal operation
17	A0	I	Test pin. Low for normal operation
18	VDD	I	Power supply, +5V
19	$\overline{\text{CS0}}$	I	Chip Select. MPU interface enabled when $\overline{\text{CS0}} = 0$ and CS1 = 1
20	CS1	I	Chip Select. MPU interface enabled when $\overline{\text{CS0}} = 0$ and CS1 = 1
21	SEL68	I	MPU interface mode: 68K = High, Z80 = Low
22	$\overline{\text{WR}}$	I	Write strobe. Data form MPU when low
23	$\overline{\text{RD}}$	I	Read/Write enable for 68K (Tie High for Z80)
24	D7	I	MPU data, parallel input (MSB)
25	D6	I	MPU data, parallel input
26	VSS	I	Ground
27	D5	I	MPU data, parallel input
28	D4	I	MPU data, parallel input
29	D3	I	MPU data, parallel input
30	D2	I	MPU data, parallel input
31	D1	I	MPU data, parallel input
32	D0	I	MPU data, parallel input (LSB), serial data input (SEN = 1)
33	VDD	I	Power supply, +5V
34	MA16	O	External memory address (MSB)
35	MA15	O	External memory address
36	MA14	O	External memory address
37	MA13	O	External memory address
38	MA12	O	External memory address
39	VSS	I	Ground
40	MA11	O	External memory address



Pin Description (Continued)

No.	Symbol	I/O	Function
41	MA10	O	External memory address
42	MA9	O	External memory address
43	MA8	O	External memory address
44	MA7	O	External memory address
45	MA6	O	External memory address
46	MA5	O	External memory address
47	VDD	I	Power supply, +5V
48	MA4	O	External memory address
49	MA3	O	External memory address
50	MA2	O	External memory address
51	MA1	O	External memory address
52	MA0	O	External memory address (LSB)
53	MD7	I/O	External memory data (MSB)
54	VSS	I	Ground
55	MD6	I/O	External memory data
56	MD5	I/O	External memory data
57	MD4	I/O	External memory data
58	VDD	I	Power supply, +5V
59	MD3	I/O	External memory data
60	MD2	I/O	External memory data
61	MD1	I/O	External memory data
62	MD0	I/O	External memory data (LSB)
63	VSS	I	Ground
64	XI	I	Crystal/External clock input
65	VDD	I	Power supply, +5V
66	XO	O	Crystal
67	VSS	I	Ground
68	OE	O	External memory output enable
69	CAS3	O	External memory column address strobe
70	CAS2	O	External memory column address strobe
71	CAS1	O	External memory column address strobe
72	VDD	I	Power supply, +5V
73	CAS0	O	External memory column address strobe
74	RAS	O	External memory row address strobe
75	WRM	O	External memory write enable, Low to write data
76	SDI2	I	Digital audio serial data input
77	N/C	—	No Connect
78	SDO	O	Digital audio serial data output
79	LRO	O	Left/Right frame clock output, Default Left = High, Right = Low
80	SCKO	O	Digital audio serial clock output

**Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage ($T_A = 25^\circ\text{C}$)	V_{DD}	-0.3	7	V
Input, Output Pin Voltage ($T_A = 25^\circ\text{C}$)	V_X	-0.3	$V_{DD} + 0.3$	V
Operating Temperature	t_{OPR}	-20	70	$^\circ\text{C}$
Storage Temperature	t_{STG}	-55	125	$^\circ\text{C}$

All voltages relative to V_{SS} (GND)

Electrical Characteristics ($V_{DD} = 5V \pm 5\%$, $T_A = -20^\circ\text{C}$ to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Current	I_{DD}	$f_{OSC} = 34\text{MHz}$		70	110	mA
High Level Input Voltage	V_{IH}		$0.80V_{DD}$		V_{DD}	V
Low Level Input Voltage	V_{IL}		V_{SS}		$0.10V_{DD}$	V
High Level Input Current	I_{IH}	$V_{IN} = V_{DD}$			10	μA
Low Level Input Current	I_{IL}	$V_{IN} = V_{SS}$			10	μA
High Level Output Voltage	V_{OH}	$I_{OH} = 2\text{mA}$	$V_{DD}-0.5$			V
Low Level Output Voltage	V_{OL}	$I_{OL} = 2\text{mA}$			$V_{SS}+0.5$	V
Input capacitance	C_{IN}			10	20	pF
Clock Frequency	f_{OSC}		20		34	MHz
Ext. System Clock Duty Cycle	τ_{EC}		45		55	%

Overview

The NJU25102 is a pre-programmed DSP dedicated to performing digital audio functions for high performance Karaoke systems. Program ROM, RAM, and firmware are internal to the device. No firmware coding or DSP system design is required.

The NJU25102 is intended for building Karaoke machines that accept two microphone inputs, a stereo music input, and deliver a stereo Karaoke output. Music input data can be accepted in PCM digital format from a CD or laserdisc player via a S/PDIF receiver (S/PDIF is the consumer subset of the Digital Audio Interface specification defined by EIAJ CP-340, AES/EBU, and IEC958). Microphone audio or analog music tracks are applied by way of stereo A/D converters. Digital Karaoke stereo output is delivered to a D/A converter driving speaker amplifiers to complete the Karaoke

system. Figure 3. shows an example of a Karaoke implementation.

NJU25102 mode and functions are selected with simple 8 bit commands via a serial or parallel command interface. An external memory device, either DRAM or SRAM, implements microphone echo delays, key control functions, and soundfield generation. Many popular memory devices can be interfaced directly to the NJU25102 without additional logic.

A master clock source drives internal DSP processing and digital audio data transfers. 33.8688MHz is the required clock frequency (X1 pin) when operating at the nominal sample rate (F_s) of 44.1kHz. The NJU25102 internal oscillator can generate this clock with a 33.8688MHz crystal.

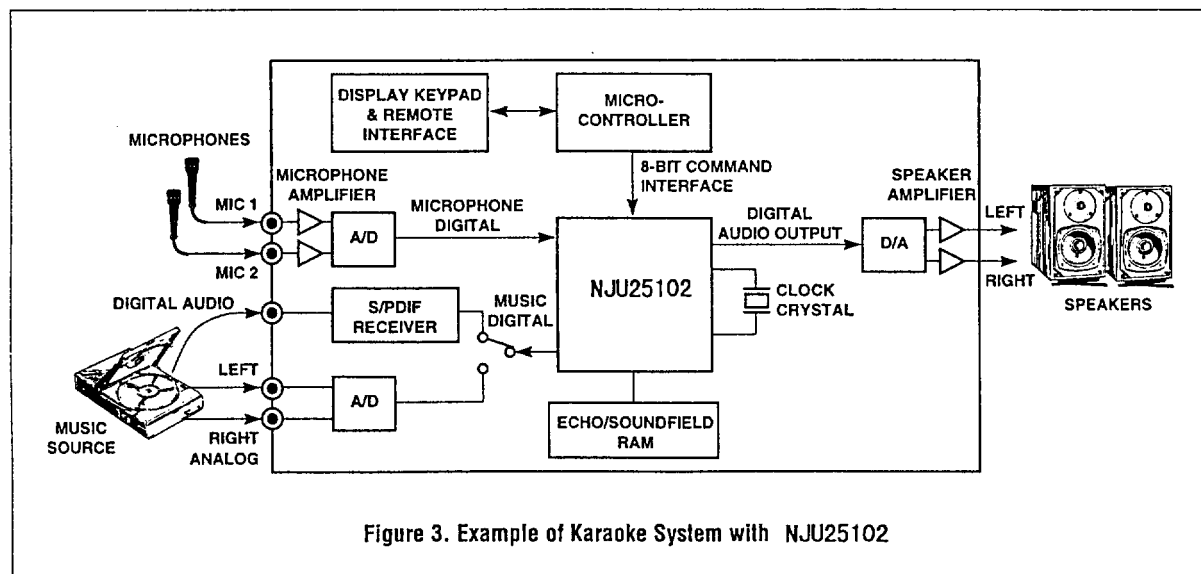


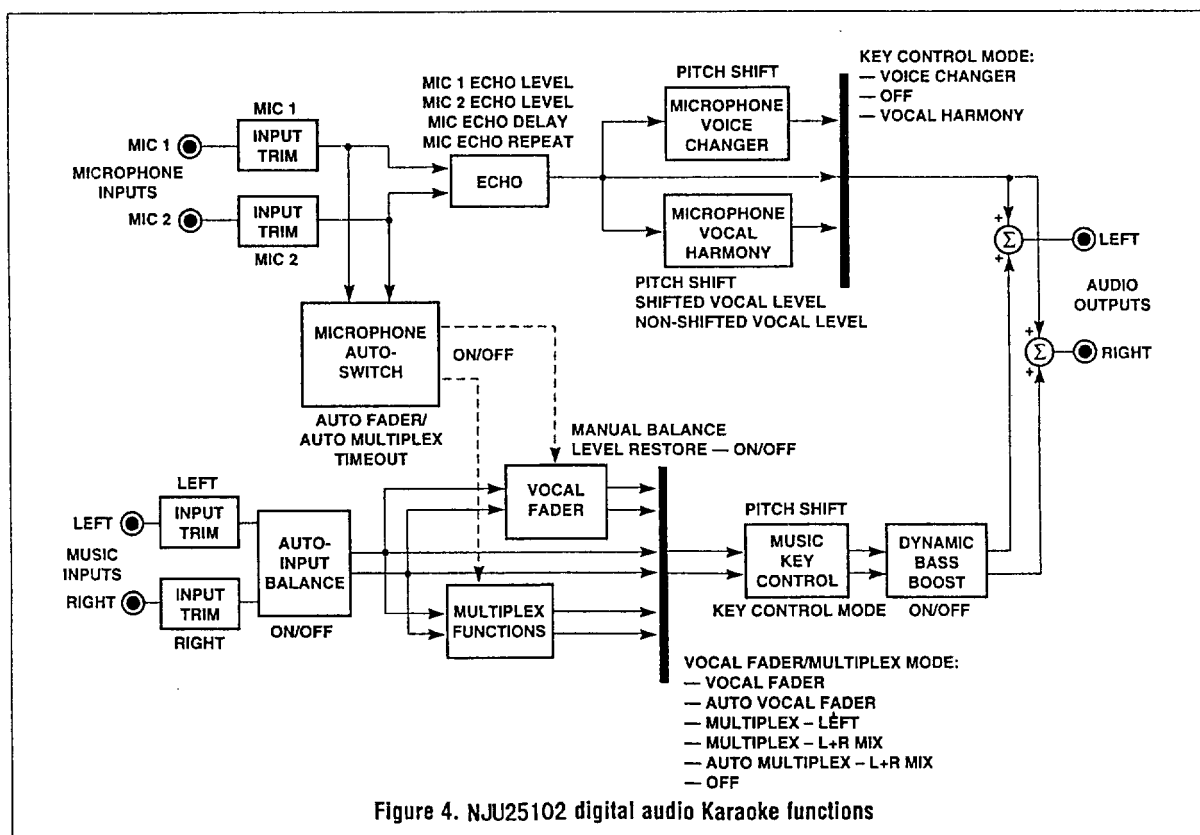
Figure 3. Example of Karaoke System with NJU25102

Karaoke Mode

The NJU25102 is pre-programmed to support these popular Karaoke functions:

- Microphone Echo
- Microphone Key Control
- Music Key Control
- Microphone Harmony
- Vocal Fader
- Multiplex-Stereo Synthesis
- Dynamic Bass Boost
- Microphone Input Level Trim
- Music Input Level Trim

Figure 4. shows the signal processing functions available in Karaoke mode. These functions, occurring in the digital audio paths between microphone inputs, music inputs, and the audio output port, are enabled via the 8 bit command interface. Labels outside the function blocks in the Figure refer to commands associated with the function. Refer to command table for details.



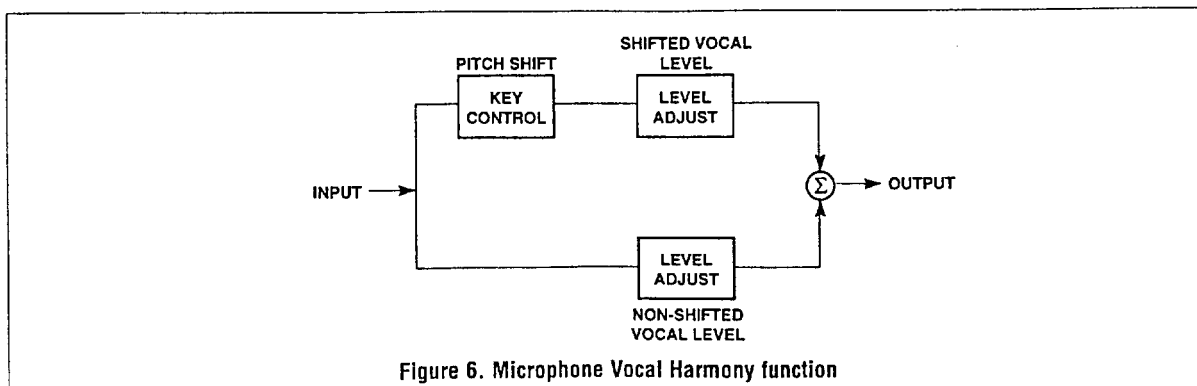
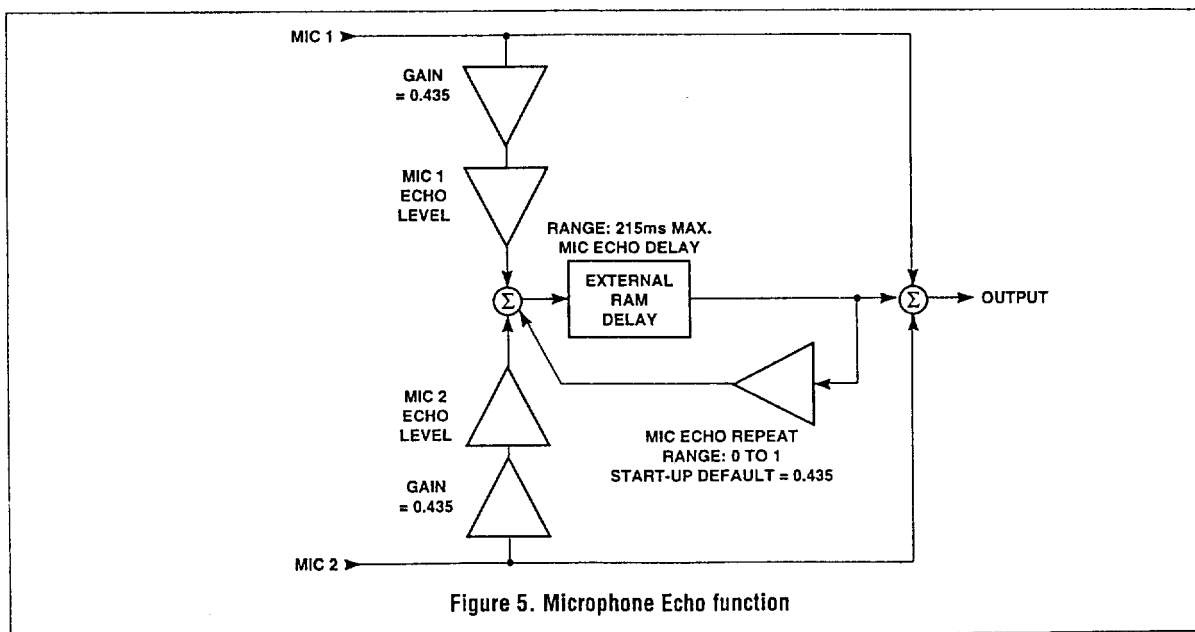
Microphone Echo

The Microphone Echo function accepts separate inputs from MIC 1 and MIC 2. Echo level control is applied independently to each microphone signal as shown in Figure 5. Echo delay is applied to the combined microphone signal. Maximum echo delay is 215ms. Microphone echo repeat is fully settable from 0% to 100%. Echo repeat is determined by the amount of delayed microphone signal fed back to the input of the RAM DELAY block.

Key Control, Voice Changer, Vocal Harmony

Any one of the three functions of Music Key Control, Microphone Voice Changer, or Microphone Vocal Harmony can be enabled at a single time. All three functions share a common Pitch Shift command. Key Control and Voice Changer change the pitch of music and microphone signals over a range of +7 to -8 semi-notes.

Microphone Vocal Harmony adds a pitch-shifted and a non-shifted microphone signal to create the sound of two vocalists as shown in Figure 6. Independent control of the pitch-shifted and a non-shifted vocal levels is provided by way of the Microphone Harmony Levels command.





Vocal Fader

The Vocal Fader function removes a portion of the input that is common (equal in phase and magnitude) to both the left and right channels and that falls within a passband approximating voice frequencies. Shown in Figure 7, the Vocal Fader operates on the principle that vocal tracks are usually recorded in the center, or equally in the left and right channels, of sound recordings.

If vocals in recorded material are not balanced equally in the left and right tracks, or if the transmission medium causes the stereo signal to become imbalanced, then the vocal attenuation will be less than optimum. The NJU25102 offers two features to augment Vocal Fader under these conditions. Auto Input Balance automatically restores the balance between left and right channels by matching the time-averaged power of the two channels. And Vocal Fader Manual Balance allows a user to adjust vocal fading by ear for maximum rejection.

Auto Input Balance operates on the entire music input signal as shown in Figure 4. It can be enabled independently of Vocal Fader. Vocal Fader Manual Balance operates only within the Vocal Fader function as shown in Figure 7.

Auto Vocal Fader

Auto Vocal Fader engages the Vocal Fader function when a Karaoke singer is singing in the microphone inputs. When the singer is silent Auto Vocal Fader turns off vocal fading so the entire music track, including vocal, can be heard. This helps the Karaoke singer regain place in music lyrics.

Auto Vocal Fader is operated by the Microphone Auto-Switch control block (Figure 4) which senses the level of the two microphone inputs. If the amplitude of either microphone input exceeds a preset threshold then the Microphone Auto-Switch turns ON. When the amplitude of both microphone inputs remains below the preset threshold for a time set by the Auto Fader/Auto Multiplex Timeout command then the Microphone Auto-Switch will turn OFF.

Vocal Fader Level Restore

Level Restore can be selected when either the Vocal Fader or Auto Vocal Fader functions are enabled. Normal operation of the Vocal Fader can reduce the volume, or average power level, of the music track since some center channel signal ($L=R$) is attenuated. Vocal Fader Level Restore raises the volume of music output from the Vocal Fader such that it matches the program volume at the input of the Vocal Fader function. As a result, Vocal Fader can be employed without reducing the music playback volume.

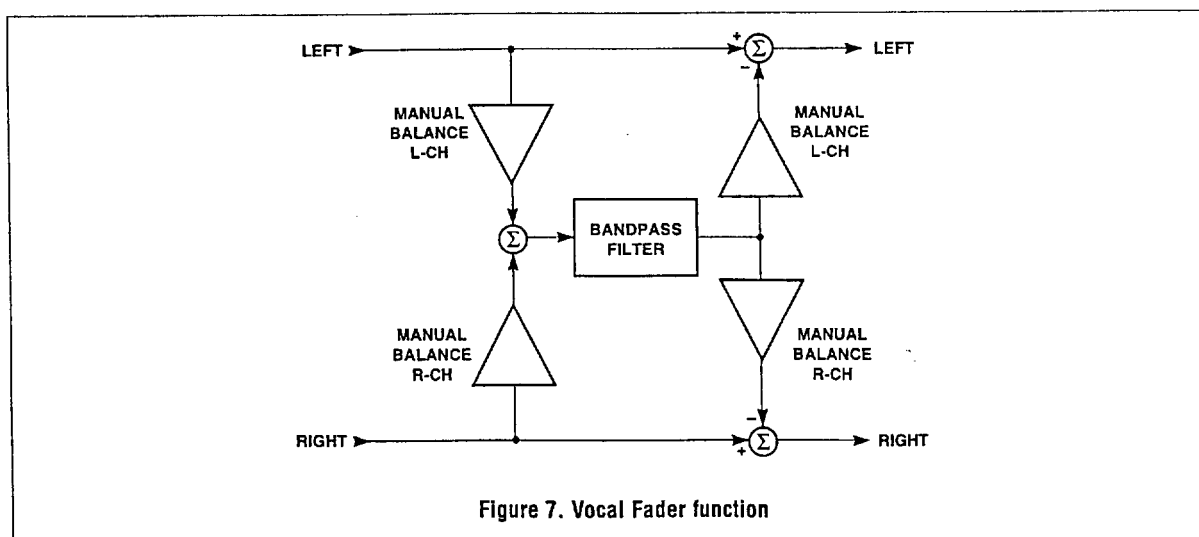


Figure 7. Vocal Fader function

Multiplex Functions

Multiplex functions are used with Multiplex Karaoke disks in which one recorded channel contains only music and the second channel contains a vocal track + music. The simplest multiplex function is Multiplex-LEFT, shown in Figure 8a, which splits the left channel music input into a synthesized stereo output. The vocal track, recorded only on the right channel in the format of most multiplex disks, is eliminated.

More powerful multiplex features are offered by the Multiplex L+R function (Figure 8b) and the Auto Multiplex L+R function (Figure 8c) which select an adjustable amount of left channel and right channel music signal to generate the synthesized stereo output. These adjustable levels of left and right music are represented by L+R Mix blocks, shown in detail in Figure 8d. The Multiplex L+R function uses one set of L+R mix levels which are designated as the 'ON State' levels. Auto Multiplex L+R, controlled by the MICRO-

PHONE AUTO-SWITCH block (Figure 4), uses two sets of L+R mix levels; an 'OFF State' mix is selected when the microphone is quiet and the 'ON State' mix is selected when microphone singer is active.

Left and right channel levels for each of the L+R Mix blocks are set according to two 16-bit words embedded in the 5-byte Multiplex L+R Mix Levels command. These mix blocks can be operated as audio pan-pots to select 100% left channel, 100% right channel, or a constant-power sum of the two channels as input to the stereo synthesis block.

Example 1: Play Multiplex discs that are recorded in reverse of the 'Onta' standard; having music only on right channel and vocal track + music on left channel. Method: Select Multiplex L+R function and adjust ON State L+R Mix Level for right channel input only (command 43 00 00 7F FF (Hex)). Left channel containing vocal + music track is rejected.

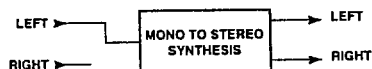


Figure 8a. Multiplex-LEFT function

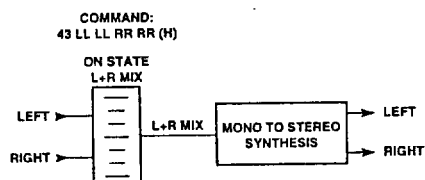


Figure 8b. Multiplex L+R function

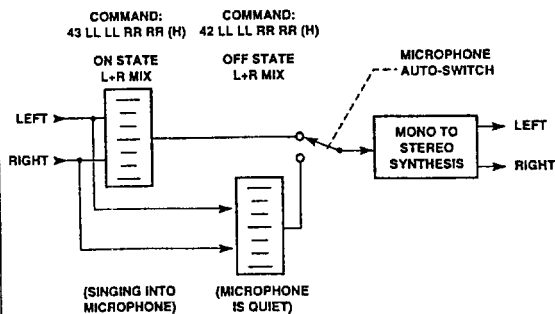


Figure 8c. Auto Multiplex L+R function

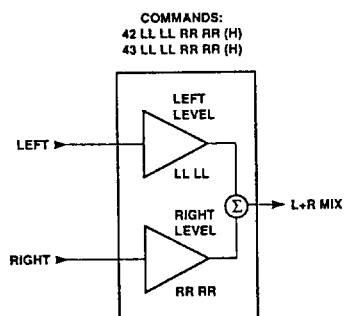


Figure 8d. Details of L+R Mix Blocks



Example 2: Select any variable amount of recorded vocal track from a multiplexed disc. Method: Select Multiplex L+R function and adjust ON State L+R Mix Level as a variable pan pot to select between 0% and 100% of vocal + music track (see Multiplex L+R Mix Levels command for details on pan-pot programming technique).

Example 3: Play a small amount of recorded vocal as a guide track when the singer is quiet, and play only music when the singer at the microphone is active. Method: Select Auto Multiplex L+R function and set OFF State L+R Mix Levels for -0.6dB Left Channel (music) and -9dB Right Channel (vocal+music). Set ON State L+R Mix Levels for 0dB Left Channel and -∞dB Right Channel. OFF State and ON State L+R Mix commands for this example are 42 77 AC 2D 6B (Hex) and 43 7F FF 00 00(Hex).

Dynamic Bass Boost

Dynamic Bass Boost provides additional low frequency gain to the music track when signal amplitude is small. The effect is similar to a Loudness control that compen-

sates for reduced sensitivity of the ear to bass frequencies at low listening levels. Dynamic Bass Boost is enabled via the command interface

The Dynamic Bass Boost function is described by a pole at 100Hz and a zero at $A_{\text{BOOST}} \times 100\text{Hz}$, where A_{BOOST} is the boost gain. Music track signal level determines the boost gain as shown below:

Music Track Signal Level	Boost Gain (A_{BOOST})
0dB (full signal level)	0dB
-12dB	6dB
-20dB	12dB
-40dB	12dB

Input Trims

Microphone Input Trim adjusts digital gain blocks at microphone input port as shown in Figure 4. Gain of MIC. 1 and MIC. 2 inputs can be varied independently.

Music Input Trim adjusts digital gain blocks at music input port as shown in Figures 4 and 9. Independent control of left and right channel gain allows trim to function as a balance control.

Music Processor Mode

Music Processor mode offers additional sound processing features of Graphic Equalizer or Soundfield Generator as shown in Figure 9. Music Processor mode operates on music inputs only; microphone inputs are not used.

Graphic Equalizer

The graphic equalizer shapes the frequency response of left and right music channel in Music Processor mode. Up to seven frequency bands can be implemented with amplitude control of each band settable from 0dB to -24dB (+12dB to -12dB span).

The graphic equalizer is preset to seven frequency bands at reset or power-up. Center frequency of the seven bands are: 30Hz, 80Hz, 250Hz, 650Hz, 2kHz, 6kHz, and 15kHz ($F_s = 44.1\text{kHz}$).

Soundfield Simulator

The soundfield simulator electronically simulates the effect of multiple acoustic echos which are present in large listening spaces such as a concert hall or theatre. Soundfield Simulator is available in NJU25102 Music Processor mode. The DSP architecture of the NJU25102 allows a wider range of soundfield effects to be simulated than is possible with most analog architectures. A pre-loaded 'Hall mode' soundfield can be selected, or custom soundfields can be implemented by downloading coefficients via the command interface.

Figure 10. illustrates the function of the soundfield simulator. Twelve coefficients, OFST0-OFST3, ATT0-ATT3, and COE0-COE3 define the behavior of the simulator as indicated in the Figure. These coefficient can be preset to values for 'Hall' mode surround, or custom coefficients can be loaded to design any desired soundfield characteristics. Refer to the Music Processor command table.

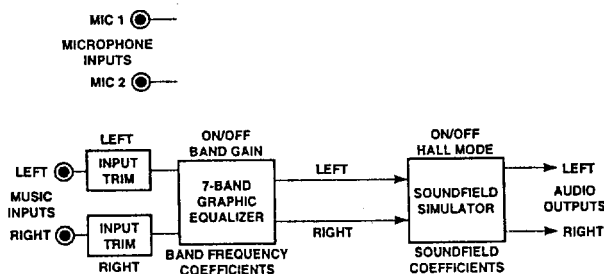


Figure 9. NJU25102 Music Processor functions

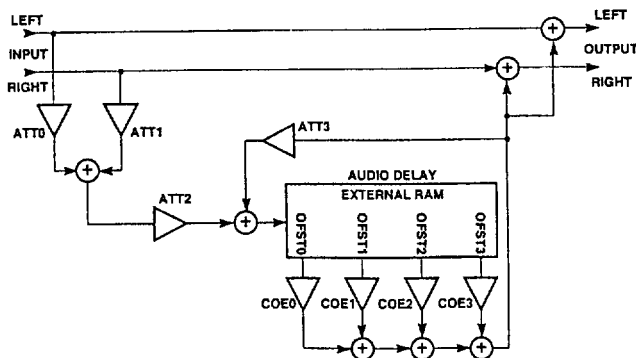


Figure 10. Soundfield Simulator



Functional Description

Digital Audio Data Interface

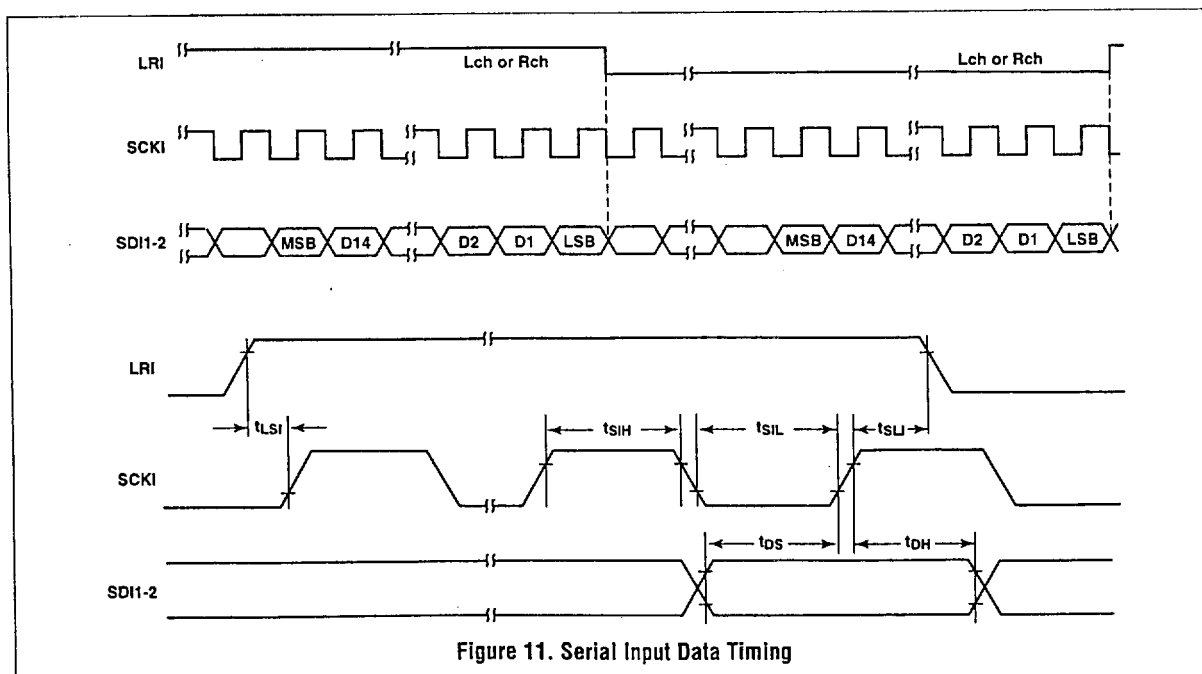
The NJU25102 has two stereo digital audio inputs (microphone and music inputs) and one stereo digital audio output. Most popular serial interface stereo A/D and D/A converters can be connected to these digital audio ports as well as format converters for S/PDIF digital audio interfaces.

Table 1. MED25102 serial digital audio pins

Input Port	SDI1	music data
	SDI2	microphone data
	SCKI	serial clock
	LRI	left/right frame clock
Output Port	SDO	audio data
	SCKO	serial clock
	LRO	left/right frame clock
	ADMCK	384Fs/256Fs for A/D, D/A
Clock Source	ADSCK	32Fs/64Fs serial clock

Three serial data formats are supported for the digital audio: left justified, right justified, and I²S. Data is always 16 bits, MSB first, and 2's complement. Polarity of the L/R clocks (LRI, LRO) is programmable along with the active edge of the serial bit clocks (SCKI, SCKO). A master clock (ADMCK) and serial bit clock (ADSCK) for the A/D and D/A converters are provided by an internal, programmable clock generator for synchronous operation with the DSP clock (768Fs). Programming for the digital audio interface is carried out with the System State Download command.

A single data format (left justified, right justified, or I²S) must be selected for both inputs and outputs. ADSCK and ADMCK frequencies (32/64Fs and 256/384Fs respectively) are also common to both input and output. SCLK and LRCLK polarities may be chosen independently between the input pair and the output.



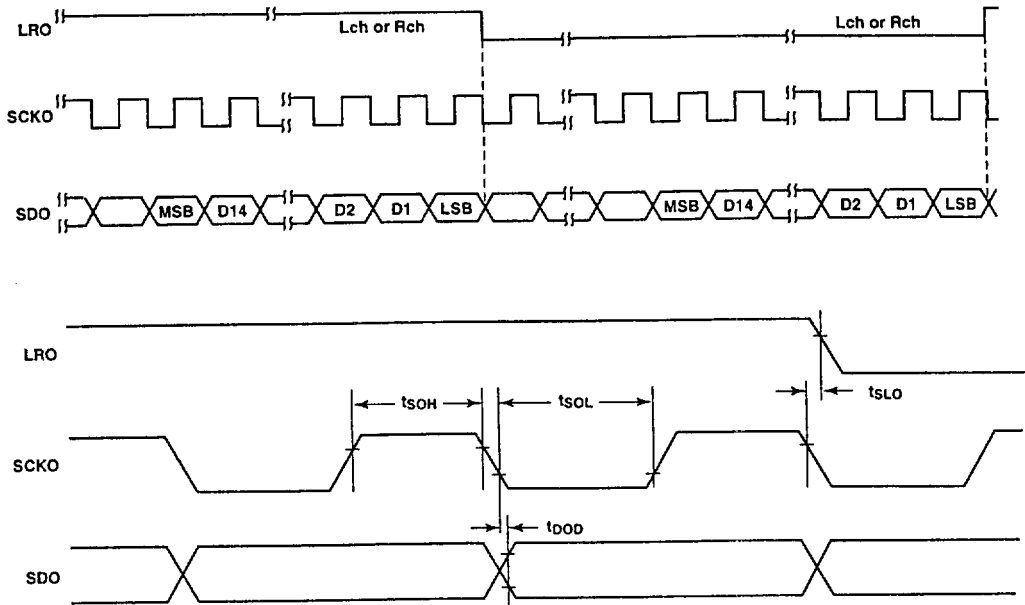


Figure 12. Serial Output Data Timing

Electrical Characteristics ($V_{DD} = 5V \pm 5\%$, $T_A = -20^\circ C$ to $70^\circ C$)

Serial Data Output

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SCKO Period		C_L : LRO, SCKO, SDO = 5pF	160			ns
L Pulse Width	t_{SOL}		80			ns
H Pulse Width	t_{SOH}		80			ns
SCKO to LRO Time	t_{SLO}				5	ns
Data Output Delay	t_{DOD}				5	ns

Serial Data Input

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SCKI Period			160			ns
L Pulse Width	t_{SIL}		80			ns
H Pulse Width	t_{SIH}		80			ns
SCKI to LRI Time	t_{SLI}		50			ns
LRI to SCKI Time	t_{LSI}		75			ns
Data Setup Time	t_{DS}		10			ns
Data Hold Time	t_{DH}		10			ns



Serial Data Formats

The three serial data formats; left justified, right justified, or I²S, are selected by FMT0 and FMT1 bits in the second byte of the three-byte System State Download command.

Digital Audio Output Interface

In Left Justified Mode, the MSB is aligned to the edge of LRI or LRO. The data is positioned at the left or "front" side of the L/R pulse (Fig. 13). In Right Justified Mode, the LSB is aligned to the LRI or LRO edge. The data is at the right or "rear" of the L/R pulse (Fig. 14). Sometimes this mode is called Japanese Mode or EIAJ Mode. The I²S Mode is similar to Left Justified Mode, except that the data is delayed one SCLK period and the sense of LRI and LRO is inverted (Fig. 15). In I²S Mode, the LRI and LRO are low for left channel data and high for right channel data, normally opposite of other modes. The polarity of LRI and LRO can be inverted independently in any mode by the use of the

LRI and LRO bits in the System State Download Command.

Normally, the serial data bits generated by a source change on the falling edge of the serial clock so that they can be easily clocked into a shift register on rising clock edge. Considering an A/D as the source and the NJU25102 as a destination, the default setting is to clock the serial data input, SDI, in on the rising edge of SCKI. This can be changed to clock data in on the falling edge using the SCKI bit in the System Download Command.

For the output serial data, the NJU25102 is considered the source and the D/A's are considered the destination. The default interface setting is for data to be clocked out of SDO on the falling edge of SCKO so that the D/A clocks data in on the rising edge. This can be changed as well independently of the input and interface mode using the SCKO bit in the System Download Command.

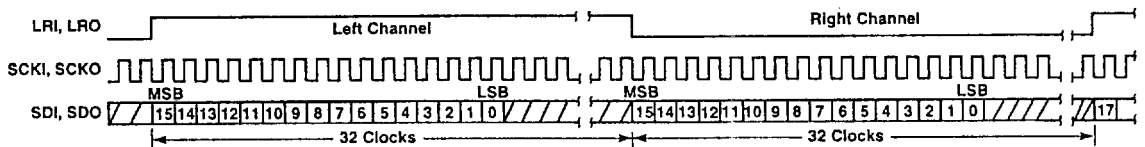


Figure 13. Left justified data format, AD SCK = 64Fs, 16-bit data

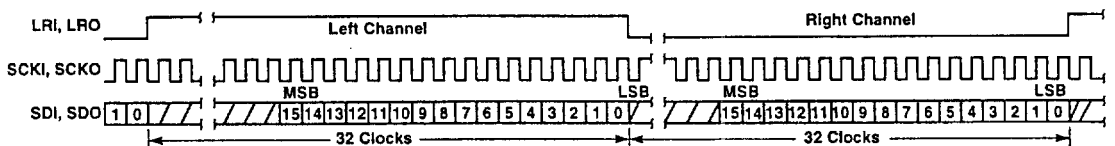


Figure 14. Right justified data format, AD SCK = 64Fs, 16-bit data

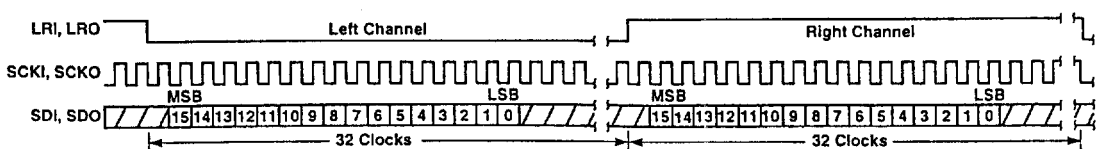


Figure 15. I²S data format, AD SCK = 64Fs, 16-bit data

The MS bit in the second System State Download Command byte selects either Master Mode or Slave Mode. In Right Justified Mode, Master Mode (MS = 0) is defined such that SCKO, the serial data clock to the D/A's, is generated from an internal divider derived from the 768Fs DSP clock (Xi). In Slave Mode (MS = 1) the serial data clock to the D/A's is a copy of the serial data clock on the input, SCKI, from the A/D. This mode should be used for asynchronous data rates, such as data from an S/PDIF receiver connected to the Digital Output from a laser disc player. When an A/D is used with analog inputs, its master clock should be synchronous to the NJU25102 using ADMCK at 256Fs or 384Fs. In this case either Master Mode or Slave Mode will work. The default setting is Master Mode (MS = 0). In I²S Mode, Master and Slave modes have slightly different meaning, which is closer to the conventional definitions associated with A/D and D/A converters. Considering the NJU25102 point of reference, Slave Mode (MS = 1) is defined in this case as LRI and SCKI are *inputs from* the A/D. This means that the A/D must be in Master Mode with L/R and SCLK *outputs*. Conversely, when the MED25102 is in Master Mode (MS = 0), the LRI and SCKI are *outputs* which drive the L/R and SCLK inputs of an A/D operating in slave mode. The SCKO and LRO to the D/A's are always *outputs*. The D/A converters, therefore can only run in Slave Mode expecting both the L/R and SCLK from the NJU25102. As in Right Justified mode,

LRO and SCKO are derived from the 768Fs DSP clock. When slave mode is selected, LRO and SCKO are generated by the LRI and SCKI inputs. Slave mode should be used for asynchronous audio data.

In the third mode, Left Justified Mode, only Slave Mode (MS = 0) is allowed. The A/D is required to be in Master Mode supplying the LRI and SCKI clocks to the NJU25102 inputs. The LRO and SCKO are generated from the LRI and SCKI inputs.

In each data format mode the serial clock frequency for SCKI and SCKO can be selected using ADSCK in the System Download Command to be either 32Fs (32-bit clocks per sample) or 64Fs (64-bit clocks per sample). Both SCKI and SCKO must be the same frequency. This clock is generated internally for use on the SCKI and SCKO pins (Master Mode), but is also available as a separate output on a pin called ADSCK. It is derived from the 768Fs Input Clock to the NJU25102.

If SCKI and SCKO are selected to be 32Fs then both Left and Right Justified Modes look exactly the same (Fig. 16), and either mode setting will work. This is because a stereo pair of 16-bit channels will use all 32 clocks per sample. In I²S mode the data bits appear shifted by one SCLK and the L/R is inverted (Fig. 17).

An output clock, ADMCK, is derived from the NJU25102 768Fs Input Clock for use as an A/D or D/A master clock. ADMCK is set to 256Fs or 384Fs using the ADMCK bit in the System Download Command.

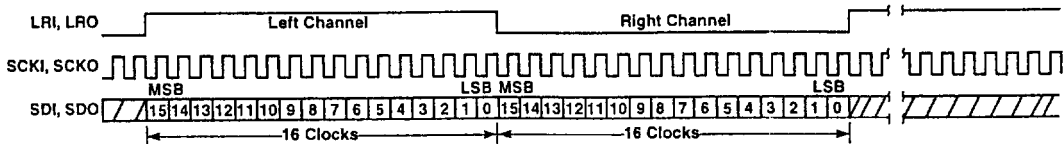


Figure 16. Left Justified data format, ADSCK = 32Fs, 16-bit data

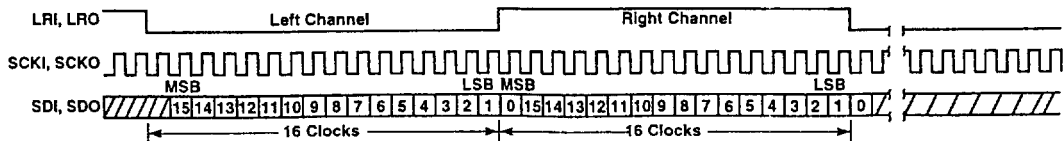


Figure 17. I²S data format, ADSCK = 32Fs, 16-bit data

Serial Interface Configurations

Audio data samples must be transferred in synchronism between the two digital audio inputs and the digital audio output of the NJU25102. That is, for each audio sample at the serial digital output there must be one and only one audio sample at either serial digital input. Audio samples are transferred at the audio sampling rate, F_s .

To maintain audio data synchronism, a single device is chosen to establish the audio sampling rate in the system. This device may be the NJU25102, or one of the A/D converters with its master clock (MCK) input sourced by the NJU25102. In either case, the audio sample rate will be derived from, and therefore synchronous with, the 768Fs DSP clock (Xi pin) driving the NJU25102.

If audio is to be received from an external digital source, from an S/PDIF interface for example, then it becomes necessary to synchronize all audio data transfers to this external source. S/PDIF format converters deliver not only an audio sample rate clock

derived from the externally applied digital inputs, but also the higher frequency master clock (MCK) used by the A/D and D/A converters. This mode of operation is called *asynchronous* since the audio data transfers are not derived from, and therefore are not synchronous with, the 768Fs DSP clock.

Figure 18. shows a typical digital audio interface implementation that can accept music channel audio in either digital or analog form. When analog music input is selected the Music A/D converter is in Master Mode and establishes the audio sample rate, F_s . Both the Microphone A/D converter and the Output D/A converter are in Slave Mode; their SCLK and L/R inputs derive from the Music A/D converter.

If digital music input is selected then the S/PDIF receiver becomes the Master Mode device in the system. The Microphone A/D converter and the Output D/A converter are in Slave Mode as before; the Music A/D converter is not used.

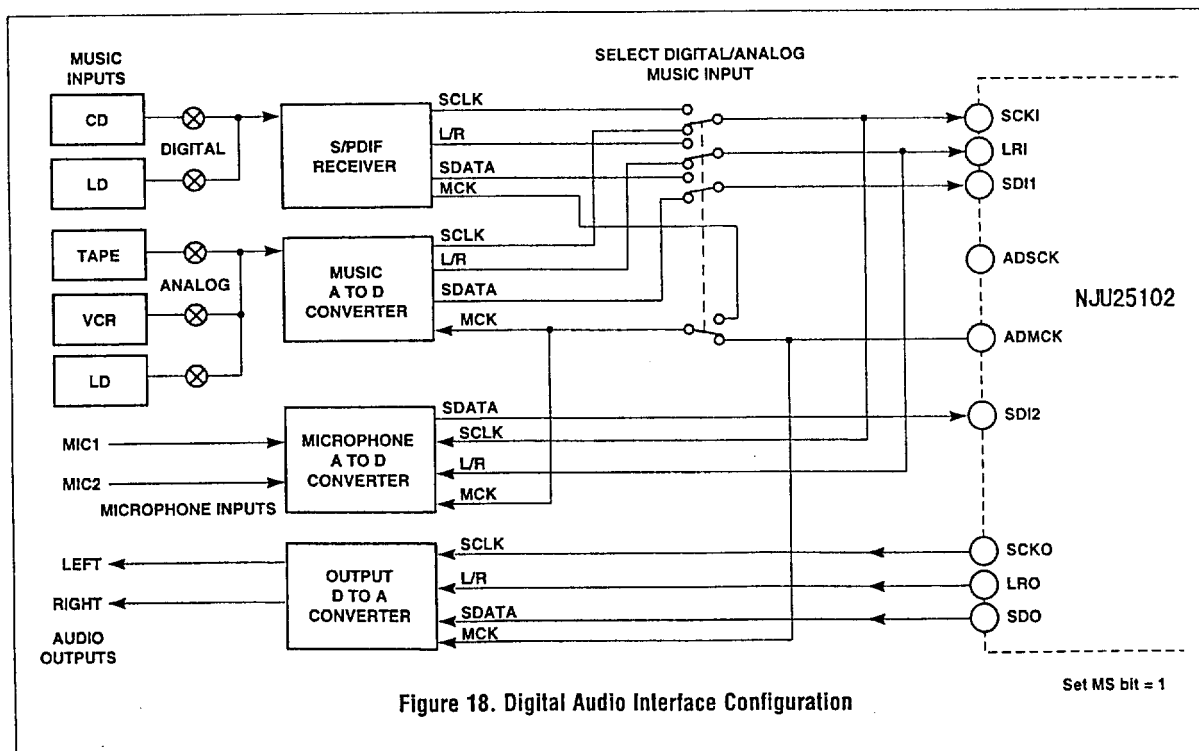


Figure 18. Digital Audio Interface Configuration

Microcontroller Interface

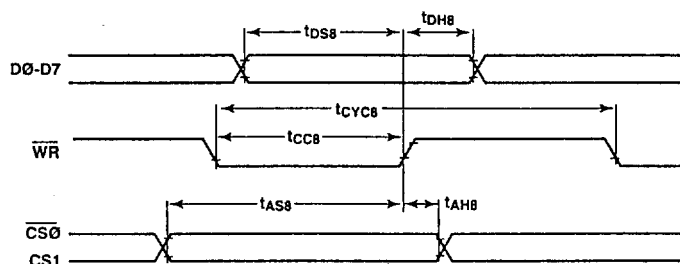
Either a Z80 or 68K type microcontroller can be used to download commands to the NJU25102. SEL68 must be set high for 68K and low for Z80. Either serial or 8-bit parallel interface modes may be used, depending on $\overline{SEN}$ input (L:serial; H:parallel). The MPU interface is enabled when $\overline{CS0} = 0$ AND $CS1 = 1$, allowing a control signal of either polarity to be used.

The MPU interface was designed for both read and write operations. However, the DSP firmware only supports write operations.

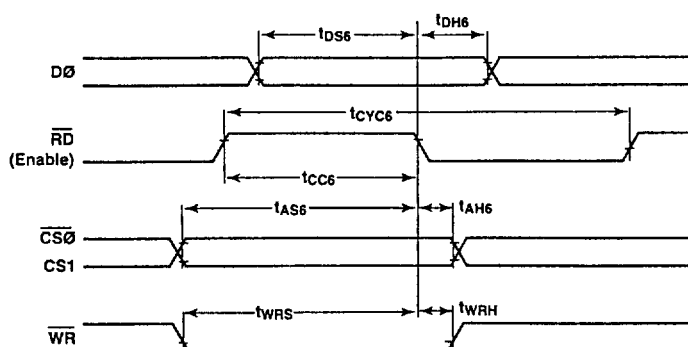
Only one command should be written to the NJU25102 per L/R period (22.7 μ s @ $f_s = 44.1$ kHz). Commands are serviced during a window of time at the end of each L/R period when processing of the audio sample is finished. Sending more than one command during a single L/R period risks overwriting earlier commands as commands may arrive while the NJU25102 is busy processing audio data.

Several commands (System Download, Microphone Echo Delay, and commands associated with the Graphic Equalizer and Soundfield Simulator) are greater than one byte in length. These multi-byte commands consist of an instruction byte followed by one or more data bytes. When the NJU25102 receives and decodes the instruction byte of a multi-byte command it halts audio processing while it waits for the remaining bytes. When the last data byte of a multi-byte instruction is written then audio processing resumes.

When writing multi-byte commands to the NJU25102 observe the following timing rules: 1) Wait an interval of at least one L/R period between writing the first byte (instruction byte) and the second byte (data byte) of the command. 2) Wait an interval of at least 1 μ s between writing all remaining data bytes.



a. Z80 Interface (SEL68 Low)



b. 68K Interface (SEL68 High)

Figure 19. Parallel Interface Timing



Parallel Interface

Z80 Mode

Writing commands to the **NJU25102** from a Z80 type microprocessor is accomplished by placing data on the input data port, D0 to D7, setting the chip selects, and strobing $\overline{WR}$ low then high. Successive writes, as in the three-byte System Download Command, can be done without resetting the chip select(s). It is recommended to return the Chip Select to the inactive state as soon as the command is sent. The recommended sequence for writing parallel data to the **NJU25102** is:

1. Set $\overline{RD} = 1$, $\overline{SEN} = 1$, and $SEL68 = 0$ (can be tied to V_{CC} and GND respectively).
2. Place data on the data port, D0:7.
3. Assert chip selects, ($\overline{CS0} = 0$ AND $CS1 = 1$). One can be permanently tied to its active state, while the other is controlled.
4. Strobe $\overline{WR}$ low, then high.
5. De-activate chip selects ($\overline{CS0} = 1$ OR $CS1 = 0$).
6. Wait at least one L/R period before writing next command (1 μ s if between data bytes of multi-byte command).

68K Mode

In 68K mode (SEL68 High) $\overline{RD}$ acts as a strobe for both read and write operations. $\overline{WR}$ defines whether a read or write is to be performed (L:write to **NJU25102**; H:there is no provision for reading from **NJU25102**). Since only write operations are allowed, $\overline{WR}$ can be tied low. The recommended sequence to write parallel data to the **NJU25102** in this mode is:

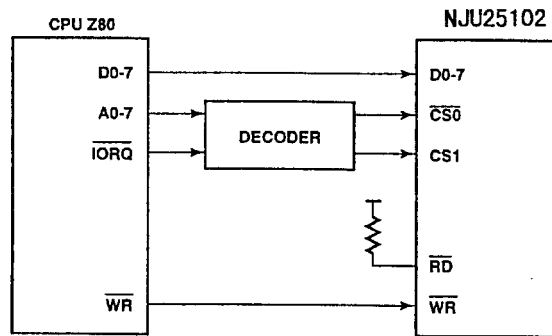
1. Set $\overline{WR} = 0$, $\overline{SEN} = 1$, and $SEL68 = 1$ (can be tied to GND and V_{CC} respectively).
2. Place data on the data port, D0:7.
3. Assert chip selects, ($\overline{CS0} = 0$ AND $CS1 = 1$). One can be permanently tied to its active state, while the other is controlled.
4. Strobe $\overline{RD}$ high, then low.
5. De-activate chip selects ($\overline{CS0} = 1$ OR $CS1 = 0$).
6. Wait at least one L/R period before writing next command (1 μ s if between data bytes of multi-byte command).

Z80 Interface and Serial Interface Timing ($V_{DD} = 5V \pm 5\%$, $T_A = -20^\circ C$ to $70^\circ C$)

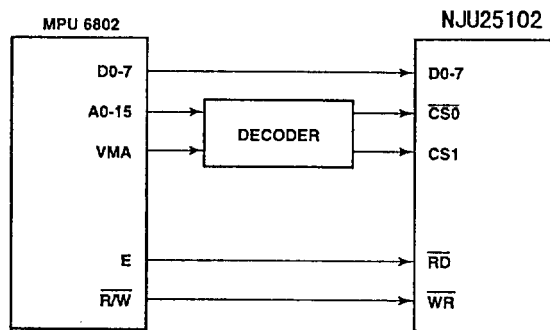
Parameter	Symbol	Condition	Min.	Max.	Unit
Address Setup Time	t_{AS8}		100		ns
Address Hold Time	t_{AH8}		100		ns
System Cycle Time	t_{CYC8}		1,000		ns
Read/Write Pulse Width	t_{CC8}		100		ns
Write Data Setup Time	t_{DS8}		10		ns
Write Data Hold Time	t_{DH8}		10		ns
System Set-up Time	t_{AW8}		20		ns

68K Interface Timing ($V_{DD} = 5V \pm 5\%$, $T_A = -20^\circ C$ to $70^\circ C$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address Setup Time	t_{AS6}		100		ns
Address Hold Time	t_{AH6}		100		ns
System Cycle Time	t_{CYC6}		1,000		ns
Read/Write Pulse Width	t_{CC6}		100		ns
Write Data Setup Time	t_{DS6}		10		ns
Write Data Hold Time	t_{DH6}		10		ns
Write-to-read Strobe Setup	t_{WRS}		100		ns
Read-to-write Strobe Setup	t_{WRH}		100		ns



20a. Z80 Interface



20b. 68K Interface

Figure 20. Microcontroller Interface



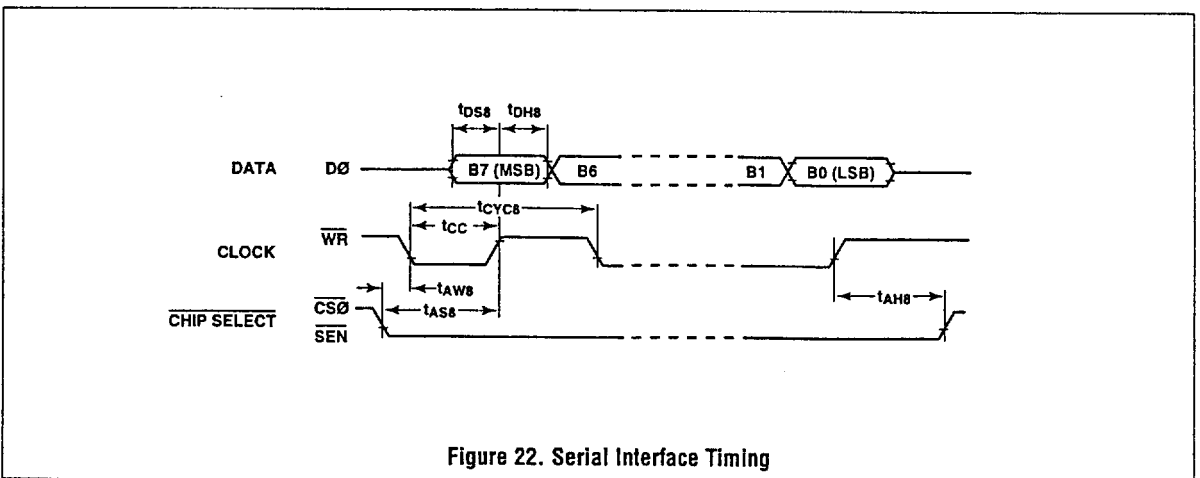
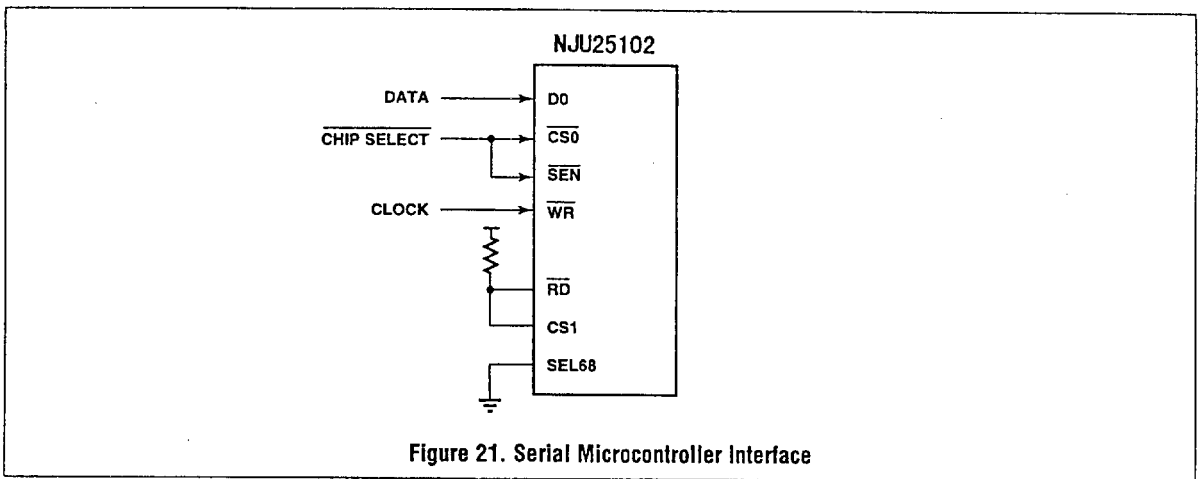
Serial Interface

In serial interface mode ($\overline{\text{SEN}} = 0$), D0 is used for the serial data input and $\overline{\text{WR}}$ is used for the serial clock. Pins $\overline{\text{CS0}}$ and $\overline{\text{SEN}}$ are tied together and driven by inverting chip select. Data is clocked in on the rising edge of $\overline{\text{WR}}$. $\overline{\text{WR}}$ must be high when $\overline{\text{CS0}}$, $\overline{\text{SEN}}$ are high.

Procedure to write one byte:

1. Set $\overline{\text{RD}} = 1$, $\text{CS1} = 1$, and $\text{SEL68} = 0$ (can be tied to VCC and GND respectively). $\overline{\text{WR}}$ must be high.
2. Assert chip select ($\overline{\text{CS0}}$, $\overline{\text{SEN}} = 0$).

3. Clock in eight bits of serial data with $\overline{\text{WR}}$ (rising edge) Return $\overline{\text{WR}}$ to high state.
4. De-activate chip select ($\overline{\text{CS0}}$, $\overline{\text{SEN}} = 0$).
5. Wait at least one L/R period (serial audio interface) before writing next command (1 μs if between data bytes of multi-byte command).





External Memory Interface

An external delay memory is used with the **NJU25102** to implement special audio effects such as Microphone Echo, Key Control, and Soundfield Simulation. External memory size of 256kbits is sufficient for all functions in Karaoke mode and is sufficient for the Soundfield Simulation function (Music Processor mode) audio delay tap settings (OFST0-OFST3) in the range of 0000(Hex) to 3FFE(Hex). External memory size of 1,024kbits (1Mbit) is also sufficient for all Karaoke mode functions and extends the Soundfield Simulation function audio delay tap range (OFST0-OFST3) from 0000(Hex) to FFFE(Hex).

The **NJU25102** interfaces to a wide range of memory devices. External memory can be SRAM or DRAM with

either 4 bit or 8 bit wide data ports. The **NJU25102** translates between an external memory data path of 4 bits or 8 bits and the 16 bit wide internal data bus.

Figure 23 shows a 1Mbit DRAM device connected to the **NJU25102**. Figures 24 show examples of connecting 256kbit and 1Mbit SRAM devices to the **NJU25102**.

Access time of RAM must be 100ns or less. Fast Page mode capability is not required for DRAM devices. The size of external memory determines the maximum allowed coefficient settings for Music Processor mode Soundfield Simulation. See Soundfield Simulation portion of command table for details.

Table 2. Settings of System State Down Load bits for Memory connection examples

Figure	Memory Size	Configuration	System State Down Load bits			
			MSIZE1	MSIZE0	MTYPE	MWIDE
23	1Mbit	256k x 4 DRAM	0	1	0	0
24	1Mbit	128k x 8 SRAM	1	0	1	1
	256kbit	32k x 8 SRAM	0	1	1	1

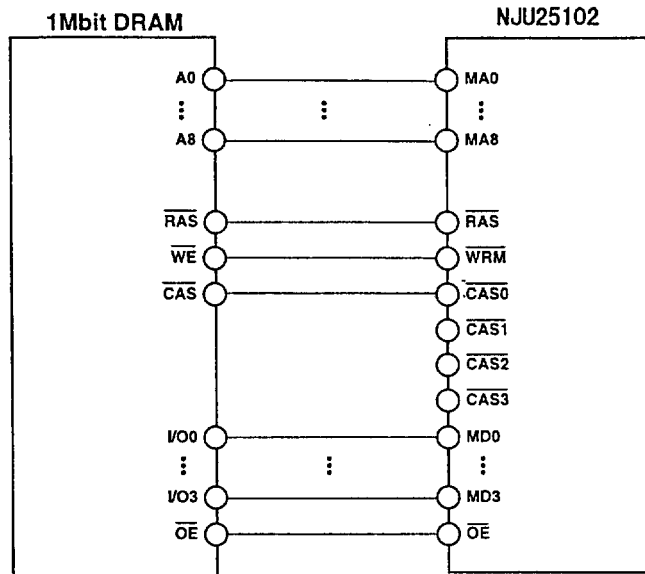
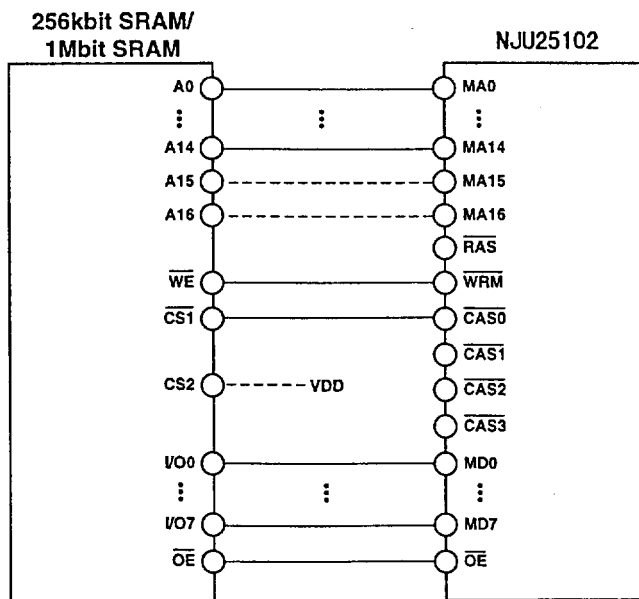


Figure 23. Single DRAM device connected to NJU25102



Note: Dotted line indicates connections for 1Mbit SRAM device only.

Figure 24. Single SRAM device connected to NJU25102



Memory access timing for external SRAM is shown below:

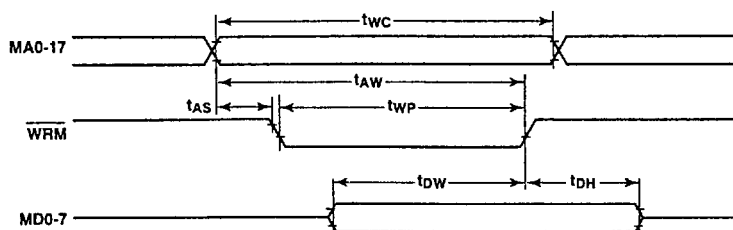


Figure 25a. SRAM WRITE Timing Example

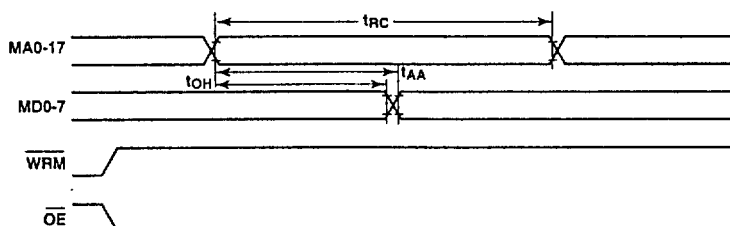


Figure 25b. SRAM READ Timing Example

Electrical Characteristics ($V_{DD} = 5V \pm 5\%$, $T_A = -20^\circ\text{C}$ to 70°C)

SRAM Interface Timing

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	$C_L \leq 70\text{pF}$	200			ns
Address Access Time	t_{AA}				200	ns
Output Hold from Address Change	t_{OH}		10			ns
Write Cycle Time	t_{WC}		200			ns
Address Setup Time	t_{AS}		10			ns
Address Valid to End of Write	t_{AW}		150			ns
Write Pulse Width	t_{WP}		100			ns
Data to Write Time Overlap	t_{DW}		60			ns
Data Hold from Write Time	t_{DH}		10			ns



Memory access timing for external DRAM is shown below:

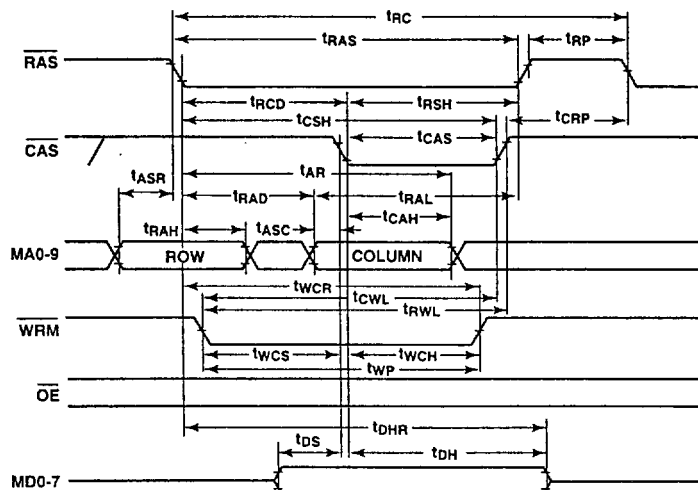


Figure 26a. DRAM WRITE Timing Example

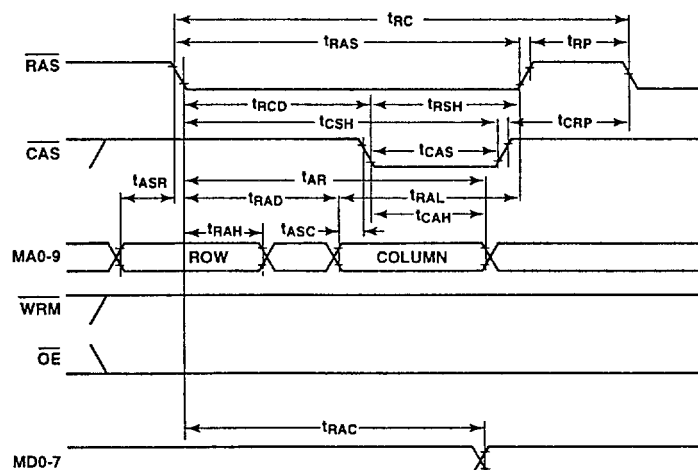


Figure 26b. DRAM READ Timing Example



Electrical Characteristics ($V_{DD} = 5V \pm 5\%$, $T_A = -20^\circ C$ to $70^\circ C$)

DRAM Interface Timing

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Random Read or Write Cycle Time	t_{RC}		200			ns
Access Time from $\overline{RAS}$	t_{RAC}	$C_L \leq 70pF$			100	ns
RAS Precharge Time	t_{RP}		100			ns
RAS Pulse Width	t_{RAS}		100			ns
RAS Hold Time	t_{RSH}		40			ns
CAS Hold Time	t_{CSH}		100			ns
CAS Pulse Width	t_{CAS}		40			ns
RAS to $\overline{CAS}$ Delay	t_{RCD}		40			ns
RAS to Column Address Delay Time	t_{RAD}		30			ns
CAS to $\overline{RAS}$ Precharge Time	t_{CRP}		100			ns
Row Address Setup Time	t_{ASR}		0			ns
Row Address Hold Time	t_{RAH}		25			ns
Column Address Setup Time	t_{ASC}		0			ns
Column Address Hold Time	t_{CAH}		30			ns
Column Address Hold Time form $\overline{RAS}$	t_{AR}		90			ns
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}		50			ns
Write Command Hold Time	t_{WCH}		40			ns
Write Command Hold Time from $\overline{RAS}$	t_{WCR}		90			ns
Write Command Pulse Width	t_{WP}		70			ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}		70			ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}		70			ns
Data-In Setup Time	t_{DS}		0			ns
Data-In Hold Time	t_{DH}		40			ns
Data-In Hold Time Reference to $\overline{RAS}$	t_{DHR}		100			ns
Write Command Setup Time	t_{WCS}		10			ns



Clock Oscillator Circuits

The on-chip oscillator requires only an external quartz crystal and two capacitors to generate the DSP clock and related timing signals. The required oscillator frequency is determined by multiplying the sampling frequency by 768. For 44.1kHz sampling frequency the required oscillator frequency is 33.8688MHz.

Table 3. Clock Oscillator Requirements

Sampling Frequency	DSP CLOCK	Crystal Frequency
44.1kHz	768x	33.8688MHz

Figure 27 shows a recommended oscillator circuit using a 3rd overtone crystal. The crystal must be specified with effective series resistance (ESR) of 40Ω or less for correct oscillator operation.

Crystals meeting the specification of $ESR \leq 40\Omega$ are usually available only in the full size HC49/U package. Half-size or surface mount crystals may not meet this specification and require a different oscillator circuit with inductor for correct operation.

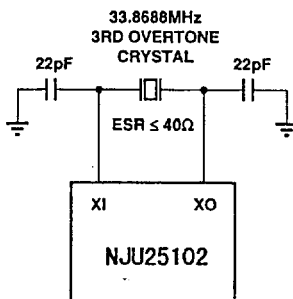


Figure 27. Suggested 33.8688MHz Crystal Oscillator Circuit

An external 33.8688MHz clock can be connected to NJU25102 XI pin in place of the crystal oscillator as shown in Figure 28. pin XO does not require connection but can be used as a buffered output.

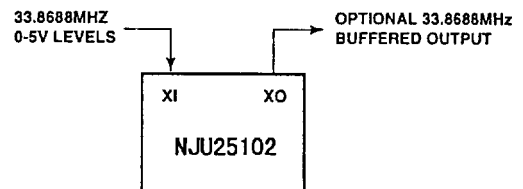


Figure 28. Driving with External 33.8688 MHz Source



Device Command Set

Commands are entered via the microcontroller (MPU) interface. Commands are one byte (8 bits) in length; however some commands must be followed with a sequence of one or more bytes containing data.

Commands are categorized into the three groups of Global Commands, Karaoke Commands, and Music Processor Commands.

Global Commands include the System State Download Command which initializes the NJU25102 digital audio interface and external memory parameters. The global Mode Select command establishes the primary operating mode (Karaoke or Music Processor). Music Input trimmer levels are also set by a global command as the music trimmer is common to both Karaoke and Music Processor modes.

The global Mode Select command changes the mode of NJU25102 audio signal processing and interpretation of subsequent command bytes. Setting Mode Select to Karaoke mode causes Karaoke functions and microphone digital inputs to become active. Subsequent command bytes are interpreted to enable Karaoke functions according to the Karaoke Command table.

Setting Mode Select to Music Processor mode disables microphone inputs and causes the Music Processor Mode functions of either Graphic Equalizer or Soundfield Generator to become active. Subsequent commands are interpreted according to the Music Processor Command table.

Mode Select can be toggled between Karaoke mode and Music Processor mode without loss of function settings in either mode.

Initialization

The following procedure is recommended to start up and initialize NJU25102 :

- 1) Apply power (VDD) to NJU25102 .
- 2) Hold $\overline{\text{RES}}$ pin (pin 13) Low until clock oscillator signal at X1 pin (pin 64) is stable. Crystal oscillators generally requires 10ms after power is applied to stabilize.
- 3) Set $\overline{\text{RES}}$ pin High.
- 4) Send System State Download command (3 bytes) to configure NJU25102 for hardware application. NJU25102 begins operation in Karaoke mode with Karaoke functions set according to the start up settings in the Command Table Summary (pages 37, 38)



Global Commands

System State Down Load (3 Bytes)

After power is applied and a hardware reset is generated on the RES pin (pin 13) a System State Download command must be sent from the host microcontroller to configure the NJU25102 hardware settings. This command controls the digital audio interface format, clock generator outputs, and configuration of the external memory interface. Settings for this command must be determined according to the circuit in which NJU25102 is installed.

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Instruction Code

7	6	5	4	3	2	1	0
SCKI	LRI	SCKO	LRO	MS	ADSCK	ADMCK	0

Data Byte 1

7	6	5	4	3	2	1	0
FMT1	FMT0	MSIZE1	MSIZE0	MTYPE	MWIDE	0	0

Data Byte 2

	0	1
SCKI		
LRI		
SCKO		
LRO		
MS	Master	Slave
ADSCK	32fs	64fs
ADMCK	384fs	256fs

FMT1	FMT0	Digital Audio Data Format
0	0	Right justified
0	1	I ² S
1	1	Left justified

MSIZE1	MSIZE0	(DRAM)	(SRAM)
0	0	64K	8K
0	1	256K	32K
1	0	1M	128K

	MTYPE	MWIDE
0	DRAM	4-bit
1	SRAM	8-bit

- LRI Assignment of Lch & Rch to audio input frame.
- SCKI Serial clock input. Data is clocked in on active edge.
- LRO Assignment of Lch & Rch to audio output frame.
- SCKO Serial clock output. Data changes on active edge.
- MS Master or slave mode serial clock out (SCKO).
- ADMCK Master clock for A/D and D/A converters.
- ADSCK Serial data clock for A/D and D/A converters.
- FMT1, 0 Serial digital audio data format for A/D and D/A converters.
- MSIZE0, Selection of external memory address size.
- MSIZE1 This is address space size of the individual memory devices.
- MTYPE Selection of external memory type.
- MWIDE Selection of bit width of external memory.
Set MWIDE = 1 if NJU25102 MD4-MD7 pins connected to external memory.

Global Commands (Continued)

Mode Select

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	MODE

Karaoke Mode 0
Music Processor Mode 1

Music Input Trim

7	6	5	4	3	2	1	0
1	1	L/R	TR4	TR3	TR2	TR1	TR0

1 – RIGHT
0 – LEFT

TR4 – 0: Input trim level of channel selected by L/R bit.
Signal will be clipped if it is overrange.

TR	Trim Level
4 3 2 1 0	
0 0 0 0 0	-∞dB (OFF)
0 0 0 0 1	-30dB
⋮	⋮
1 1 1 1 0	-1dB
1 1 1 1 1	+0dB

All steps are 1dB.

Karaoke Commands

Microphone Input Trim

7	6	5	4	3	2	1	0
1	0	MIC	TR4	TR3	TR2	TR1	TR0

1 – MIC 2
0 – MIC 1

TR4 – 0: Input trim level of channel selected by L/R bit.
Signal will be clipped if it is over range.

TR	Trim Level
4 3 2 1 0	
0 0 0 0 0	-∞dB (OFF)
0 0 0 0 1	-30dB
⋮	⋮
1 1 1 1 0	-1dB
1 1 1 1 1	+0dB

All steps are 1dB.

Microphone Echo Level

7	6	5	4	3	2	1	0
0	0	1	MIC	EC3	EC2	EC1	EC0

1 – MIC 2
0 – MIC 1

EC	ECHO LEVEL
3 2 1 0	
0 0 0 0	-∞dB
0 0 0 1	-28dB
⋮	⋮
1 1 1 0	-2dB
1 1 1 1	-0dB

All steps are 2dB.

**Microphone Echo Delay (3 Bytes)**

7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0

Instruction Byte

7	6	5	4	3	2	1	0
U7	U6	U5	U4	U3	U2	U1	U0

Data Byte 1

7	6	5	4	3	2	1	0
L7	L6	L5	L4	L3	L2	L1	L0

Data Byte 2

DELAY format is a 16 bit word where U7-0 is upper byte and L7-0 is lower byte. Allowed delay range is 0000(Hex) to 24FE(Hex). DELAY units are sample clock interval (1/Fs). Therefore the microphone echo delay time equals the DELAY setting divided by sample rate Fs

$$\text{Delay time (mS)} = \text{DELAY}/F_s(\text{kHz})$$

Example: Maximum delay time setting at 44.1kHz sample rate is $24FE(\text{Hex})/F_s = 9470/44.1 = 214.7\text{mS}$.

Microphone Echo Repeat (3 Bytes)

7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1

Instruction Byte

7	6	5	4	3	2	1	0
U7	U6	U5	U4	U3	U2	U1	U0

Data Byte 1

7	6	5	4	3	2	1	0
L7	L6	L5	L4	L3	L2	L1	L0

Data Byte 2

REPEAT format is 16 bit word where U7-0 is upper byte and L7-0 is lower byte. REPEAT is a bipolar gain value which ranges from -1 (inverting unity) to +1 (non-inverting unity). REPEAT is coded in a two byte, twos-complement code where 8000(Hex) corresponds to -1 and 7FFF(Hex) corresponds to +1 (0.99997).

The most useful REPEAT values for audio echo are in the range of 0.00 to 0.80 (0000(Hex) to 6666(Hex)).

Examples:

setting	REPEAT code	echo repeat effect
0.00	0000(Hex)	single echo – no repeat
0.40	3333(Hex)	short – approximately 3 repeats
0.60	4CCC (Hex)	long – approximately 7 repeats



Key Control Mode

7	6	5	4	3	2	1	0
0	1	0	0	0	1	M1	M0
						MUSIC KEY CONTROL	0 0
						MICROPHONE VOICE CHANGER	1 0
						MICROPHONE VOCAL HARMONY	1 1

Key control can be applied to either the music signal (MUSIC KEY CONTROL) or the microphone signal (MICROPHONE VOICE CHANGER). MICROPHONE VOCAL HARMONY mode adds shifted and non-shifted vocals together to create a harmony. Use Microphone Harmony Levels command to set shifted and non-shifted vocal levels when MICROPHONE VOCAL HARMONY mode is enabled.

Always issue new Pitch Shift command after changing Key Control Mode.

To turn off all Key Control modes set Pitch Shift to ZERO semi-notes (command: 0101 0000).

Pitch Shift

7	6	5	4	3	2	1	0
0	1	0	1	PS3	PS2	PS1	PS0

PS3-0: Key control pitch shift for mode selected by Key Control Mode command.

Key control function: $f_{\text{shift}} = f_{\text{IN}} \times 2^{n/12}$ where n is pitch shift in semi-notes.

PS 3 2 1 0	Pitch Shift
0 1 1 1	+7 semi note
0 1 1 0	+6 semi note
:	:
0 0 0 1	+1 semi note
0 0 0 0	0 semi note
1 1 1 1	-1 semi note
:	:
1 0 0 0	-8 semi note

Microphone Harmony Levels

7	6	5	4	3	2	1	0
0	1	1	VOC	LVL3	LVL2	LVL1	LVL0
			1 - SHIFTED VOCAL				
			0 - NON-SHIFTED VOCAL				

LVL 3 2 1 0	VOCAL LEVEL
0 0 0 0	-∞dB
0 0 0 1	-28dB
:	:
1 1 1 0	-2dB
1 1 1 1	-0dB

All steps are 2dB

LVL3-0: Level of SHIFTED VOCAL or NON-SHIFTED vocal as determined by VOC bit.

Settings of this command have effect only when MICROPHONE VOCAL HARMONY is selected via Key Control Mode command.

Vocal Fader/Multiplex

7	6	5	4	3	2	1	0	
0	0	0	0	1	M1	M2	M3	
					VOCAL FADER	1	0	0
					AUTO VOCAL FADER	1	1	0
					MULTIPLEX – LEFT	1	0	1
					MULTIPLEX L+R	0	0	1
					AUTO MULTIPLEX L+R	0	1	1
					OFF	0	0	0

Sets vocal fader function or multiplex function for music channel processing.

Operation of AUTO VOCAL FADER and AUTO MULTIPLEX L+R are linked to MIC 1 and MIC 2 signal levels by MICROPHONE AUTO-SWITCH (see Figure 4).

MULTIPLEX L+R and AUTO MULTIPLEX L+R functions require setting of levels for combining left and right channel signals. See Multiplex L+R Mix Levels command.

Multiplex L+R Mix Levels (5 Bytes)

7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	ST

OFF STATE L+R MIX 0

ON STATE L+R MIX 1

Instruction Byte

7	6	5	4	3	2	1	0
LU7	LU6	LU5	LU4	LU3	LU2	LU1	LU0

Data Byte 1

7	6	5	4	3	2	1	0
LL7	LL6	LL5	LL4	LL3	LL2	LL1	LL0

Data Byte 2

7	6	5	4	3	2	1	0
RU7	RU6	RU5	RU4	RU3	RU2	RU1	RU0

Data Byte 3

7	6	5	4	3	2	1	0
RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0

Data Byte 4

Sets levels of left channel and right channel signal mixing for MULTIPLEX L+R and AUTO MULTIPLEX L+R functions. Settings of this command have effect only for MULTIPLEX L+R and AUTO MULTIPLEX L+R functions.

There are two types of L+R Mix Level settings. The ON State L+R Mix is used by both the MULTIPLEX L+R function and by the AUTO MULTIPLEX L+R function for the case when microphone signals are sensed by the MICROPHONE AUTO-SWITCH (Auto Switch → ON). The OFF State L+R Mix is used only by the AUTO MULTIPLEX L+R function for the case when no microphone signals are detected by the MICROPHONE AUTO-SWITCH (Auto Switch → OFF). Settings for the OFF State L+R Mix or the ON State L+R Mix are loaded as determined by bit 0 of the instruction byte.

Referring to command format above, LEFT and RIGHT are 16 bit words where where LU7-0 is upper byte and LL7-0 is lower byte of LEFT word (data bytes 1 and 2), RU7-0 is upper byte and RL7-0 is lower byte of RIGHT word (data bytes 3 and 4). LEFT and RIGHT are unipolar gain values which range from 0 to +1. LEFT and RIGHT are coded in a two byte, twos-complement code where 0000(Hex) corresponds to 0 and 7FFF(Hex) corresponds to +1 (0.99997).

The mixed left and right channel signal is equal to: (LEFT x left channel input) + (RIGHT x right channel input).

It is recommended to set LEFT and RIGHT such that the L+R mix output is a constant-power sum of the two input channels (pan-pot function). To accomplish this set LEFT and RIGHT according to the relation:

$$LEFT^2 + RIGHT^2 = 1$$

Examples of constant-power (pan-pot) settings for LEFT/RIGHT:

Left/Right Channel Gains	LEFT data byte 1	LEFT 2	RIGHT 3	RIGHT 4
0.0dB left / -∞dB right	7F	FF	00	00
0.0dB left / -21dB right	7F	7E	0B	68
0.0dB left / -18dB right	7E	FB	10	1D
-0.1dB left / -15dB right	7D	F6	16	C3
-0.3dB left / -12dB right	7B	E5	20	27
-0.6dB left / -9dB right	77	AC	2D	6B
-1.3dB left / -6dB right	6E	C3	40	27
-3dB left / -3dB right	5A	82	5A	82
-6dB left / -1.3dB right	40	27	6E	C3
-9dB left / -0.6dB right	2D	6B	77	AC
-12dB left / -0.3dB right	20	27	7B	E5
-15dB left / -0.1dB right	16	C3	7D	F6
-18dB left / 0.0dB right	10	1D	7E	FB
-21dB left / 0.0dB right	0B	68	7F	7E
-∞dB left / 0.0dB right	00	00	7F	FF

Auto Fader/Auto Multiplex Timeout (3 Bytes)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Instruction Byte

7	6	5	4	3	2	1	0
U7	U6	U5	U4	U3	U2	U1	U0

Data Byte 1

7	6	5	4	3	2	1	0
L7	L6	L5	L4	L3	L2	L1	L0

Data Byte 2

Sets the delay from the time that MIC 1 and MIC 2 audio signals become silent to the time that Auto Fader or Auto Multiplex functions turn OFF. TIMEOUT is a parameter of the Microphone Auto-Switch which senses MIC.1 and MIC.2 signal levels.

TIMEOUT format is 16 bit word where U7-0 is upper byte and L7-0 is lower byte. Allowed TIMEOUT range is 0000(Hex) to 7FFF(Hex). TIMEOUT units are sixteen times the sample clock interval (16/Fs). Therefore the Auto Fader/Auto Multiplex Timeout time equals sixteen times the TIMEOUT setting divided by sample rate Fs

$$\text{Timeout time (sec)} = \frac{(16 \times \text{TIMEOUT})}{f_s}$$

$$= \frac{\text{TIMEOUT}}{2756} \quad (f_s = 44.1\text{kHz})$$

Example: Maximum timeout setting is

$$\frac{7FFF(\text{HEX})}{2756 \text{ (decimal)}} = \frac{32767}{2756} = 11.9 \text{ seconds}$$

Vocal Fader Manual Balance

7	6	5	4	3	2	1	0
0	0	0	1	L/R	A2	A1	A0

0 - R. CH.
 1 - L. CH.

Adjusts null point of Vocal Fader to optimize vocal cancellation.

Note: For correct operation, send command to insure that one channel is always set at 0dB when opposite channel is set to value other than 0dB.

A	L. CH/R. CH
2 1 0	
0 0 0	0dB
0 0 1	+0.5dB
⋮	⋮
1 1 1	+3.5dB

All steps sizes are 0.5dB

Example Sequence:

Command	Sets	Result
0 0 0 1 0 0 1 0	L-ch set to +1.0dB	
0 0 0 1 1 0 0 0	R-ch set to 0.0dB	L-ch 1.0dB > R-ch
0 0 0 1 0 0 0 0	L-ch set to 0.0dB	L-ch = R-ch
0 0 0 1 1 0 1 1	R-ch set to +1.5dB	R-ch 1.5dB > L-ch
0 0 0 1 1 1 1 1	R-ch set to +3.5dB	R-ch 3.5dB > L-ch

Fader/Auto Balance/Bass Boost

7	6	5	4	3	2	1	0
0	1	0	0	1	BAL	REV	BASS

1 - ON
 Auto Input Balance 0 - OFF
 1 - ON
 Vocal Fader Level Restore 0 - OFF
 1 - ON
 Dynamic Bass Boost 0 - OFF



Music Processor Commands

Commands are interpreted according to the following table after the Global Mode Select command is issued for Music Processor Mode (command: 0000 0011). Bypass mode passes Music Input data directly to the Audio Outputs. Data is unchanged except for a three sample delay.

Music Input Trim function is included in OFF, Soundfield Simulator, and Graphic Equalizer modes. Music input trim is not included in Bypass mode.

Graphic Equalizer/Soundfield Simulator

7	6	5	4	3	2	1	0
0	0	0	0	1	0	GEQ	SFLD

OFF -	0	0
Soundfield Simulator -	0	1
Graphic Equalizer -	1	0
Bypass Mode -	1	1

Graphic Equalizer/Band Gain (8 bytes)

Loads gain settings for the seven Graphic Equalizer frequency bands in sequence. Center frequencies of default graphic equalizer bands are: 30Hz, 80Hz, 250Hz, 650Hz, 2kHz, 6kHz, and 15kHz for sample rate (Fs) of 44.1kHz. If 32kHz sample rate is chosen then Equalizer band center frequencies become 30Hz, 80Hz, 250Hz, 650Hz, 2kHz, 5kHz, and 10kHz.

This command consists of an instruction byte followed by seven single byte values for band gain settings starting with the lowest frequency band (30Hz).

7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	1

Byte values for band gains are set according to the table.

B7-B0	BAND GAIN
0 0 0 0 1 1 0 0	0dB
0 0 0 0 1 0 1 1	-1dB
:	:
0 0 0 0 0 0 0 1	-11dB
0 0 0 0 0 0 0 0	-12dB
1 1 1 1 1 1 1 1	-13dB
:	:
1 1 1 1 0 1 0 1	-23dB
1 1 1 1 0 1 0 0	-24dB

All steps are 1dB

1. Instruction Code 11(Hex)
2. 30Hz band gain byte
3. 80Hz band gain byte
- :
8. 15kHz band gain byte

Graphic Equalizer Coefficients/Download

Custom graphic equalizer bands can be implemented with the NJU25102 Coefficients for the biquad bandpass filters can be downloaded to set center frequencies and Q factor as desired. From two to seven equalizer bands are supported. Contact Medianix for Contact New Japan Radio Co.,Ltd for information on design and download of custom filter coefficients.



Soundfield Simulator Coefficients — Download

Loads values for the twelve Soundfield Simulator coefficients in sequence: OFST0–OFST3, ATTO–ATT3, and COE0–COE3 to implement a custom configuration of the soundfield simulator. Refer to Figure 10. Soundfield Simulator.

This command consists of an instruction byte followed by twelve, two-byte values for the soundfield simulator coefficients.

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0

1. Instruction Code 12(Hex)
2. OFST0 upper byte
3. OFST0 lower byte
4. OFST1 upper byte
5. OFST1 lower byte
6. OFST2 upper byte
7. OFST2 lower byte
8. OFST3 upper byte
9. OFST3 lower byte
10. ATTO upper byte
11. ATTO lower byte
12. ATT1 upper byte
13. ATT1 lower byte
14. ATT2 upper byte
15. ATT2 lower byte
16. ATT3 upper byte
17. ATT3 lower byte
18. COE0 upper byte
19. COE0 lower byte
20. COE1 upper byte
21. COE1 lower byte
22. COE2 upper byte
23. COE2 lower byte
24. COE3 upper byte
25. COE3 lower byte

OFST0–OFST3 are values of the four audio delay taps. OFSTx is sent as a two byte code. Delay associated with each tap equals the OFSTx setting divided by sample rate Fs: Delay (ms) = OFSTx/Fs (kHz).

Audio Delay is implemented in external RAM. Maximum allowed OFSTx codes are a function of memory size as shown below:

External RAM Size	Maximum OFSTx Code	Maximum Delay (Fs = 44.1kHz)
256kbits	3FFE(Hex)	371.5ms
512kbits	7FFE(Hex)	743.0ms
1024kbits	FFFF(Hex)	1.486sec

COE0–COE3, ATTO–ATT3 are bipolar gain values which range from –1 (inverting unity) to +1 (non-inverting unity). COEx and ATTx are coded in a two byte, two's-complement code where 8000(Hex) corresponds to –1 and 7FFF(Hex) corresponds to +1 (0.99997).

To program positive gain values (0.0 to 0.99997):
COEx or ATTx = 8000(Hex) x gain setting

To program negative gain values (–1.0 to –0.00003):
COEx or ATTx = 10000(Hex) – [8000(Hex) x gain setting]

Examples:

Gain Setting	COEx or ATTx Code
–1.0	8000(Hex)
–0.054	F916(Hex)
0.0	0000(Hex)
+0.485	3E14(Hex)
+0.99997	7FFF(Hex)

Soundfield Simulator Coefficients — Hall Mode

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	1

This command sets the twelve Soundfield Simulator coefficients: OFST0–OFST3, ATTO–ATT3, and COE0–COE3 to pre-stored values designed for Hall mode.

The maximum audio delay tap for this soundfield is less than 3FFE(Hex). External memory required is no greater than 256kbits.



Command Table Summary and Start-up Values

Device reset (RES/pin 13) initializes the NJU25102 according to the values in the command table below. Note that parameters associated with the global command system state download (digital audio

interface, memory size, etc.) are not altered at reset. These must be initialized via the command interface when the device is powered up.

Global Commands

Command Bits								Function	Startup/Reset State	
7	6	5	4	3	2	1	0		Code	Value
0	0	0	0	0	0	0	0	System Download Command (3 bytes)		
0	0	0	0	0	0	1	A	Mode Select: 0 = Karaoke 1 = Music Processor	0	Karaoke
1	1	A	B	B	B	B	B	A = L/R Music Input Trimmer: 0 = L, 1 = R B = 5-bit Trim Level	1 1 0 0 1	-6dB (L/R ch)

Karaoke Commands

Command Bits								Function	Startup/Reset State	
7	6	5	4	3	2	1	0		Code	Value
0	0	0	0	0	0	0	1	Auto Fader/Auto Multiplex Timeout (3 bytes)	25AEH	3.5s
0	0	0	0	1	A	B	C	ABC = Vocal Fader/Multiplex mode 000 = Off 100 = Vocal Fader 110 = Auto Vocal Fader 101 = Multiplex — Left 001 = Multiplex L+R 011 = Auto Multiplex L=R	0 0 0	All Off
0	0	0	1	A	B	B	B	Vocal Fader Manual Balance A = Channel: 0 = R, 1 = L B = 3-bit setting	0 0 0	0dB (L/R ch)
0	0	1	A	B	B	B	B	A = Microphone Echo, 0 = Mic 1, 1 = Mic 2 B = Mic Echo Level, 4-bit setting	0 0 0 0	-∞dB (L/R ch)
0	1	0	0	0	0	0	0	Microphone Echo Delay (3 bytes)	2400H	t _{DELAY} = 209ms*
0	1	0	0	0	0	0	1	Microphone Echo Repeat (3 bytes)	37AEH	0.435
0	1	0	0	0	0	1	A	Multiplex, L+R Mix levels (5 bytes) A = 0: OFF State L+R Mix	5A82H 5A82H	-3dB (L ch) -3dB (R ch)
								A = 1: ON State L+R Mix	7FFFH 0000H	0dB (L ch) -∞dB (R ch)

**Karaoke Commands** (continued)

Command Bits								Function	Startup/Reset State	
7	6	5	4	3	2	1	0		Code	Value
0	1	0	0	0	1	A	A	AA = Key Control Mode 00 = Music Key Control 10 = Microphone Voice Changer 11 = Microphone Vocal Harmony	0 0	Music Key Control
0	1	0	0	1	A	B	C	A = Auto Input Balance B = Fade Level Restorer C = Dynamic Bass Boost All: 0 = Off, 1 = On	0 0 0	All Off
0	1	0	1	A	A	A	A	A = Pitch Shift, 4-bit setting	0 0 0 0	No Pitch Shift
0	1	1	0	A	A	A	A	A = Harmony: Shifted Vocal, 4-bit setting	1 1 0 1	-4dB
0	1	1	1	A	A	A	A	A = Harmony: Non-shifted Vocal, 4-bit setting	1 1 0 1	-4dB
1	0	A	B	B	B	B	B	A = Microphone Trimmer: 0 = Mic 1, 1 = Mic 2 B = Mic Input Trim, 5-bit setting	1 1 0 0 1	-6dB (Mic 1/Mic 2)

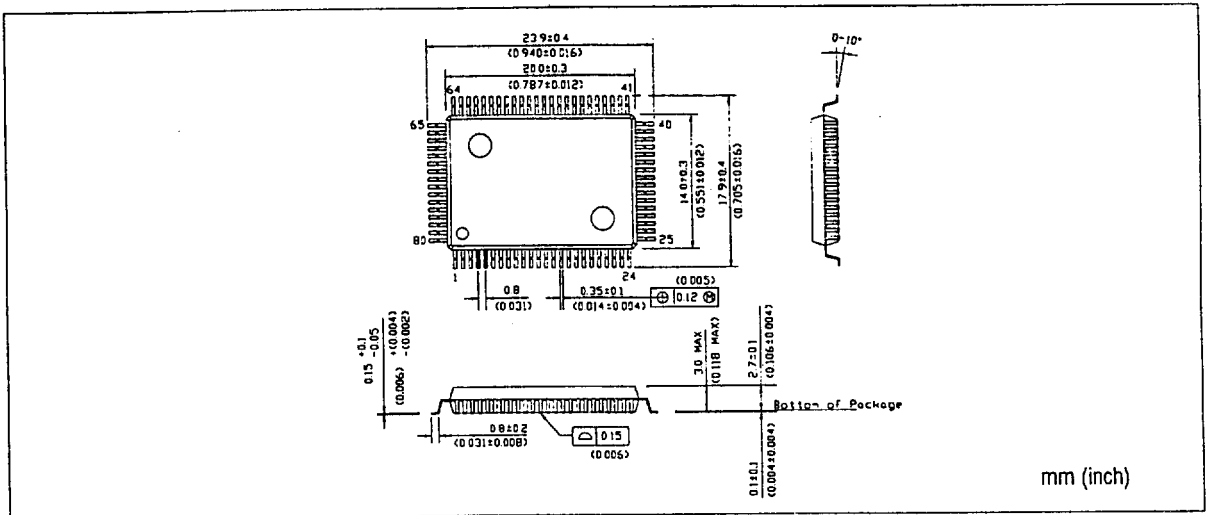
Music Processor Commands

Command Bits								Function	Startup/Reset State	
7	6	5	4	3	2	1	0		Code	Value
0	0	0	0	1	0	A	A	AA = Music Processor Mode 00 = OFF (Music Input Trim included) 01 = Soundfield Simulator 10 = Graphic Equalizer 11 = Bypass (Music Input Trim not included)	00	OFF
0	0	0	1	0	0	0	0	Graphic Equalizer Bandwidth Coefficient Download Followed by: 1 Byte to set number of bands 6 Bytes/Band to set bandwidth (Lowest frequency first)		7 Bands, 30Hz, 80Hz, 250Hz, 650Hz, 2kHz, 6kHz, 15kHz
0	0	0	1	0	0	0	1	Graphic Equalizer (8 bytes), Band Gain	OCH	All bands 0dB
0	0	0	1	0	0	1	0	Soundfield Simulator (25 bytes) 4 Delay times, 2 Bytes each 8 Sets of Gain values, 2 Bytes each		
0	0	0	1	0	0	1	1	Soundfield Simulator Coefficients — Hall Mode		Preset to Hall Mode

* 44.1kHz



Plastic QFP-80 Dimensions



Plastic QFP-80 Solder Pads

