Features

- **E^2 Programmable 65,536 x 1, 131,072 x 1, and 262,144 x 1 bit Serial Memories Designed To Store Configuration Programs For Programmable Gate Arrays**
- **Simple Interface to SRAM FPGAs Requires Only One User I/O Pin**
- **Compatible With AT6000 FPGAs, ATT3000 FPGA, EPF8000 FPGAs, ORCA FPGAs, XC2000, XC3000, XC4000, XC5000 FPGAs**
- **Cascadable To Support Additional Configurations or Future Higher-density Arrays (17C128 and 17C256 only)**
- **Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available In the Space-efficient Plastic DIP or Surface-mount PLCC and SOIC Packages**
- **In-system Programmable Via 2-Wire Bus**
- **Emulation of 24CXX Serial E^2PROMs**

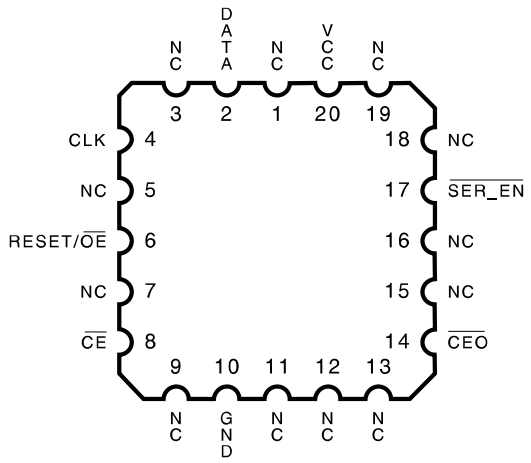
Description

The AT17C65/128/256 (AT17CXXX family) FPGA Configuration E^2PROMS (Configurator) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. Both the AT17C65 and the AT17C128 are packaged in the 8-pin DIP and the popular 20-pin Plastic Leaded Chip Carrier, and SOIC. The AT17C256 is available in 14-pin SOIC or 20-pin PLCC or SOIC packages. The AT17CXXX family uses a simple serial-access procedure to configure one or more FPGA devices. The AT17CXXX organization supplies enough memory to configure one or multiple smaller FPGAs. Using a special feature of the AT17CXXX, the user can select the polarity of the reset function by programming a special E^2PROM bit.

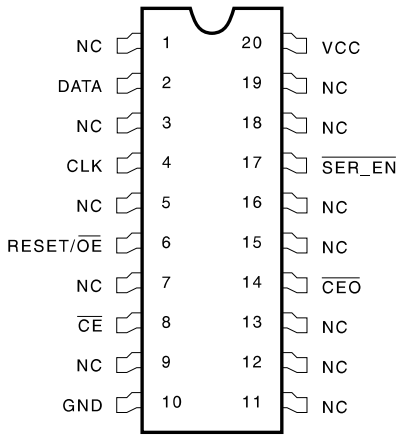
The AT17C65/128/256 can be programmed with the standard programmers from other manufacturers.

Pin Configurations

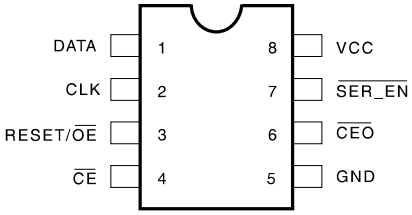
20-Pin PLCC



20-Pin SOIC



8-Pin DIP



FPGA Configuration E^2PROM

65K, 128K, and 256K

- **Please refer to Section 5, FPGA Configuration Memories, page 5-3 for complete AT17C65/128/256 data sheet.**

0391D

Controlling The AT17C65/128/256 Serial E²PROMs

Most connections between the FPGA device and the Serial E²PROM are simple and self-explanatory:

- The DATA output of the AT17C65/128/256 drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17C65/128/256.
- The $\overline{CEO}$ output of any AT17C128/256 drives the $\overline{CE}$ input of the next AT17C128/256 in a cascade chain of PROMs.
- $\overline{SER\_EN}$ must be connected to V_{CC}.

There are, however, two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$, as shown in the AC Characteristics Waveform.

Condition 1

The simplest connection is to have the FPGA D/$\overline{P}$ output drive both $\overline{CE}$ and RESET/$\overline{OE}$ in parallel. Due to its simplicity, however, this method will fail if the FPGA receives an external reset condition during the configuration cycle. If a system reset is applied to the FPGA, it will abort the original configuration and then reset itself for a new configuration, as intended. Of course, the AT17C65/128/256 does not see the external reset signal and will not reset its internal address counters and, consequently, will remain out of sync with the FPGA for the remainder of the configuration cycle.

Condition 2

The FPGA D/$\overline{P}$ output drives only the $\overline{CE}$ input of the AT17C65/128/256, while its $\overline{OE}$ input is driven by the inversion of the FPGA $\overline{RESET}$ input. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. A high level on the RESET/$\overline{OE}$ input to the AT17CXXX during FPGA reset clears the PROM internal address pointer, so that the reconfiguration starts at the beginning. The AT17C65/128/256 does not require an inverter since the RESET polarity is programmable.

Block Diagram