A DIVISION OF CIRRUS LOGIC

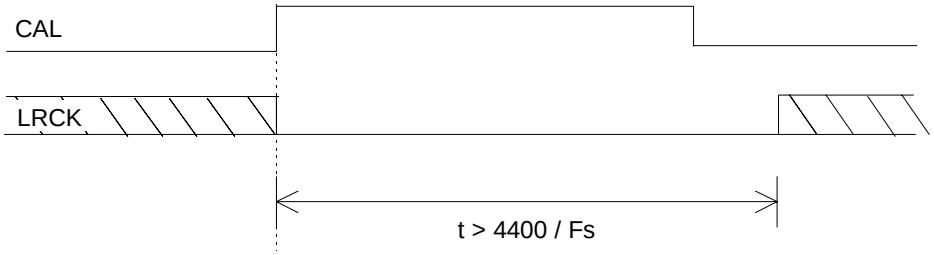
10/7/97

Errata: CS5396 Revision B

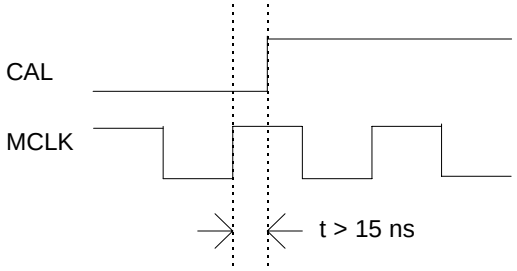
CS5396/CS5397 : 120 dB, 96 kHz Audio A/D Converter (DS229PP2 SEP '97)

This information is provided to document the performance of the CS5396 revision B silicon. These items will be fixed in revision C silicon.

- When in slave mode, the part must be calibrated with the LRCK low as in the following diagram:



- The rising edge of the CAL pin must lag the rising edge MCLK by at least 15 ns as in the diagram below:



If there are any questions concerning this information please call:

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