TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T C 7 M Z 5 7 3 F K

Low Voltage Octal D-Type Latch with 5 V Tolerant Inputs and Outputs

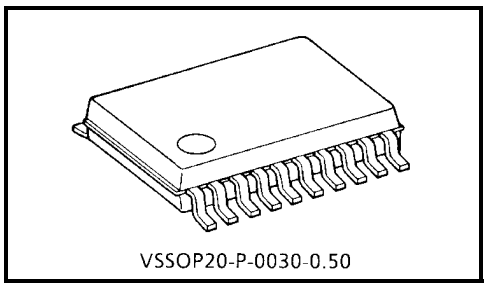
The TC7MZ573FK is a high performance CMOS octal D-type latch. Designed for use in 3.3 V systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5 V supply environment for both inputs and outputs.

This 8 bit D-type latch is controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.

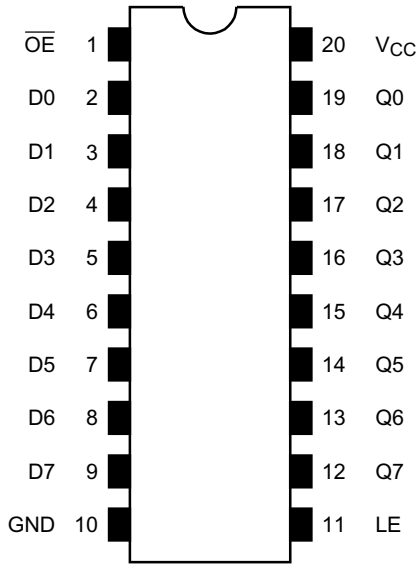


Weight: 0.03 g (typ.)

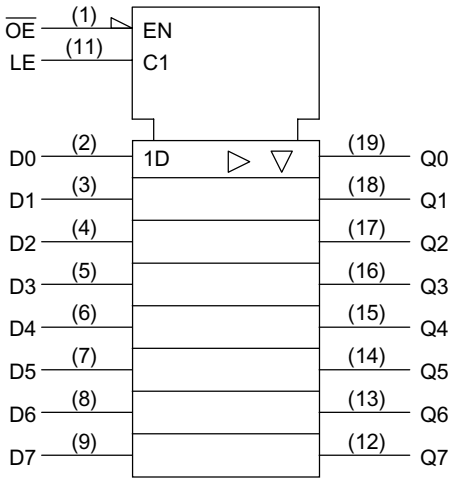
Features

- Low voltage operation: V_{CC} = 2.0~3.6 V
- High speed operation: t_{pd} = 8.0 ns (max) (V_{CC} = 3.0~3.6 V)
- Output current: $|I_{OH}|/I_{OL}$ = 24 mA (min) (V_{CC} = 3.0 V)
- Latch-up performance: ±500 mA
- Package: VSSOP (US20)
- Power down protection is provided on all inputs and outputs.
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 573 type.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

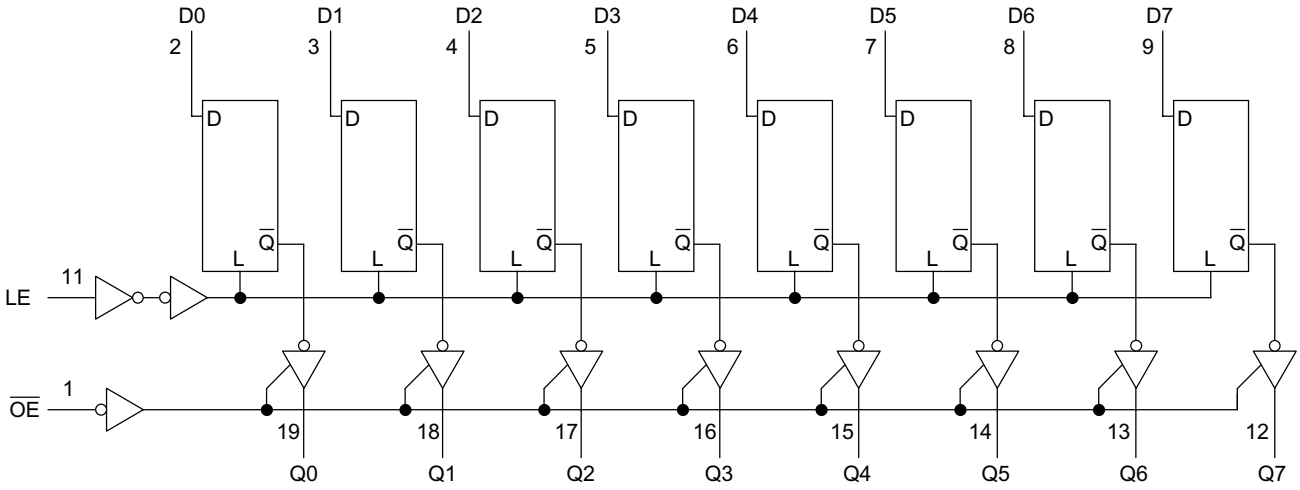
Inputs			Outputs
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Q_n: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5~7.0	V
DC input voltage	V_{IN}	−0.5~7.0	V
DC output voltage	V_{OUT}	−0.5~7.0 (Note1)	V
		−0.5~V_{CC} + 0.5 (Note2)	
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note3)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	180	mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65~150	°C

Note1: Output in off-state

Note2: High or low state. I_{OUT} absolute maximum rating must be observed.

Note3: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0~3.6	V
		1.5~3.6 (Note4)	
Input voltage	V_{IN}	0~5.5	V
Output voltage	V_{OUT}	0~5.5 (Note5)	V
		0~V_{CC} (Note6)	
Output current	I_{OH}/I_{OL}	±24 (Note7)	mA
		±12 (Note8)	
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~10 (Note9)	ns/V

Note4: Data retention only

Note5: Output in off-state

Note6: High or low state

Note7: V_{CC} = 3.0~3.6 V

Note8: V_{CC} = 2.7~3.0 V

Note9: V_{IN} = 0.8~2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = –40~85°C)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	High level	V_{IH}	—		2.7~3.6	2.0	—	V
	Low level	V_{IL}	—		2.7~3.6	—	0.8	
Output voltage	High level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 μA	2.7~3.6	V_{CC} – 0.2	—	V
				I_{OH} = –12 mA	2.7	2.2	—	
				I_{OH} = –18 mA	3.0	2.4	—	
				I_{OH} = –24 mA	3.0	2.2	—	
	Low level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	2.7~3.6	—	0.2	
				I_{OL} = 12 mA	2.7	—	0.4	
				I_{OL} = 16 mA	3.0	—	0.4	
				I_{OL} = 24 mA	3.0	—	0.55	
Input leakage current		I_{IN}	V_{IN} = 0~5.5 V		2.7~3.6	—	±5.0	μA
3-state output off-state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~5.5 V		2.7~3.6	—	±5.0	μA
Power off leakage current		I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	—	10.0	μA
			V_{IN}/V_{OUT} = 3.6~5.5 V		2.7~3.6	—	±10.0	
Increase in I_{CC} per input		ΔI_{CC}	V_{IH} = V_{CC} – 0.6 V		2.7~3.6	—	500	

AC Characteristics (Ta = –40~85°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time (D-Q)	t_{pLH} t_{pHL}	Figure 1, Figure 2	2.7	—	9.0	ns
			3.3 ± 0.3	1.5	8.0	
Propagation delay time (LE-Q)	t_{pLH} t_{pHL}	Figure 1, Figure 2	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 3	2.7	—	9.5	ns
			3.3 ± 0.3	1.5	8.5	
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	2.7	—	7.0	ns
			3.3 ± 0.3	1.5	6.5	
Minimum pulse width (LE)	$t_{w\ (H)}$	Figure 1, Figure 2	2.7	3.3	—	ns
			3.3 ± 0.3	3.3	—	
Minimum set-up time	t_s	Figure 1, Figure 2	2.7	2.5	—	ns
			3.3 ± 0.3	2.5	—	
Minimum hold time	t_h	Figure 1, Figure 2	2.7	1.5	—	ns
			3.3 ± 0.3	1.5	—	
Output to output skew	t_{osLH} t_{osHL}	(Note10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

Note10: This parameter is guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Dynamic Switching Characteristics
(Ta = 25°C, Input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500\ \Omega$)

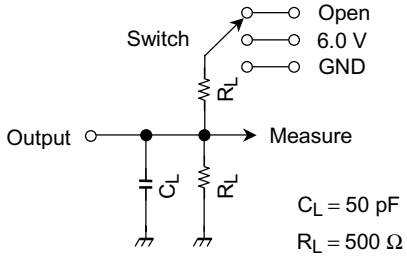
Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
Quiet output minimum dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—	3.3	7	pF
Output capacitance	C_{OUT}	—	3.3	8	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz (Note11)	3.3	25	pF

Note11: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V
t_{pHZ}, t_{pZH}	GND
t_w, t_s, t_h	Open

Figure 1

AC Waveform

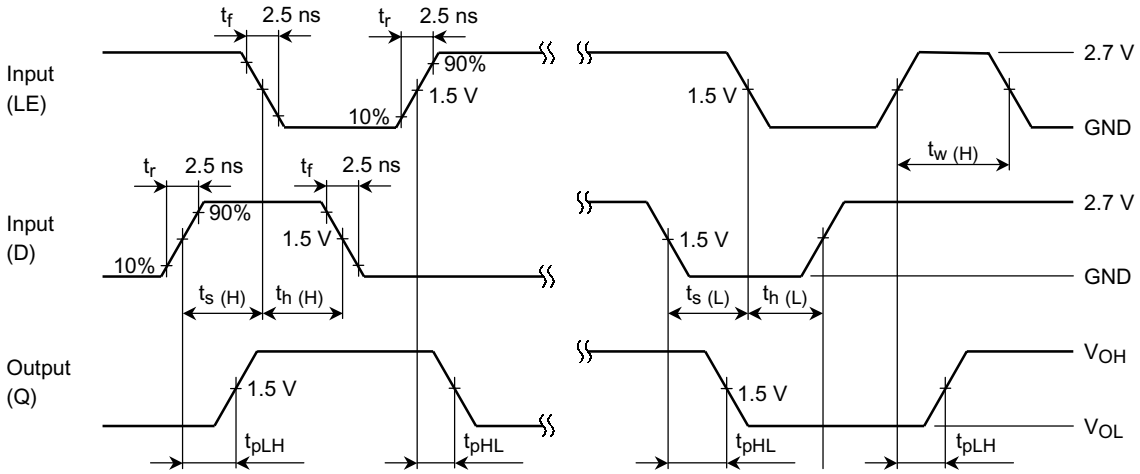


Figure 2 t_{pLH}, t_{pHL}, t_w, t_s, t_h

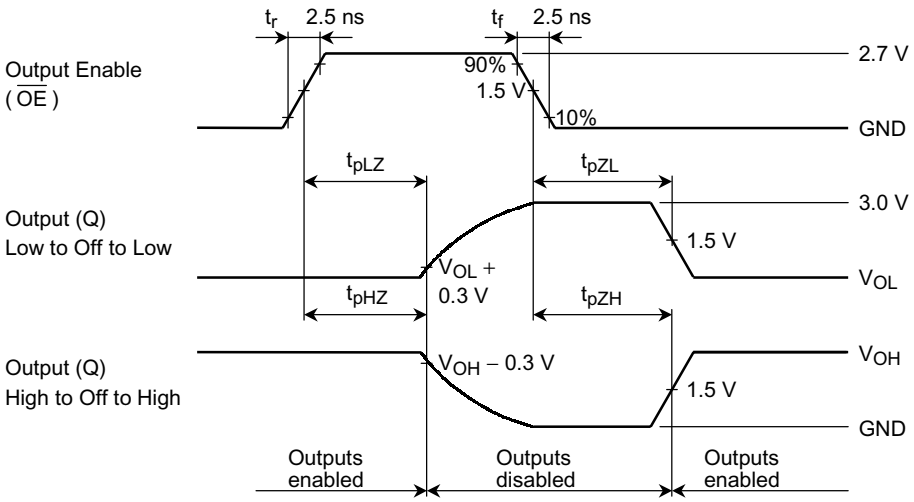
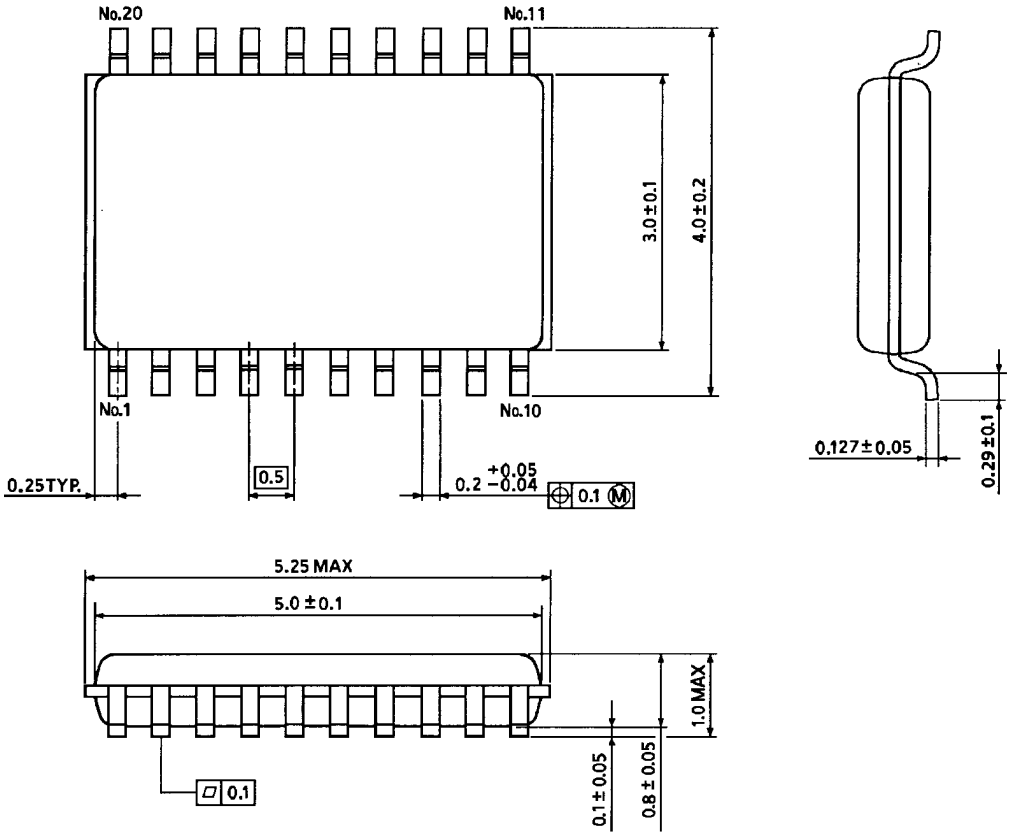


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Package Dimensions

VSSOP20-P-0030-0.50 Unit : mm



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