# M5M29GB/T161BWG

**16,777,216-BIT (1048,576-WORD BY16-BIT)**
**CMOS 3.3V-ONLY, BLOCK ERASE FLASH MEMORY**

## DESCRIPTION

The MITSUBISHI Mobile FLASH M5M29GB/T161BWG are 3.3V-only high speed 16,777,216-bit CMOS boot block Flash Memories with alternating BGO (Back Ground Operation) feature. The BGO feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank. This BGO feature is suitable for mobile and personal computing, and communication products. The M5M29GB/T161BWG are fabricated by CMOS technology for the peripheral circuits and DINOR(Divided bit line NOR) architecture for the memory cells, and are available in 6x8-balls CSP (0.75mm ball pitch) .

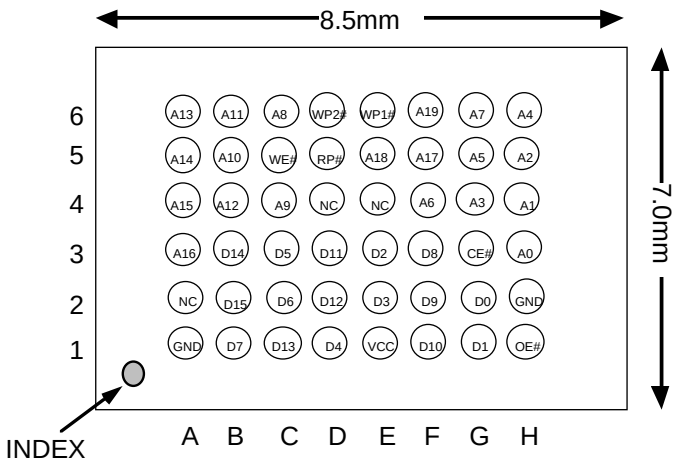
## FEATURES

- Organization ..... 1048,576 word x 16bit (M5M29GB/T161BWG)
- Supply voltage ..... $V_{CC}$ = 2.7~3.6V
- Access time ..... 90ns (Max.)
- Power Dissipation
  - Read ..... 54 mW (Max. at 5MHz)
  - (After Automatic Power saving) ..... 0.33µW (typ.)
  - Program/Erase ..... 126 mW (Max.)
  - Standby ..... 0.33µW (typ.)
  - Deep power down mode ..... 0.33µW (typ.)
- Auto program for Bank(I)
  - Program Time ..... 4ms (typ.)
  - Program Unit
    - (Byte Program) ..... 1word
    - (Page Program) ..... 128word
- Auto program for Bank(II)
  - Program Time ..... 4ms (typ.)
  - Program Unit ..... 128word
- Auto Erase
  - Erase time ..... 40 ms (typ.)
  - Erase Unit
    - Bank(I) Boot Block ..... 16Kword x 1
    - Parameter Block ..... 16Kword x 7
    - Bank(II) Main Block ..... 32Kword x 28
- Program/Erase cycles ..... 100Kcycles
- Boot Block
  - M5M29GB161BWG ..... Bottom Boot
  - M5M29GT161BWG ..... Top Boot
- Other Functions
  - Soft Ware Command Control
  - Selective Block Lock
  - Erase Suspend/Resume
  - Program Suspend/Resume
  - Status Register Read
  - Alternating Back Ground Program/Erase Operation Between Bank(I) and Bank(II)
- Package
  - 7mm x 8.5mm CSP (Chip Scale Package)
  - 6 x 8 balls, 0.75mm ball pitch

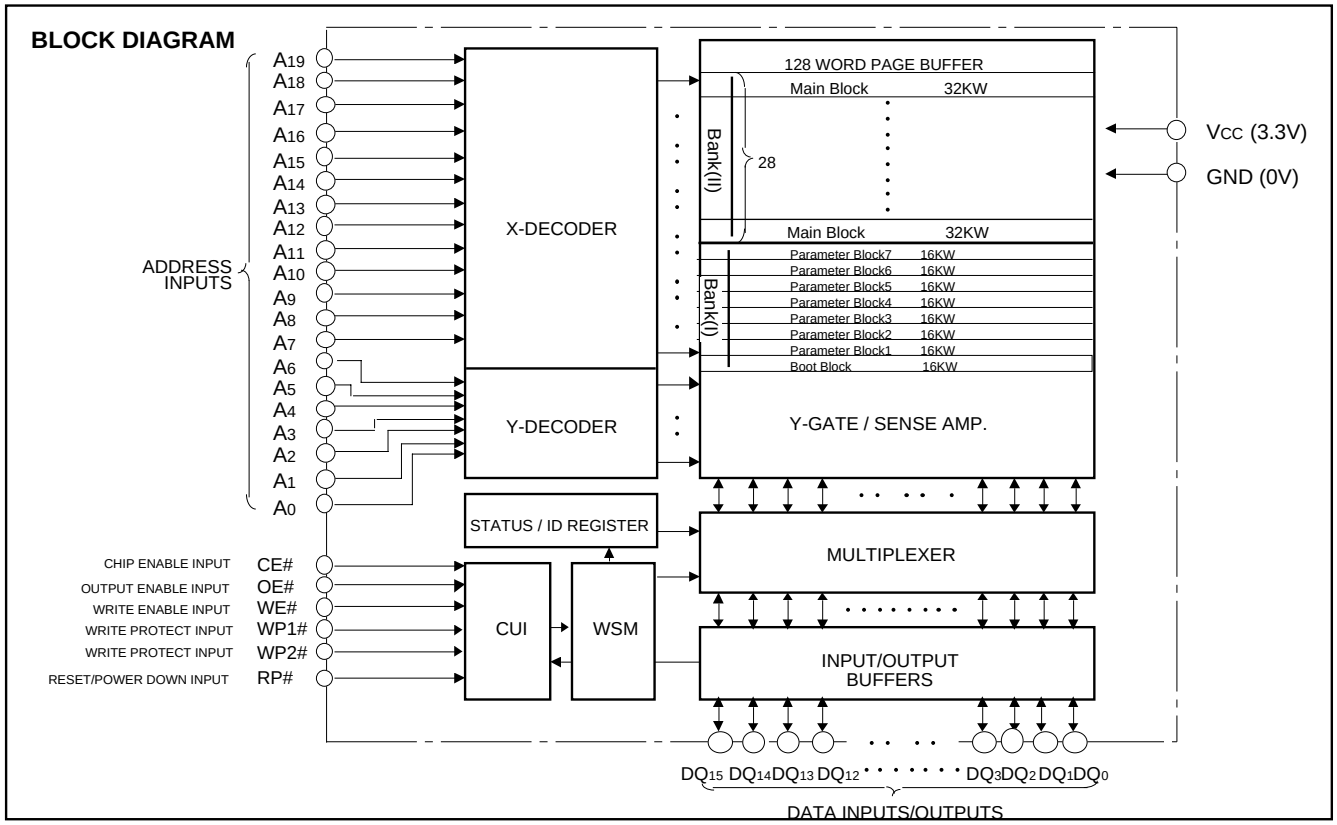
## APPLICATION

Digital Cellular Phone
Telecommunication
Mobile Computing Machine
PDA (Personal Digital Assistance)
Car Navigation System
Video Game Machine

## PIN CONFIGURATION (TOP VIEW)




M5M29GB/T161BWG
CSP(0.75mm ball pitch):48FJA
16-bit version NC : NO CONNECTION




M5M29GB/T161BWG (16 bit version)

## FUNCTION

The M5M29GB/T161BWG includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and byte/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.
A Deep Powerdown mode is enabled when the RP# pin is at GND, minimizing power consumption.

**Read**
The M5M29GB/T161BWG has three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the M5M29GB/T161BWG automatically resets to read array mode. In the read array mode, low level input to CE# and OE#, high level input to WE# and RP#, and address signals to the address inputs (A19-A0:M5M29GB/T161BWG) output the data of the addressed location to the data input/output (D15-D0:M5M29 GB/T161BWG).

**Write**
Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing WE# to low level, while CE# is at low level and OE# is at high level. Address and data are latched on the earlier rising edge of WE# and CE#. Standard micro-processor write timings are used.

**Alternating Background Operation (BGO)**
The M5M29GB/T161BWG allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Read array operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in software command write cycling or the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation.

**Output Disable**
When OE# is at VIH, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

**Standby**
When CE# is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

**Deep Power-Down**
When RP# is at VIL, the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/ output are in a high-impedance(High-Z) state. After return from powerdown, the CUI is reset to Read Array , and the Status Register is cleared to value 80H.
During block erase or program modes, RP# low will abort either operation. Memory array data of the block being altered become invalid.

**Automatic Power-Saving (APS)**
The Automatic Power-Saving minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or CE# isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. While in this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

**SOFTWARE COMMAND DEFINITIONS**

The device operations are selected by writing specific software command into the Command User Interface.

**Read Array Command** (FFH)

The device is in Read Array mode on initial device power up and after exit from deep powerdown, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

**Read Device Identifier Command** (90H)

It can normally read device identifier codes when Read Device Identifier Code Command(90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from address 0000H and 0001H, respectively.

**Read Status Register Command** (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.

The contents of Status Register are latched on the later falling edge of OE# or CE#. So CE# or OE# must be toggled every status read.

**Clear Status Register Command** (50H)

The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

**Block Erase / Confirm Command** (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

**Program Commands**

**A)Word Program (40H)**

Word program is executed by a two-command sequence. The Word Program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation. The Word Program Command is Valid for only Bank(I).

**B)Page Program for Data Blocks (41H)**

Page Program for Bank(I) and Bank(II) allows fast programming of 128words of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 129th cycle , write data must be serially inputted. Address A6-A0 have to be incremented from 00H to 7FH. After completion of data loading, the WSM controls the program pulse application and verify operation.

**C)Single Data Load to Page Buffer (74H) / Page Buffer to Flash (0EH/D0H)**

Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address and data. Distinct data up to 128word can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programing the data on the page buffer is cleared automatically.

This command is valid for only Bank(I) alike Word Program.

**Clear Page Buffer Command** (55H)

Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

**Suspend/Resume Command** (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

**DATA PROTECTION**

The M5M29GB/T161BWG provides selectable block locking of memory blocks. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the M5 M29GB/T161BWG have a master Write Protect pin (WP1# & WP2 #) which prevents any modifications to memory blocks whose lock-bits are set to "0", when WP1# or WP2# is low. When WP1# & WP2# are high , all blocks can be programmed or erased regardless of the state of the lock-bits, and the lock-bits are cleared to "1" by erase. See the BLOCK LOCKING table on P.9 for details.

**Power Supply Voltage**

When the power supply voltage (Vcc) is less than $V_{LKO}$, Low $V_{CC}$ Lock-Out voltage, the device is set to the Read-only mode. Regarding DC electrical characteristics of $V_{LKO}$, see P.9

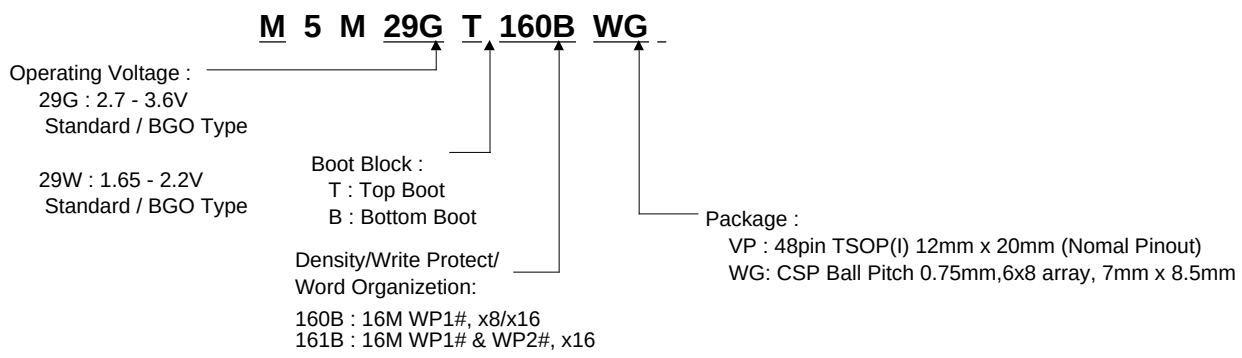
A delay time of 2 us is required before any device operation is initiated. The delay time is measured from the time Vcc reaches Vccmin (2.7V).

During power up, RP#=GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

**MEMORY ORGANIZATION**

The M5M29GB/T161BWG has one 16Kword boot block, seven 16 Kword parameter blocks, for Bank(I) and twenty-eight 32Kword main blocks for Bank(II). A block is erased independently of other blocks in the array.

**Mitsubishi 16M Flash Memory Type name**



**MEMORY ORGANIZATION**

x16 ( Wordmode)

| | | |
|---|---|---|
| F8000H-FFFFFH | 32Kword MAIN BLOCK 35 | BANK(II) |
| F0000H-F7FFFH | 32Kword MAIN BLOCK 34 | |
| E8000H-EFFFFH | 32Kword MAIN BLOCK 33 | |
| E0000H-E7FFFH | 32Kword MAIN BLOCK 32 | |
| D8000H-DFFFFH | 32Kword MAIN BLOCK 31 | |
| D0000H-D7FFFH | 32Kword MAIN BLOCK 30 | |
| C8000H-CFFFFH | 32Kword MAIN BLOCK 29 | |
| C0000H-C7FFFH | 32Kword MAIN BLOCK 28 | |
| B8000H-BFFFFH | 32Kword MAIN BLOCK 27 | |
| B0000H-B7FFFH | 32Kword MAIN BLOCK 26 | |
| A8000H-AFFFFH | 32Kword MAIN BLOCK 25 | |
| A0000H-A7FFFH | 32Kword MAIN BLOCK 24 | |
| 98000H-9FFFFH | 32Kword MAIN BLOCK 23 | |
| 90000H-97FFFH | 32Kword MAIN BLOCK 22 | |
| 88000H-8FFFFH | 32Kword MAIN BLOCK 21 | |
| 80000H-87FFFH | 32Kword MAIN BLOCK 20 | |
| 78000H-7FFFFH | 32Kword MAIN BLOCK 19 | |
| 70000H-77FFFH | 32Kword MAIN BLOCK 18 | |
| 68000H-6FFFFH | 32Kword MAIN BLOCK 17 | |
| 60000H-67FFFH | 32Kword MAIN BLOCK 16 | |
| 58000H-5FFFFH | 32Kword MAIN BLOCK 15 | |
| 50000H-57FFFH | 32Kword MAIN BLOCK 14 | |
| 48000H-4FFFFH | 32Kword MAIN BLOCK 13 | |
| 40000H-47FFFH | 32Kword MAIN BLOCK 12 | |
| 38000H-3FFFFH | 32Kword MAIN BLOCK 11 | |
| 30000H-37FFFH | 32Kword MAIN BLOCK 10 | |
| 28000H-2FFFFH | 32Kword MAIN BLOCK 9 | |
| 20000H-27FFFH | 32Kword MAIN BLOCK 8 | |
| 1C000H-1FFFFH | 16Kword PARAMETER BLOCK 7 | BANK(I) |
| 18000H-1BFFFH | 16Kword PARAMETER BLOCK 6 | |
| 14000H-17FFFH | 16Kword PARAMETER BLOCK 5 | |
| 10000H-13FFFH | 16Kword PARAMETER BLOCK 4 | |
| 0C000H-0FFFFH | 16Kword PARAMETER BLOCK 3 | |
| 08000H-0BFFFH | 16Kword PARAMETER BLOCK 2 | |
| 04000H-07FFFH | 16Kword PARAMETER BLOCK 1 | |
| 00000H-03FFFH | 16Kword BOOT BLOCK 0 | |

$A_{19}$-$A_0$
(M5M29GB161BWG)

**M5M29GB161BWG Memory Map**

x16 ( Wordmode)

| | | |
|---|---|---|
| FC000H-FFFFFH | 16Kword BOOT BLOCK 35 | BANK(I) |
| F8000H-FBFFFH | 16Kword PARAMETER BLOCK 34 | |
| F4000H-F7FFFH | 16Kword PARAMETER BLOCK 33 | |
| F0000H-F3FFFH | 16Kword PARAMETER BLOCK 32 | |
| EC000H-EFFFFH | 16Kword PARAMETER BLOCK 31 | |
| E8000H-EBFFFH | 16Kword PARAMETER BLOCK 30 | |
| E4000H-E7FFFH | 16Kword PARAMETER BLOCK 29 | |
| E0000H-E3FFFH | 16Kword PARAMETER BLOCK 28 | |
| D8000H-DFFFFH | 32Kword MAIN BLOCK 27 | BANK(II) |
| D0000H-D7FFFH | 32Kword MAIN BLOCK 26 | |
| C8000H-CFFFFH | 32Kword MAIN BLOCK 25 | |
| C0000H-C7FFFH | 32Kword MAIN BLOCK 24 | |
| B8000H-BFFFFH | 32Kword MAIN BLOCK 23 | |
| B0000H-B7FFFH | 32Kword MAIN BLOCK 22 | |
| A8000H-AFFFFH | 32Kword MAIN BLOCK 21 | |
| A0000H-A7FFFH | 32Kword MAIN BLOCK 20 | |
| 98000H-9FFFFH | 32Kword MAIN BLOCK 19 | |
| 90000H-97FFFH | 32Kword MAIN BLOCK 18 | |
| 88000H-8FFFFH | 32Kword MAIN BLOCK 17 | |
| 80000H-87FFFH | 32Kword MAIN BLOCK 16 | |
| 78000H-7FFFFH | 32Kword MAIN BLOCK 15 | |
| 70000H-77FFFH | 32Kword MAIN BLOCK 14 | |
| 68000H-6FFFFH | 32Kword MAIN BLOCK 13 | |
| 60000H-67FFFH | 32Kword MAIN BLOCK 12 | |
| 58000H-5FFFFH | 32Kword MAIN BLOCK 11 | |
| 50000H-57FFFH | 32Kword MAIN BLOCK 10 | |
| 48000H-4FFFFH | 32Kword MAIN BLOCK 9 | |
| 40000H-47FFFH | 32Kword MAIN BLOCK 8 | |
| 38000H-3FFFFH | 32Kword MAIN BLOCK 7 | |
| 30000H-37FFFH | 32Kword MAIN BLOCK 6 | |
| 28000H-2FFFFH | 32Kword MAIN BLOCK 5 | |
| 20000H-27FFFH | 32Kword MAIN BLOCK 4 | |
| 18000H-1FFFFH | 32Kword MAIN BLOCK 3 | |
| 10000H-17FFFH | 32Kword MAIN BLOCK 2 | |
| 08000H-0FFFFH | 32Kword MAIN BLOCK 1 | |
| 00000H-07FFFH | 32Kword MAIN BLOCK 0 | |

$A_{19}$-$A_0$
(M5M29GT161BWG)

**M5M29GT161BWG Memory Map**

## BUS OPERATIONS

### Bus Operations for Word-Wide Mode ( M5M29GB/T161BWG)

| Mode \ Pins | | CE# | OE# | WE# | RP# | $DQ_{0-15}$ |
|---|---|---|---|---|---|---|
| Read | Array | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Data out |
| | Status Register | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Status Register Data |
| | Lock Bit Status | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Lock Bit Data ($DQ_6$) |
| | Identifier Code | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | Identifier Code |
| Output disable | | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | $V_{IH}$ | Hi-Z |
| Stand by | | $V_{IH}$ | X [1)] | X | $V_{IH}$ | Hi-Z |
| Write | Program | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | Command/Data in |
| | Erase | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | Command |
| | Others | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | Command |
| Deep Power Down | | X | X | X | $V_{IL}$ | Hi-Z |

1) X can be $V_{IH}$ or $V_{IL}$ for control pins.

## SOFTWARE COMMAND DEFINITION

### Command List

| Command | 1st bus cycle | | | 2nd bus cycle | | | 3rd ~129th bus cycles (M5M29GB/T161BWG ) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Mode | Address | Data (DQ15-0)1) | Mode | Address | Data (DQ15-0) | Mode | Address | Data (DQ15-0) |
| Read Array | Write | X | FFH | | | | | | |
| Device Identifier | Write | X | 90H | Read | IA 2) | ID 2) | | | |
| Read Status Register | Write | Bank 3) | 70H | Read | Bank | SRD 4) | | | |
| Clear Status Register | Write | X | 50H | | | | | | |
| Clear Page Buffer | Write | X | 55H | Write | X | D0H 1) | | | |
| Word Program 5) | Write | Bank(I) 5) | 40H | Write | WA 6) | WD 6) | | | |
| Page Program 7) | Write | Bank | 41H | Write | WA0 7) | WD0 7) | Write | WAn 7) | WDn 7) |
| Single Data Load to Page Buffer 5) | Write | Bank(I) 5) | 74H | Write | WA | WD | | | |
| Page Buffer to Flash 5) | Write | Bank(I) 5) | 0EH | Write | WA 8) | D0H 1) | | | |
| Block Erase / Confirm | Write | Bank | 20H | Write | BA 9) | D0H 1) | | | |
| Suspend | Write | Bank | B0H | | | | | | |
| Resume | Write | Bank | D0H | | | | | | |
| Read Lock Bit Status | Write | X | 71H | Read | BA | DQ6 10) | | | |
| Lock Bit Program / Confirm | Write | Bank | 77H | Write | BA | D0H 1) | | | |
| Erase All Unlocked Blocks | Write | X | A7H | Write | X | D0H 1) | | | |

1) Upper byte data (DQ8-DQ15) is ignored.
2) IA=ID Code Address : A0=VIL (Manufacturer's Code) : A0=VIH (Device Code), ID=ID Code
3) Bank = Bank Address (Bank(I) or Bank(II)). A19-A17.
4) SRD = Status Register Data
5) Word Program, Single Data Load and Page Buffer to Flash Command is valid for only Bank(I).
6) WA = Write Address,WD = Write Data
7) WA0,WAn=Write Address, WD0,WDn=Write Data.
: Write Address and Write Data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128word (128word x 16bit).
and also A19-A7(Block Address, Page Address) must be valid.
8) WA = Write Address : Upper page address, A19-A7(Block Address, Page Address) must be valid.
9) BA = Block Address : Bank1: A19-A14
Bank2: A19-A15
10) DQ6 provides Block Lock Status, DQ6 = 1 : Block Unlock, DQ6 = 0 : Block Locked.

## BLOCK LOCKING

| 161BWG | | | Lock Bit (Internally) | Write Protection Provided | | | | Note |
|---|---|---|---|---|---|---|---|---|
| | | | | BANK(I) | | BANK(II) | Lock Bit | |
| RP# | WP1# | WP2# | | Boot | Parameter | Data | | |
| $V_{IL}$ | X | X | X | Locked | Locked | Locked | Locked | Deep Power Down Mode |
| $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | 0 | Locked | Locked | Locked | Locked | |
| | | | 1 | Locked | Unlocked | Unlocked | Locked | |
| | $V_{IH}$ | $V_{IH}$ | X | Unlocked | Unlocked | Unlocked | Unlocked | All Blocks Unlocked |
| | $V_{IL}$ | $V_{IL}$ | X | Locked | Locked | Locked | Locked | All Blocks Locked |
| | $V_{IH}$ | $V_{IL}$ | 0 | Locked | Locked | Locked | Locked | |
| | | | 1 | Locked | Unlocked | Locked | Locked | Only Parameter Block is Unlocked |

1) $DQ_6$ provides Lock Status of each block after writing the Read Lock Status command (71H).
WP1# & WP2# pins must not be switched during performing Erase / Write operations or WSM Busy (WSMS = 0).
2) Erase/Write command for locked blocks is aborted. At this time read mode is not array read mode but status read mode and 00B0 H is read. Please issue Clear Status Register command plus Read Array command to change the mode from status read mode to array read mode.

## STATUS REGISTER

| Symbol | Status | Definition | |
|---|---|---|---|
| | | "1" | "0" |
| SR.7 ($DQ_7$) | Write State Machine Status | Ready | Busy |
| SR.6 ($DQ_6$) | Suspend Status | Suspended | Operation in Progress / Completed |
| SR.5 ($DQ_5$) | Erase Status | Error | Successful |
| SR.4 ($DQ_4$) | Program Status | Error | Successful |
| SR.3 ($DQ_3$) | Block Status after Program | Error | Successful |
| SR.2 ($DQ_2$) | *Reserved* | - | - |
| SR.1 ($DQ_1$) | *Reserved* | - | - |
| SR.0 ($DQ_0$) | *Reserved* | - | - |

*DQ3 indicates the block status after the page programming, byte/word programming and page buffer to flash. When DQ3 is "1", the page has the over-programed cell . If over-program occurs, the device is block fail. However if DQ3 is "1", please try the block erase to the block. The block may revive.

## DEVICE IDENTIFIER CODE

| Code \ Pins | $A_0$ | $DQ_7$ | $DQ_6$ | $DQ_5$ | $DQ_4$ | $DQ_3$ | $DQ_2$ | $DQ_1$ | $DQ_0$ | Hex. Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer Code | $V_{IL}$ | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1CH |
| Device Code (-T161BWG) | $V_{IH}$ | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0H |
| Device Code (-B161BWG) | $V_{IH}$ | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A1H |

The upper data($D_{15-8}$) is "0".

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ voltage | With respect to Ground | -0.2 | 4.6 | V |
| $V_{I1}$ | All input or output voltage except $V_{CC}$,A9,RP# 1) | | -0.6 | 4.6 | V |
| $T_a$ | Ambient temperature | | -40 | 85 | °C |
| $T_{bs}$ | Temperature under bias | | -50 | 95 | °C |
| $T_{stg}$ | Storage temperature | | -65 | 125 | °C |
| $I_{OUT}$ | Output short circuit current | | | 100 | mA |

1) Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is $V_{CC}$+0.5V which, during transitions, may overshoot to $V_{CC}$+1.5V for periods <20ns.

## CAPACITANCE

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_{IN}$ | Input capacitance (Address, Control Pins) | Ta = 25°C, f = 1MHz, $V_{in}$ = $V_{out}$ = 0V | | | 8 | pF |
| $C_{OUT}$ | Output capacitance | | | | 12 | pF |

## DC ELECTRICAL CHARACTERISTICS (Ta = -40~ 85°C, Vcc = 2.7V ~ 3.6V, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ1) | Max | |
| $I_{LI}$ | Input leakage current | 0V≤$V_{IN}$≤$V_{CC}$ | | | | ±1.0 | µA |
| $I_{LO}$ | Output leakage current | 0V≤$V_{OUT}$≤$V_{CC}$ | | | | ±10 | µA |
| $I_{SB1}$ | $V_{CC}$ standby current | $V_{CC}$ = 3.6V, $V_{IN}$=$V_{IL}$/$V_{IH}$, CE# = RP# =WP# = $V_{IH}$ | | | 50 | 200 | µA |
| $I_{SB2}$ | | $V_{CC}$ = 3.6V, $V_{IN}$=GND or $V_{CC}$, CE# = RP# = WP# = $V_{CC}$±0.3V | | | 0.1 | 5 | µA |
| $I_{SB3}$ | $V_{CC}$ deep powerdown current | $V_{CC}$ = 3.6V, $V_{IN}$=$V_{IL}$/$V_{IH}$, RP# = $V_{IL}$ | | | 5 | 15 | µA |
| $I_{SB4}$ | | $V_{CC}$ = 3.6V, $V_{IN}$=GND or $V_{CC}$, RP# =GND±0.3V | | | 0.1 | 5 | µA |
| $I_{CC1}$ | $V_{CC}$ read current for Word or Byte | $V_{CC}$ = 3.6V, $V_{IN}$=$V_{IL}$/$V_{IH}$, CE# = $V_{IL}$, RP#=OE#=$V_{IH}$, $I_{OUT}$ = 0mA | 5MHz | | 8 | 15 | mA |
| | | | 1MHz | | 2 | 4 | |
| $I_{CC2}$ | $V_{CC}$ Write current for Word or Byte | $V_{CC}$ = 3.6V,$V_{IN}$=$V_{IL}$/$V_{IH}$, CE# =WE#= $V_{IL}$, RP#=OE#=$V_{IH}$ | | | | 15 | mA |
| $I_{CC3}$ | $V_{CC}$ program current | $V_{CC}$ = 3.6V, $V_{IN}$=$V_{IL}$/$V_{IH}$, CE# = RP# =WP# = $V_{IH}$ | | | | 35 | mA |
| $I_{CC4}$ | $V_{CC}$ erase current | $V_{CC}$ = 3.6V, $V_{IN}$=$V_{IL}$/$V_{IH}$, CE# = RP# =WP# = $V_{IH}$ | | | | 35 | mA |
| $I_{CC5}$ | $V_{CC}$ suspend current | $V_{CC}$ = 3.6V, $V_{IN}$=$V_{IL}$/$V_{IH}$, CE# = RP# =WP# = $V_{IH}$ | | | | 200 | µA |
| $V_{IL}$ | Input low voltage | | | – 0.5 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | | | 2.0 | | Vcc+0.5 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 4.0mA | | | | 0.45 | V |
| $V_{OH1}$ | Output high voltage | $I_{OH}$ = –2.0mA | | 0.85Vcc | | | V |
| $V_{OH2}$ | | $I_{OH}$ = –100µA | | Vcc–0.4 | | | V |
| $V_{LKO}$ | Low $V_{CC}$ Lock-Out voltage 2) | | | 1.5 | | 2.2 | V |

All currents are in RMS unless otherwise noted.
1) Typical values at Vcc=3.3V, Ta=25°C
2) To protect against initiation of write cycle during Vcc power-up/ down, a write cycle is locked out for Vcc less than $V_{LKO}$.
If Vcc is less than $V_{LKO}$, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Vcc is less than $V_{LKO}$, the alteration of memory contents may occur.

**AC ELECTRICAL CHARACTERISTICS** (Ta = -40 ~85°C, Vcc = 2.7V ~3.6V)

**Read-Only Mode**

| Symbol | | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Vcc=2.7-3.6V | | | |
| | | | 90ns | | | |
| | | | Min | Typ | Max | |
| $t_{RC}$ | $t_{AVAV}$ | Read cycle time | 90 | | | ns |
| $t_{a\ (AD)}$ | $t_{AVQV}$ | Address access time | | | 90 | ns |
| $t_{a\ (CE)}$ | $t_{ELQV}$ | Chip enable access time | | | 90 | ns |
| $t_{a\ (OE)}$ | $t_{GLQV}$ | Output enable access time | | | 30 | ns |
| $t_{CLZ}$ | $t_{ELQX}$ | Chip enable to output in low-Z | 0 | | | ns |
| $t_{DF(CE)}$ | $t_{EHQZ}$ | Chip enable high to output in high Z | | | 25 | ns |
| $t_{OLZ}$ | $t_{GLQX}$ | Output enable to output in low-Z | 0 | | | ns |
| $t_{DF(OE)}$ | $t_{GHQZ}$ | Output enable high to output in high Z | | | 25 | ns |
| $t_{PHZ}$ | $t_{PLQZ}$ | RP# low to output high-Z | | | 150 | ns |
| $t_{OH}$ | $t_{OH}$ | Output hold from CE#, OE#, addresses | 0 | | | ns |
| $t_{PS}$ | $t_{PHEL}$ | RP# recovery to CE# low | 150 | | | ns |

Timing measurements are made under AC waveforms for read operations.

**AC ELECTRICAL CHARACTERISTICS** (Ta = -40 ~85°C, Vcc = 2.7V ~3.6V)

**Write Mode** (WE# control)

| Symbol | | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Vcc=2.7-3.6V | | | |
| | | | 90ns | | | |
| | | | Min | Typ | Max | |
| $t_{WC}$ | $t_{AVAV}$ | Write cycle time | 90 | | | ns |
| $t_{AS}$ | $t_{AVWH}$ | Address set-up time | 50 | | | ns |
| $t_{AH}$ | $t_{WHAX}$ | Address hold time | 0 | | | ns |
| $t_{DS}$ | $t_{DVWH}$ | Data set-up time | 50 | | | ns |
| $t_{DH}$ | $t_{WHDX}$ | Data hold time | 0 | | | ns |
| $t_{OEH}$ | $t_{WHGL}$ | OE# hold from WE# high | 10 | | | ns |
| $t_{RE}$ | - | Latency between Read and Write FFH or 71H | 30 | | | ns |
| $t_{CS}$ | $t_{ELWL}$ | Chip enable set-up time | 0 | | | ns |
| $t_{CH}$ | $t_{WHEH}$ | Chip enable hold time | 0 | | | ns |
| $t_{WP}$ | $t_{WLWH}$ | Write pulse width | 60 | | | ns |
| $t_{WPH}$ | $t_{WHWL}$ | Write pulse width high | 30 | | | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | OE# hold to WE# Low | 0 | | | ns |
| $t_{BLS}$ | $t_{PHHWH}$ | Block Lock set-up to write enable high | 90 | | | ns |
| $t_{BLH}$ | $t_{QVPH}$ | Block Lockhold from valid SRD | 0 | | | ns |
| $t_{DAP}$ | $t_{WHRH1}$ | Duration of auto-program operation | | 4 | 80 | ms |
| $t_{DAE}$ | $t_{WHRH2}$ | Duration of auto-block erase operation | | 40 | 600 | ms |
| $t_{WHRL}$ | $t_{WHRL}$ | Write enable high to F-RY/BY# low | | | 90 | ns |
| $t_{PS}$ | $t_{PHWL}$ | RP# high recovery to write enable low | 150 | | | ns |

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at Vcc=3.3V, Ta=25°C

**AC ELECTRICAL CHARACTERISTICS** (Ta = -40 ~ 85°C, Vcc = 2.7V ~ 3.6V)

**Write Mode** (F-CE# control)

| Symbol | | Parameter | Limits Vcc=2.7-3.6V 90ns | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{WC}$ | $t_{AVAV}$ | Write cycle time | 90 | | | ns |
| $t_{AS}$ | $t_{AVWH}$ | Address set-up time | 50 | | | ns |
| $t_{AH}$ | $t_{EHAX}$ | Address hold time | 0 | | | ns |
| $t_{DS}$ | $t_{DVWH}$ | Data set-up time | 50 | | | ns |
| $t_{DH}$ | $t_{EHDX}$ | Data hold time | 0 | | | ns |
| $t_{OEH}$ | $t_{EHGL}$ | OE# hold from CE# high | 10 | | | ns |
| $t_{RE}$ | - | Latency between Read and Write FFH or 71H | 30 | | | ns |
| $t_{WS}$ | $t_{WLEL}$ | Write enable set-up time | 0 | | | ns |
| $t_{WH}$ | $t_{EHWH}$ | Write enable hold time | 0 | | | ns |
| $t_{CEP}$ | $t_{ELEH}$ | CE# pulse width | 60 | | | ns |
| $t_{CEPH}$ | $t_{EHEL}$ | CE# pulse width high | 30 | | | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | OE# hold to CE# Low | 90 | | | ns |
| $t_{BLS}$ | $t_{PHHEH}$ | Block Lock set-up to chip enable high | 90 | | | ns |
| $t_{BLH}$ | $t_{QVPH}$ | Block Lockhold from valid SRD | 0 | | | ns |
| $t_{DAP}$ | $t_{EHRH1}$ | Duration of auto-program operation | | 4 | 80 | ms |
| $t_{DAE}$ | $t_{EHRH2}$ | Duration of auto-block erase operation | | 40 | 600 | ms |
| $t_{EHRL}$ | $t_{EHRL}$ | CE# high to F-RY/BY# low | | | 90 | ns |
| $t_{PS}$ | $t_{PHWL}$ | RP# high recovery to write enable low | 150 | | | ns |

Read timing parameters during command write operation mode are the same as during read-only operation mode.
Typical values at Vcc=3.3V, Ta=25°C

**Erase and Program Performance**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Block Erase Time | | 40 | 600 | ms |
| Main Block Write Time (Page Mode) | | 1.0 | 1.8 | sec |
| Page Write Time | | 4 | 80 | ms |

**Program Suspend Latency / Erase Suspend Time**

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Program Suspend Latency | | | 15 | µs |
| Erase Suspend Time | | | 15 | µs |

Please see page 19.

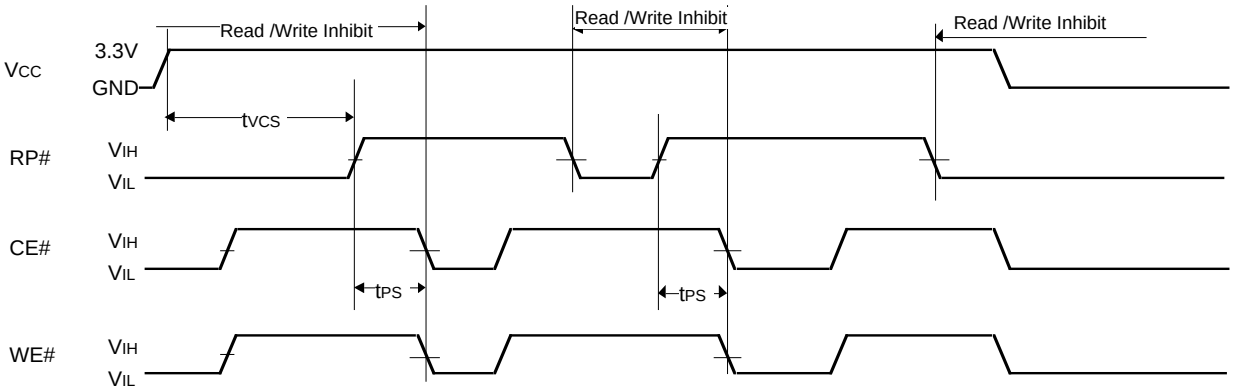
**Vcc Power Up / Down Timing**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{VCS}$ | RP# =$V_{IH}$ set-up time from Vccmin | 2 | | | µs |

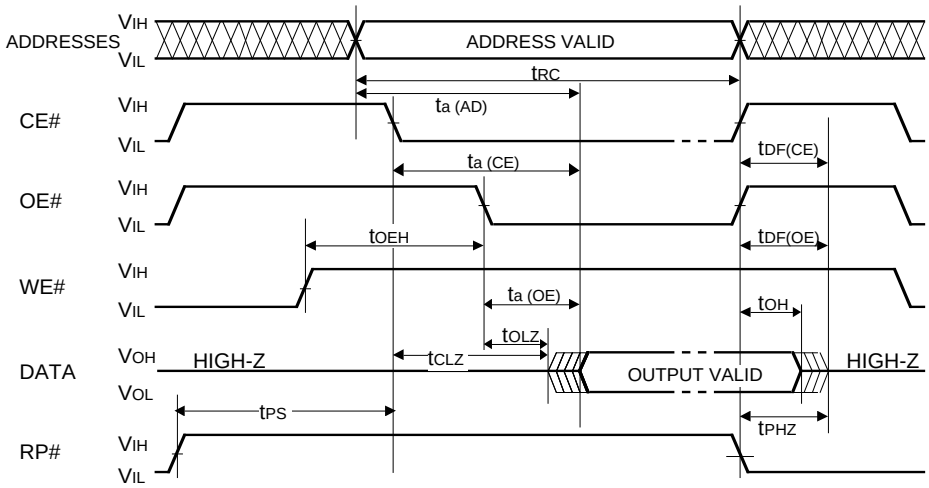
Please see page 12.

During power up/down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming.
The device must be protected against initiation of write cycle for memory contents during power up/down.
The delay time of min.2µsec is always required before read operation or write operation is initiated from the time Vcc reaches Vccmin during power up/down.
By holding RP# VIL, the contents of memory is protected during Vcc power up/down.
During power up, RP# must be held VIL for min.2µs from the time Vcc reaches Vccmin.
During power down, RP# must be held VIL until Vcc reaches GND.
RP# doesn't have latch mode ,therefore RP# must be held VIH during read operation or erase/program operation.

### Vcc POWER UP / DOWN TIMING




### AC WAVEFORMS FOR READ OPERATION AND TEST CONDITIONS

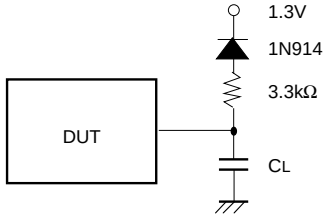



TEST CONDITIONS
FOR AC CHARACTERISTICS

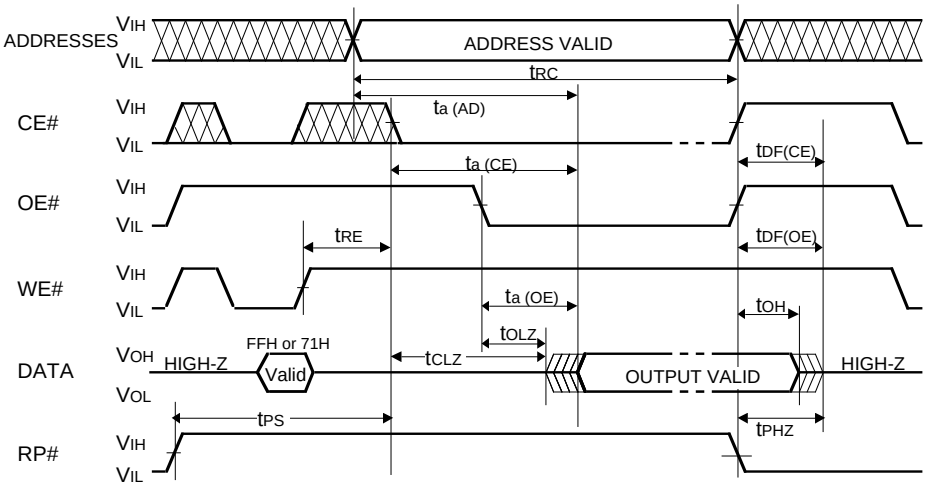
Input voltage : $V_{IL}$ = 0V, $V_{IH}$ = 3.0V
Input rise and fall times : ≤5ns
Reference voltage
at timing measurement : 1.5V

Output load : 1TTL gate +CL(30pF)

or

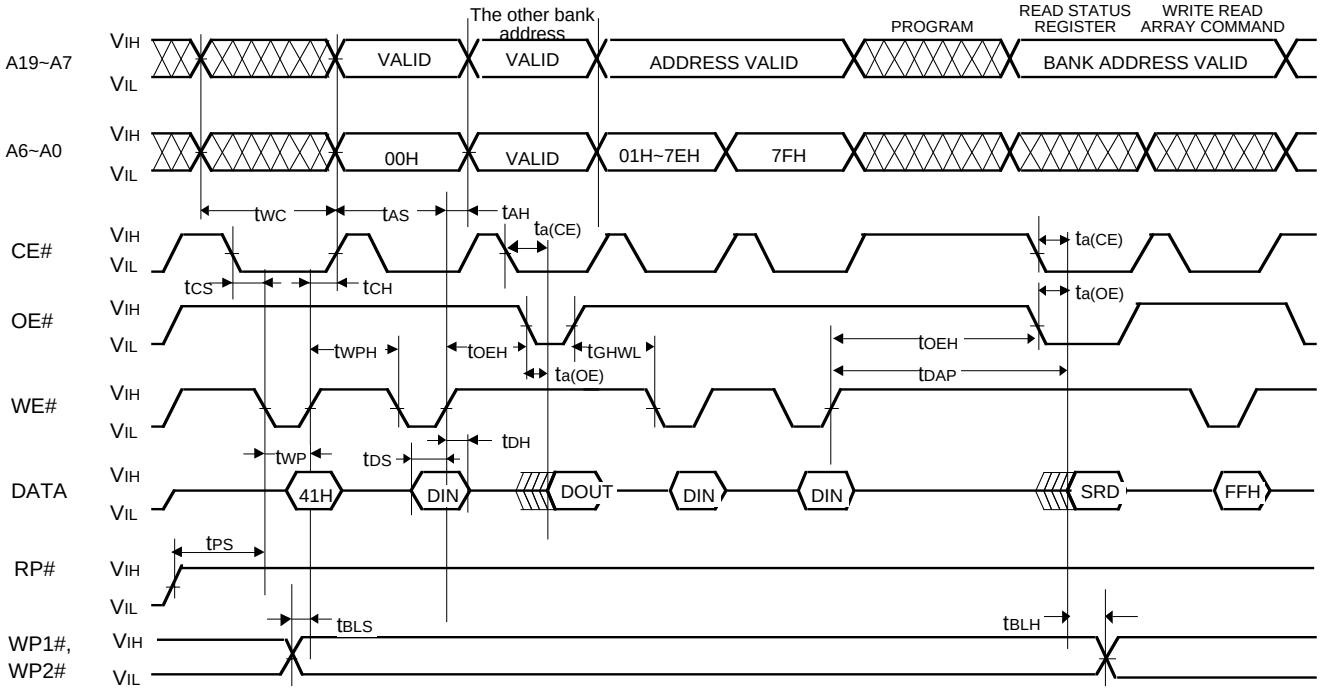



### AC WAVEFORMS FOR WRITE FFH or 71H AND READ OPERATION

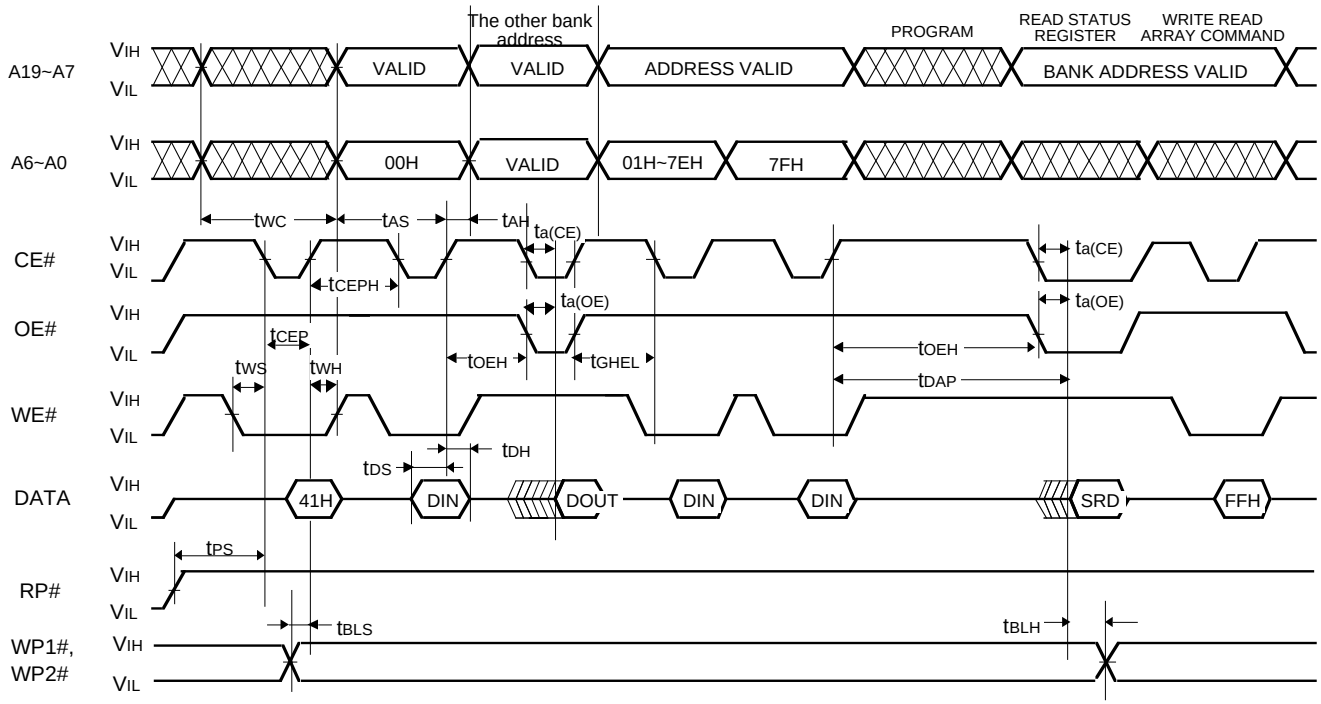



In the case of use CE# is Low fixed, it is allowed to define a timming specification of tRE from rising edge of WE# to falling edge of OE#, and valid data is read after spec of tRE+ta(CE). (This is only for FFH,71H program and read)

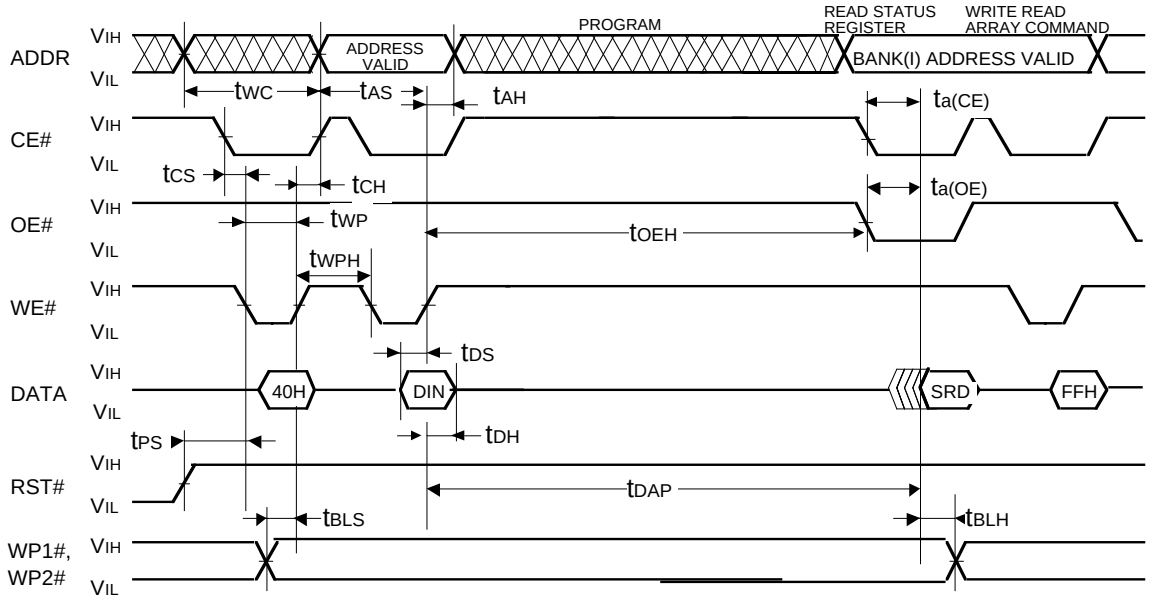
**AC WAVEFORMS FOR PAGE PROGRAM OPERATION** (WE# **control**)



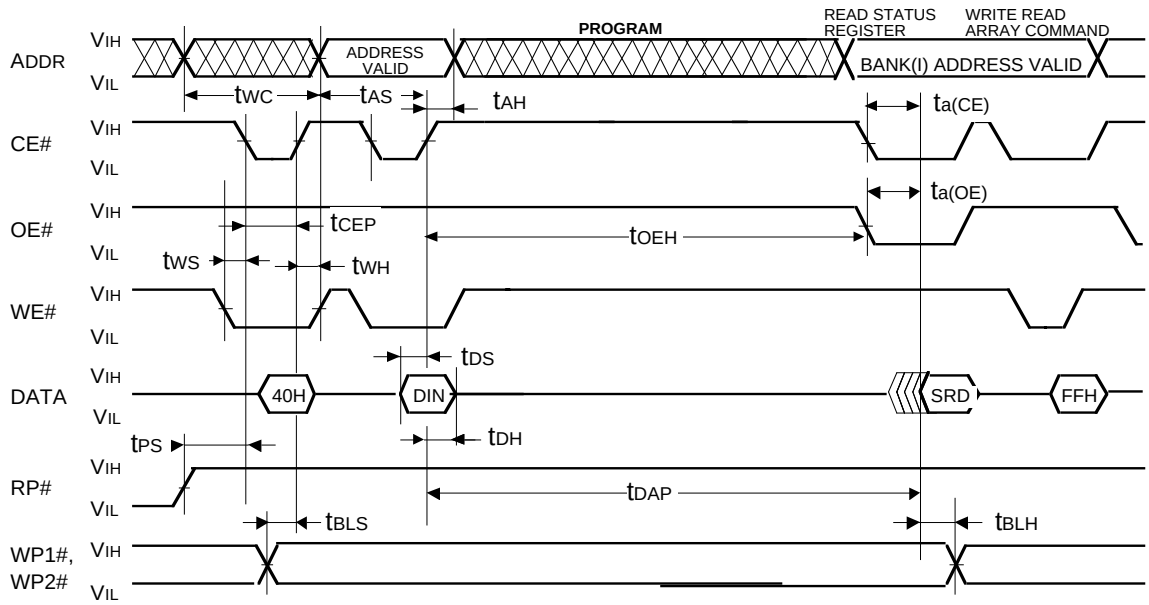

**AC WAVEFORMS FOR PAGE PROGRAM OPERATION** (CE# **control**)



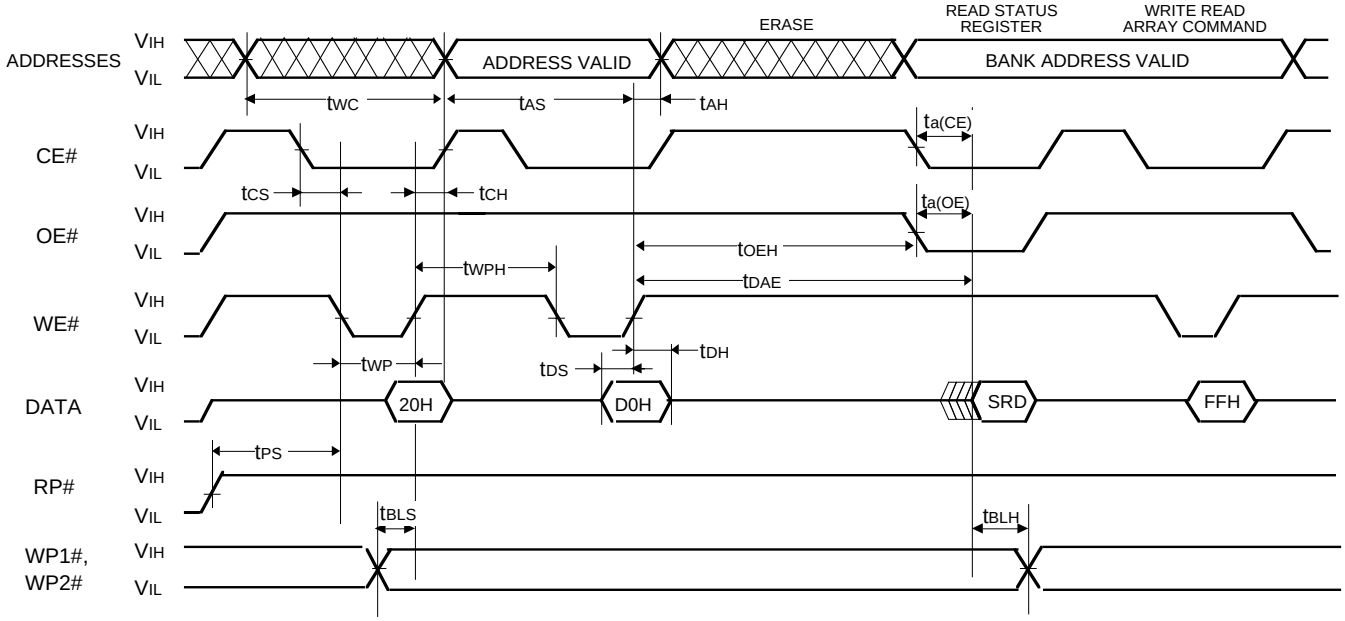
**AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION (WE# control) (to only BANK(I))**



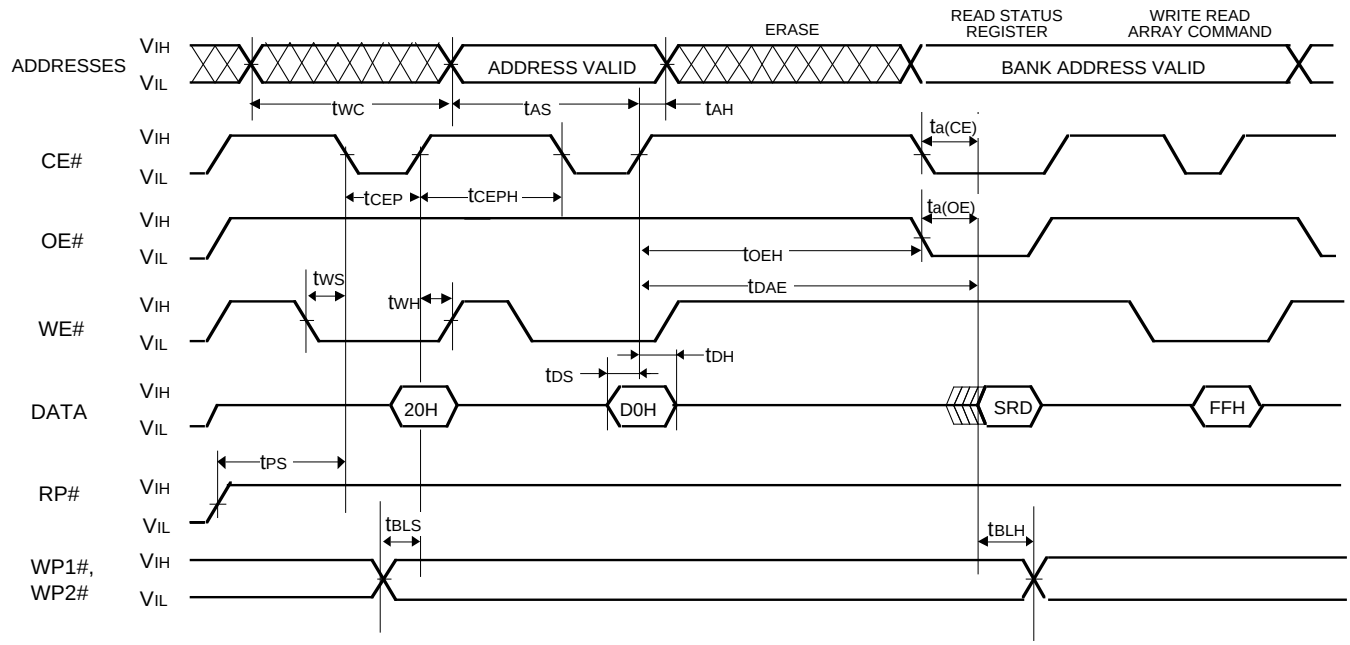

**AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION (CE# control) (to only BANK(I))**



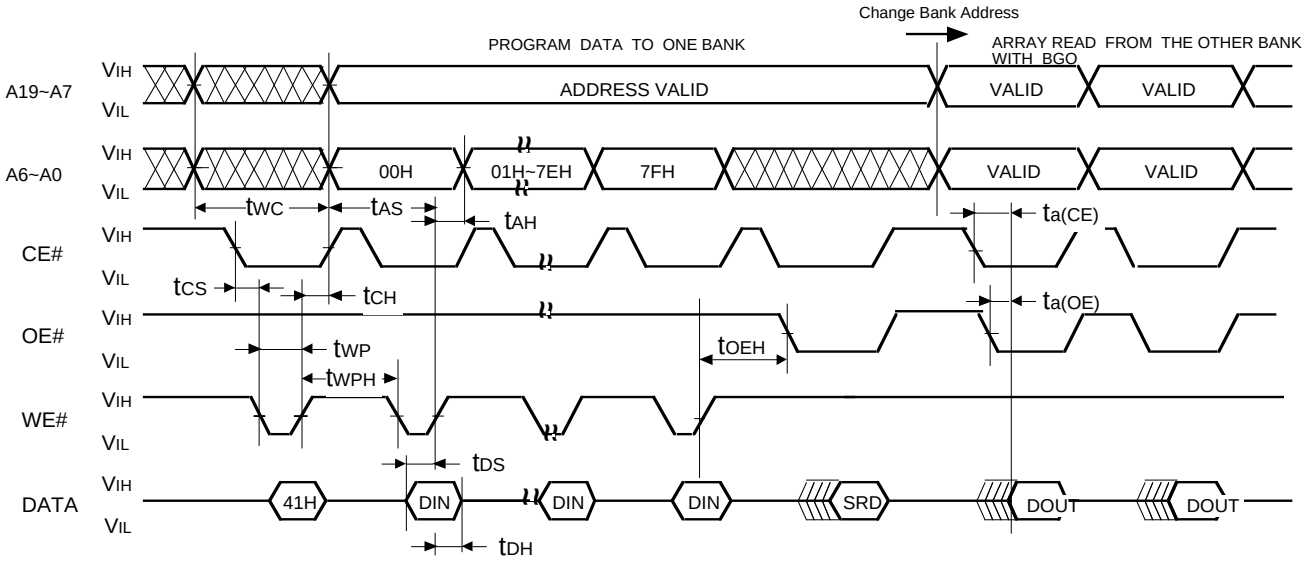
**AC WAVEFORMS FOR ERASE OPERATIONS (WE# control )**



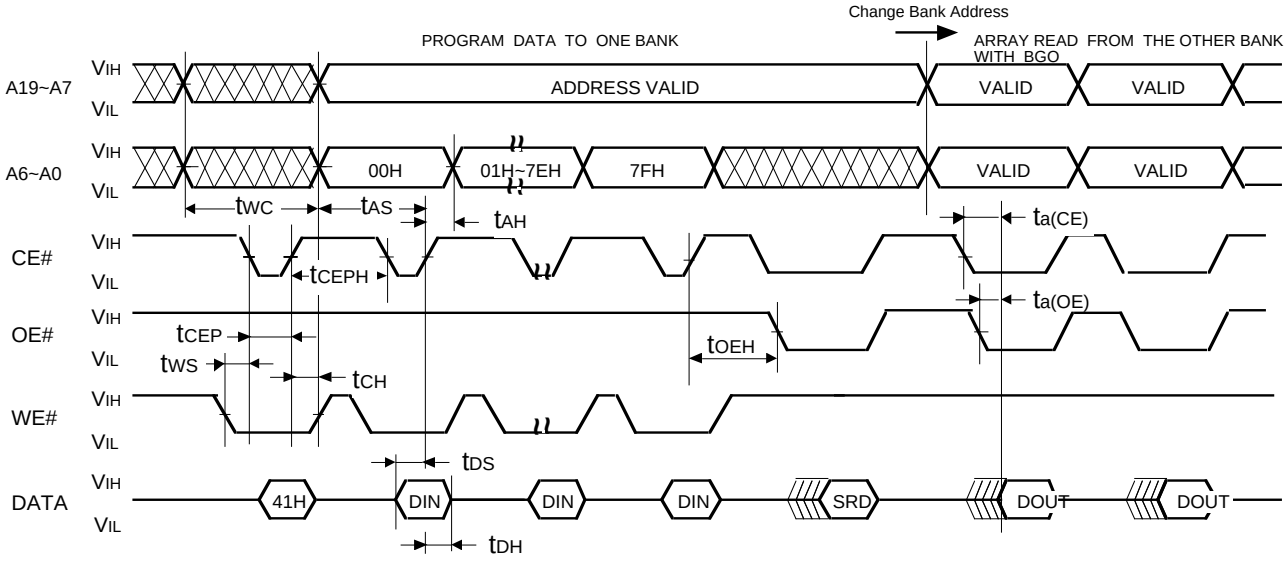

**AC WAVEFORMS FOR ERASE OPERATIONS (CE# control)**



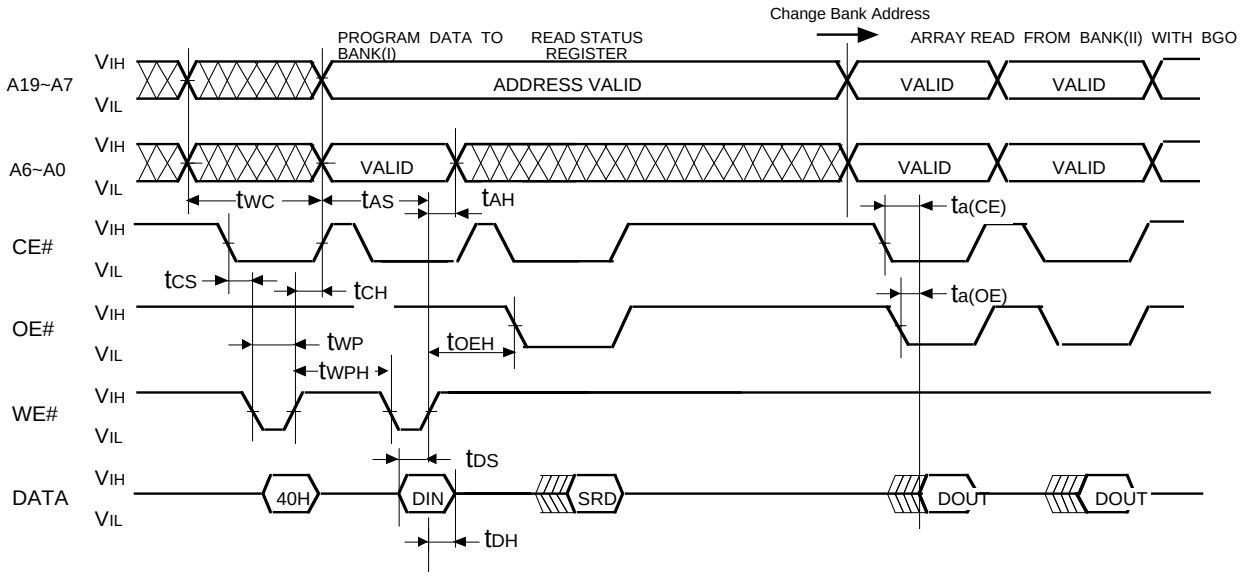
**AC WAVEFORMS FOR PAGE PROGRAM OPERATION WITH BGO (WE# control)**



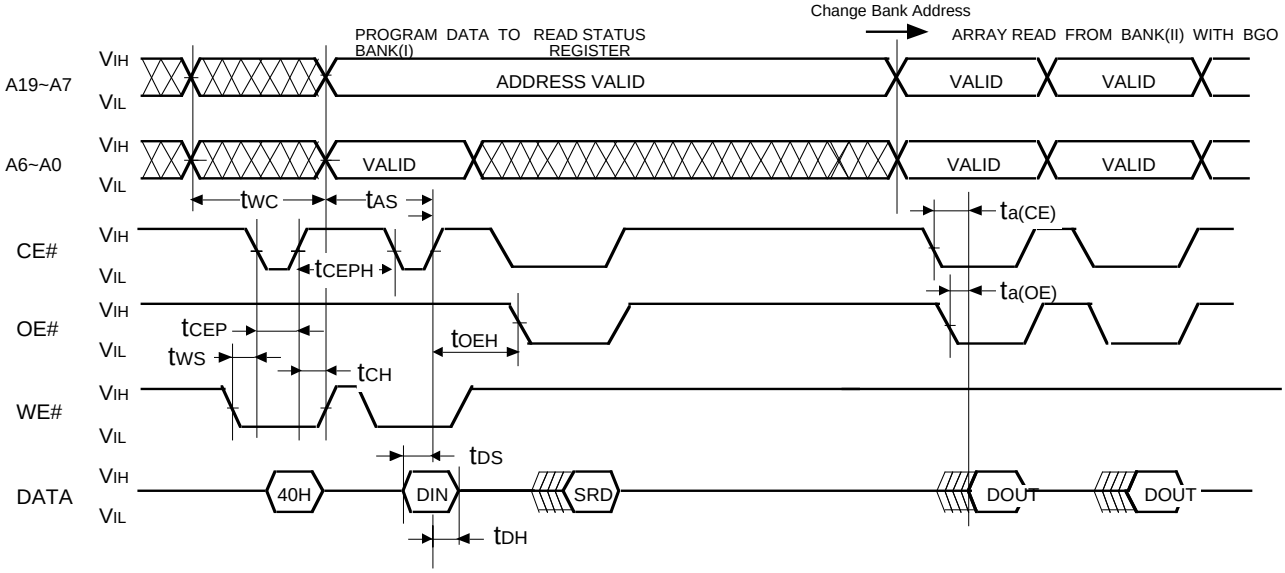

**AC WAVEFORMS FOR PAGE PROGRAM OPERATION WITH BGO (CE# control)**



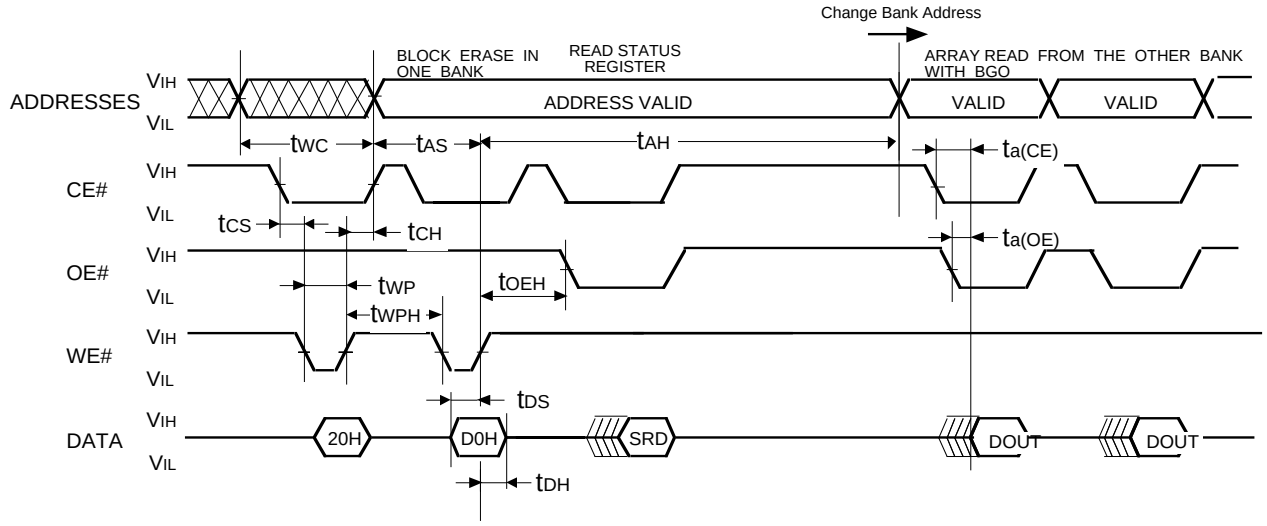
**AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION WITH BGO (WE# control)**



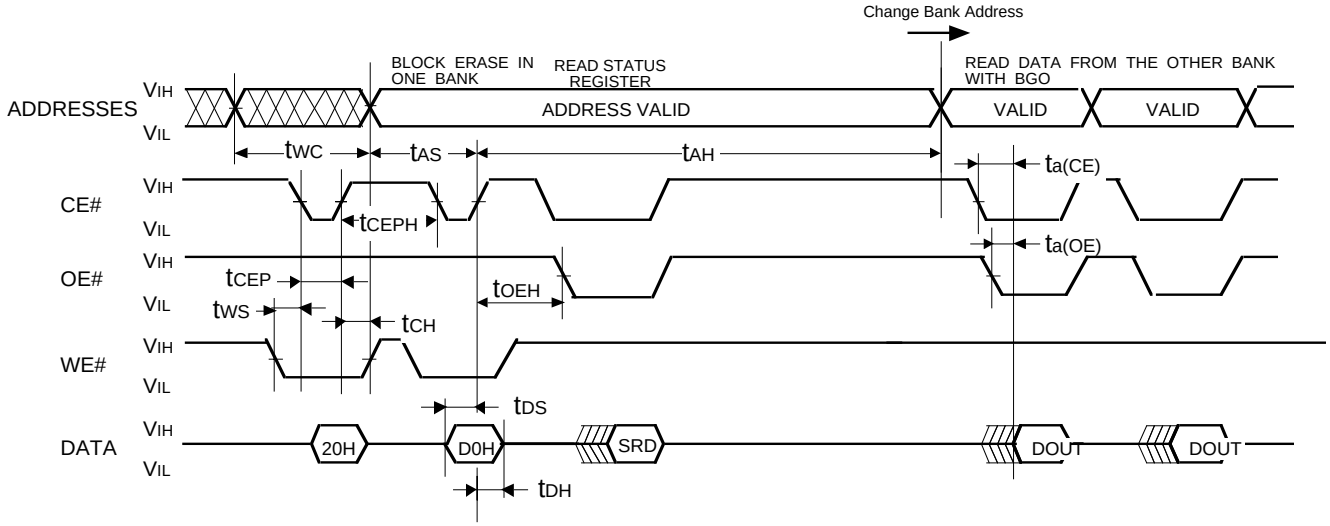

**AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION WITH BGO (CE# control)**



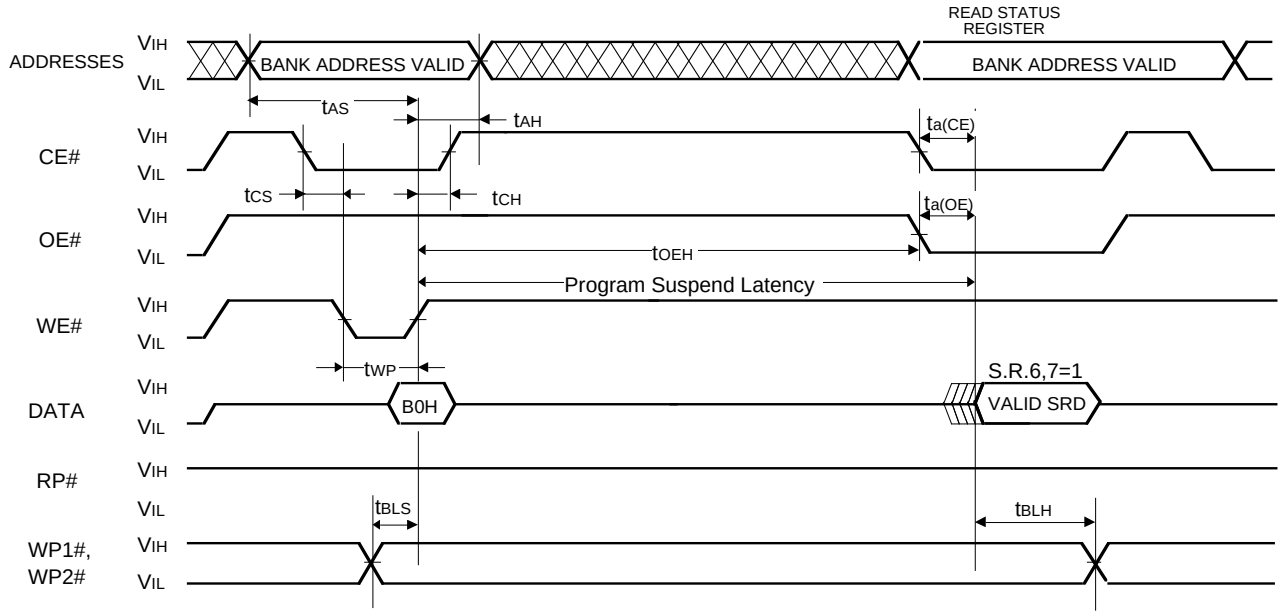
**AC WAVEFORMS FOR BLOCK ERASE OPERATION WITH BGO (WE# control)**



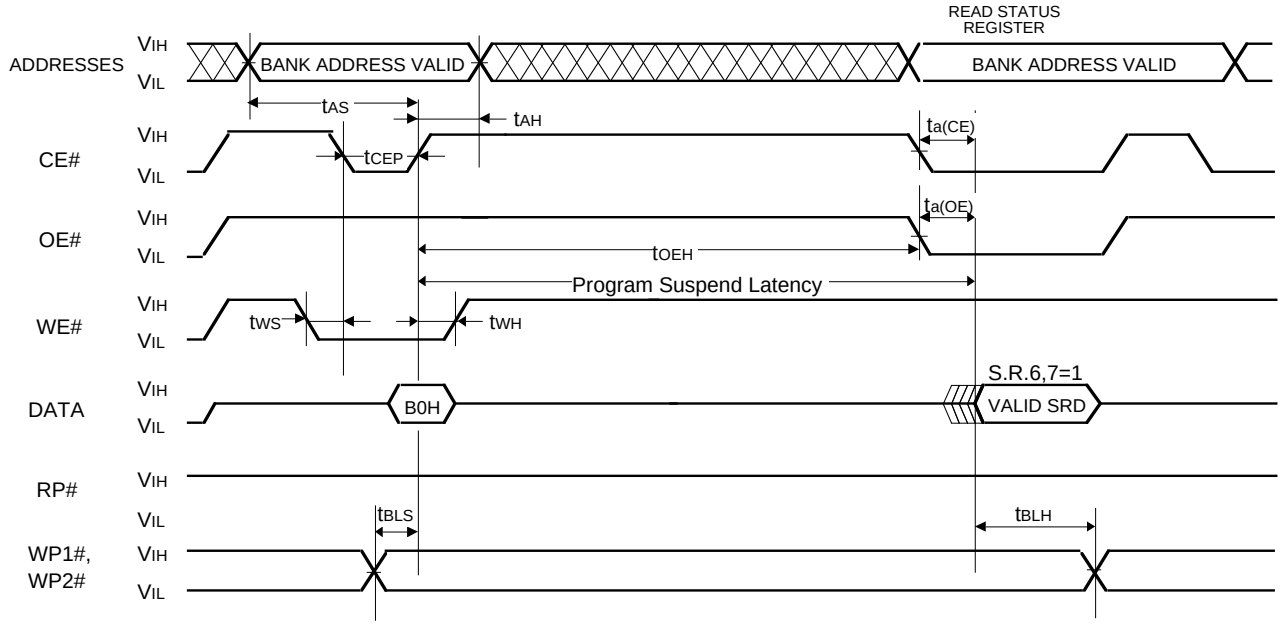

**AC WAVEFORMS FOR BLOCK ERASE OPERATION WITH BGO (CE# control)**



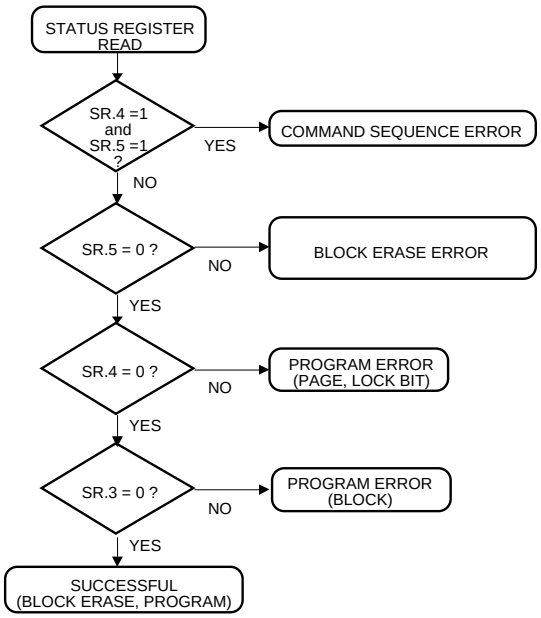
**AC WAVEFORMS FOR SUSPEND OPERATION (WE# control )**



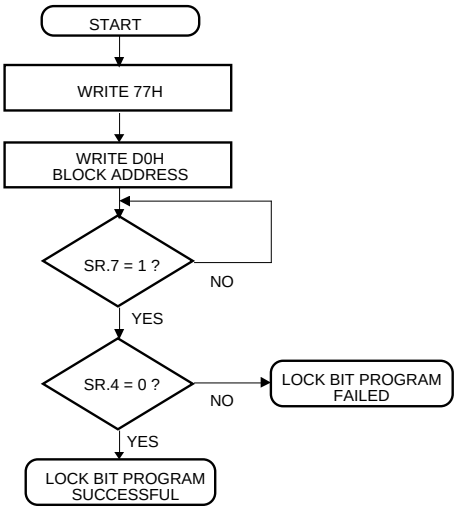

**AC WAVEFORMS FOR SUSPEND OPERATION (CE# control )**



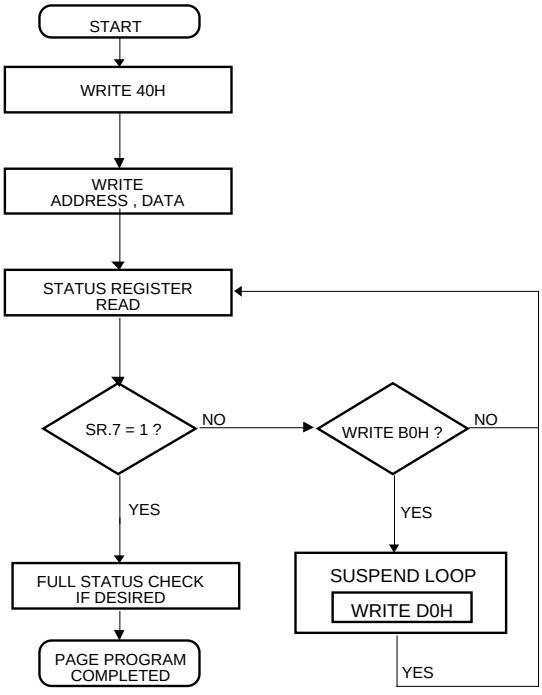
### FULL STATUS CHECK PROCEDURE




### LOCK BIT PROGRAM FLOW CHART

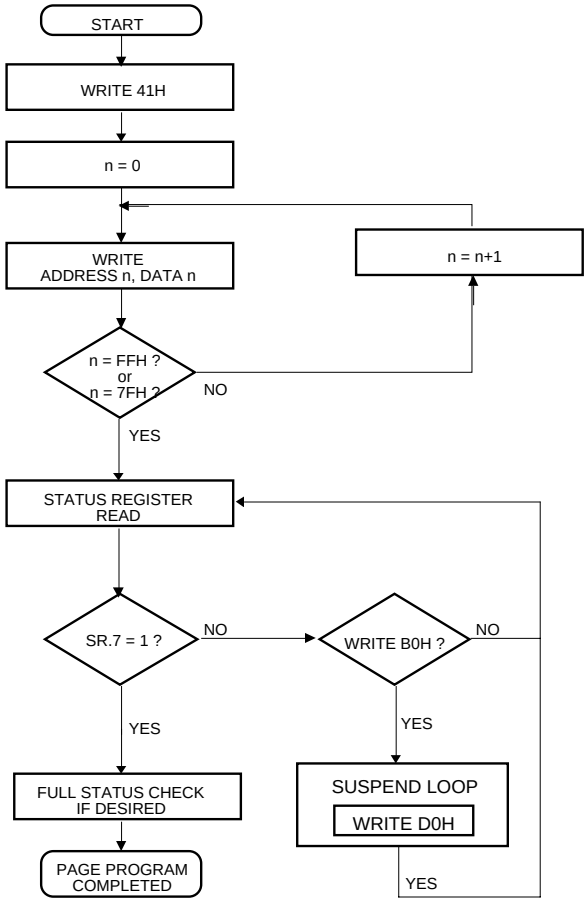



### BYTE PROGRAM FLOW CHART

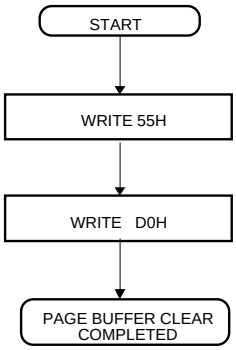



* Word program is admitted to only BANK(I).

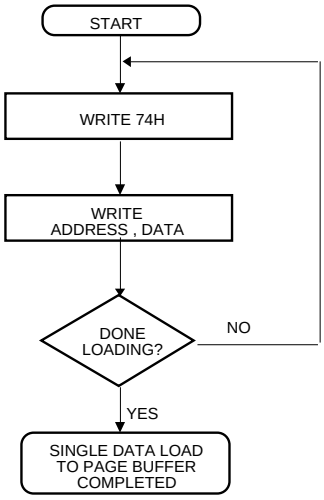
### PAGE PROGRAM FLOW CHART



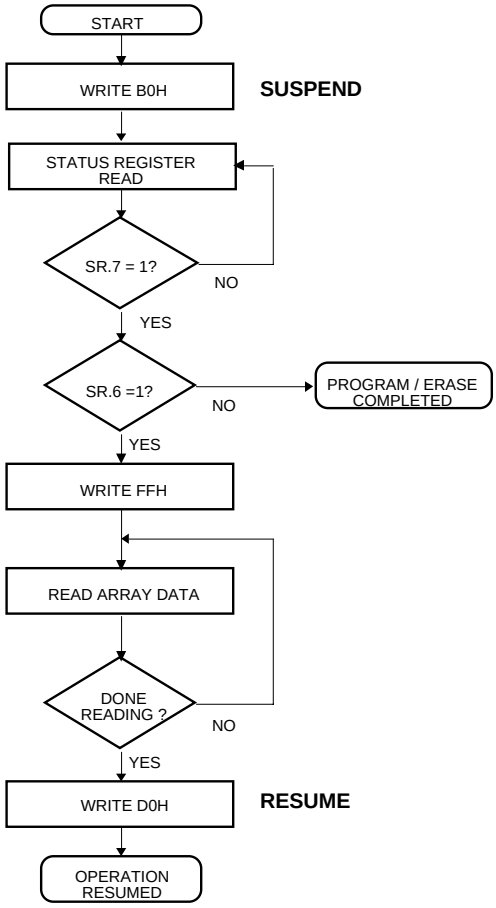
### CLEAR PAGE BUFFER




### SINGLE DATA LOAD TO PAGE BUFFER

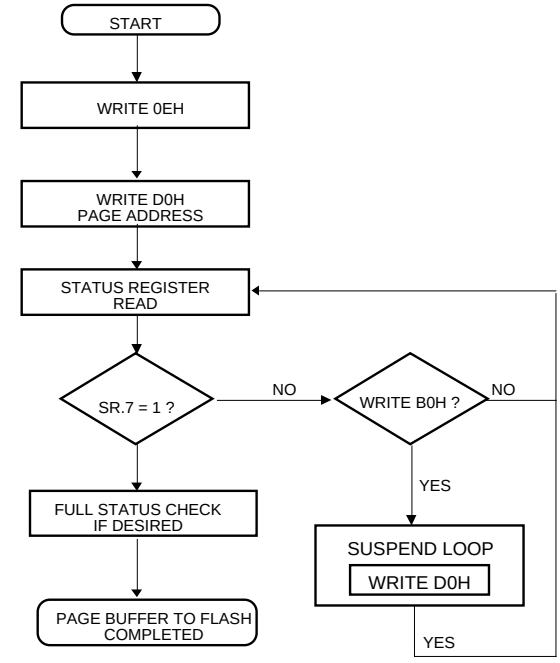



### SUSPEND / RESUME FLOW CHART

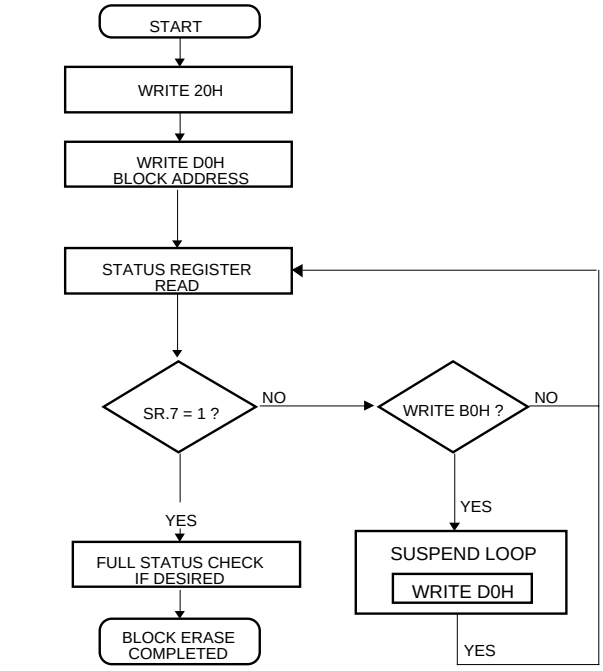



* The bank address is required when writing this command. Also, there is no need to suspend the erase or program operation when reading data from the other bank. Please use BGO function.

### PAGE BUFFER TO FLASH




### BLOCK ERASE FLOW CHART



**OPERATION STATUS and EFFECTIVE COMMAND**