

MCP (Multi-Chip Package) FLASH MEMORY & SRAM CMOS

8M (× 8/× 16) FLASH MEMORY & 2M (× 8) STATIC RAM

MB84VD2002-10/MB84VD2003-10

■ FEATURES

- Power supply voltage of 2.7 to 3.6 V
- High performance
100 ns maximum access time
- Operating Temperature
–20 to +85°C

— FLASH MEMORY

- Simultaneous operations Read-while Erase or Read-while-Program
- Minimum 100,000 write/erase cycles
- Sector erase architecture
Two 16 K byte, four 8 K bytes, two 32 K byte, and fourteen 64 K bytes.
Any combination of sectors can be concurrently erased. Also supports full chip erase.
- Boot Code Sector Architecture
MB84VD2002: Top sector
MB84VD2003: Bottom sector
- Embedded Erase™ Algorithms
Automatically pre-programs and erases the chip or any sector
- Embedded Program™ Algorithms
Automatically writes and verifies data at specified address
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion
- Ready-Busy output (RY/BY)
Hardware method for detection of program or erase cycle completion
- Automatic sleep mode
When addresses remain stable, automatically switch themselves to low power mode.
- Low V_{CC} write inhibit ≤ 2.5 V
- Erase Suspend/Resume
Suspends the erase operation to allow a read in another sector within the same device
- Please refer to "MBM29DL800TA/BA" data sheet in detailed function

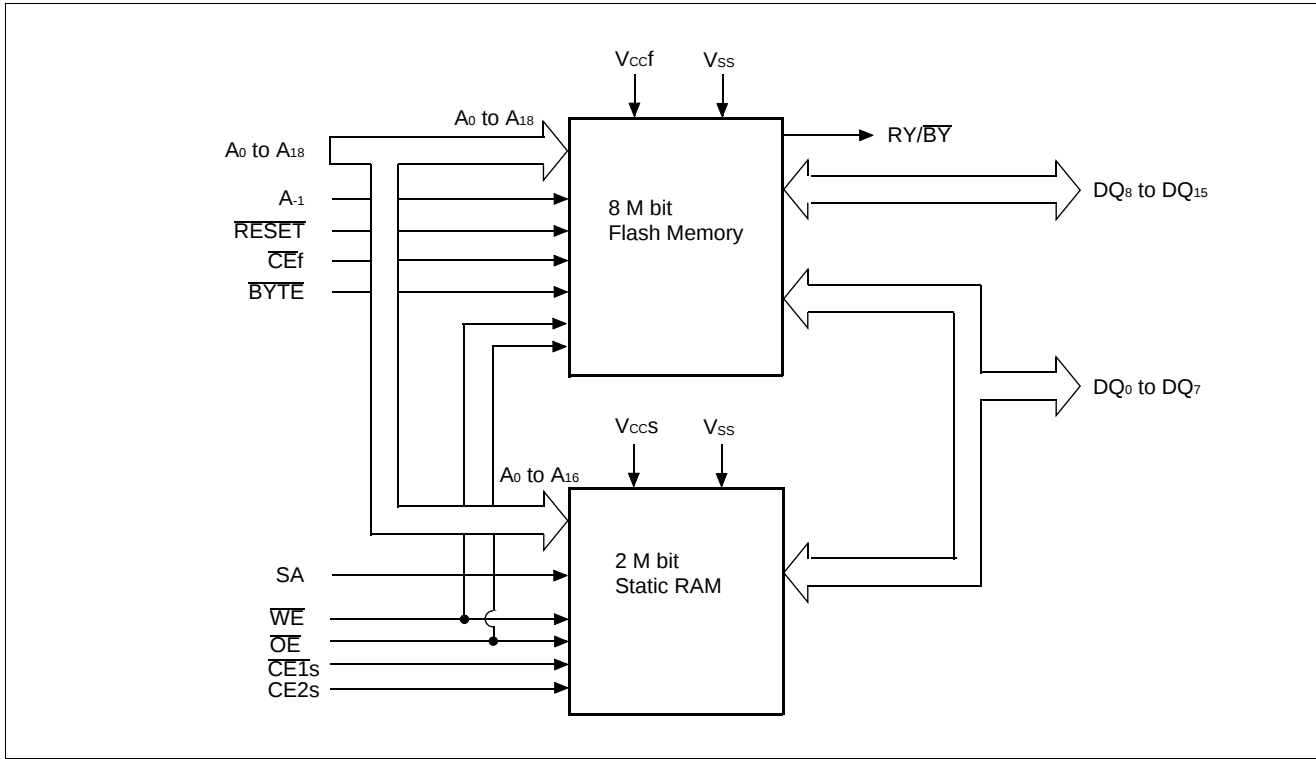
— SRAM

- Power dissipation
Operating : 35 mA max.
Standby : 50 μ A max.
- Power down features using $\overline{CE}1$ s and CE2s
- Data retention supply voltage: 2.0 V to 3.6 V

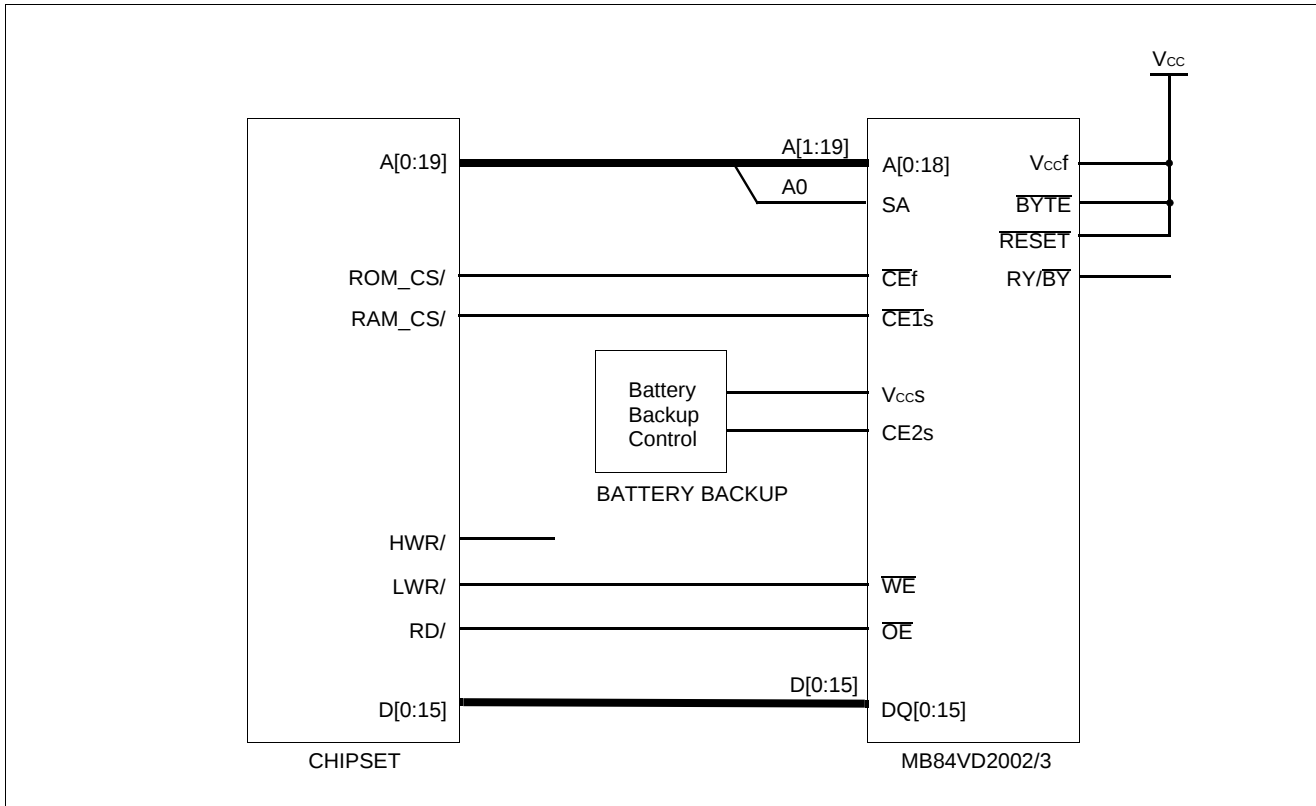
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■ BLOCK DIAGRAM



■ EXAMPLE OF CONNECTION WITH CHIPSET



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PIN ASSIGNMENTS

(Top View)

	A	B	C	D	E	F	G	H
6	$\overline{CE1s}$	V _{SS}	DQ ₁	A ₁	A ₂	A ₄	CE2s	A ₉
5	A ₁₀	DQ ₅	DQ ₂	A ₀	A ₃	A ₇	RY/ $\overline{BY}$	A ₁₄
4	$\overline{OE}$	DQ ₇	DQ ₄	DQ ₀	A ₆	A ₁₈	$\overline{RESET}$	A ₁₅
3	A ₁₁	A ₈	A ₅	DQ ₈	DQ ₃	DQ ₁₂	A ₁₂	$\overline{BYTE}$
2	A ₁₃	A ₁₇	SA*	$\overline{CEf}$	DQ ₁₀	V _{ccf}	DQ ₆	DQ ₁₅ /A ₋₁
1	$\overline{WE}$	V _{ccs}	A ₁₆	V _{SS}	DQ ₉	DQ ₁₁	DQ ₁₃	DQ ₁₄

*: A₁₇ for SRAM

Table 1 Pin Configuration

Pin	Function	Input/ Output
A ₀ to A ₁₆	Address Inputs (Common)	I
A ₋₁ , A ₁₇ to A ₁₈	Address Input (Flash)	I
SA	Address Input (SRAM)	I
DQ ₀ to DQ ₇	Data Inputs/Outputs (Common)	I/O
DQ ₈ to DQ ₁₅	Data Inputs/Outputs (Flash)	I/O
$\overline{CEf}$	Chip Enable (Flash)	I
$\overline{CE1s}$	Chip Enable (SRAM)	I
CE2s	Chip Enable (SRAM)	I
$\overline{OE}$	Output Enable (Common)	I
$\overline{WE}$	Write Enable (Common)	I
RY/ $\overline{BY}$	Ready/Busy Outputs (Flash)	O
$\overline{BYTE}$	Selects 8-bit or 16-bit mode (Flash)	I
$\overline{RESET}$	Hardware Reset Pin/Sector Protection Unlock (Flash)	I
N.C.	No Internal Connection	—
V _{SS}	Device Ground (Common)	Power
V _{ccf}	Device Power Supply (Flash)	Power
V _{ccs}	Device Power Supply (SRAM)	Power

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■ PRODUCT LINE UP

		Flash Memory	SRAM
Ordering Part No.	$V_{CC} = 3.0\text{ V}^{+0.6\text{ V}}_{-0.3\text{ V}}$	MB84VD2002-10/MB84VD2003-10	
Max. Address Access Time (ns)		100	100
Max. $\overline{CE}$ Access Time (ns)		100	100
Max. $\overline{OE}$ Access Time (ns)		40	50

■ BUS OPERATIONS

Table 2 User Bus Operations (BYTE= V_{IL})

Operation (1), (3)	$\overline{CEf}$	$\overline{CE1s}$	$CE2s$	$\overline{OE}$	$\overline{WE}$	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₅	RESET
Full Standby	H	H	X	X	X	HIGH-Z	HIGH-Z	H
		X	L					
Output Disable	X	X	X	H	H	HIGH-Z	HIGH-Z	H
Read from Flash (2)	L	H	X	L	H	D _{OUT}	HIGH-Z	H
		X	L					
Write to Flash	L	H	X	H	L	D _{IN}	HIGH-Z	H
		X	L					
Read from SRAM	H	L	H	L	H	D _{OUT}	HIGH-Z	H
Write to SRAM	H	L	H	X	L	D _{IN}	HIGH-Z	H
Flash Hardware Reset	X	H	X	X	X	HIGH-Z	HIGH-Z	L
		X	L					

Table 3 User Bus Operations (BYTE= V_{IH})

Operation (1), (3)	$\overline{CEf}$	$\overline{CE1s}$	$CE2s$	$\overline{OE}$	$\overline{WE}$	DQ ₀ to DQ ₇	DQ ₈ to DQ ₁₅	RESET
Full Standby	H	H	X	X	X	HIGH-Z	HIGH-Z	H
		X	L					
Output Disable	X	X	X	H	H	HIGH-Z	HIGH-Z	H
Read from Flash (2)	L	H	X	L	H	D _{OUT}	D _{OUT}	H
		X	L					
Write to Flash	L	H	X	H	L	D _{IN}	D _{IN}	H
		X	L					
Read from SRAM	H	L	H	L	H	D _{OUT}	HIGH-Z	H
Write to SRAM	H	L	H	X	L	D _{IN}	HIGH-Z	H
Flash Hardware Reset	X	H	X	X	X	HIGH-Z	HIGH-Z	L
		X	L					

Legend: L = V_{IL} , H = V_{IH} , X = V_{IL} or V_{IH} . See DC Characteristics for voltage levels.

- Notes:**
1. Other operations except for indicated this column are inhibited.
 2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL} , $\overline{OE}$ at V_{IH} initiates the write operations.
 4. Do not apply $\overline{CEf} = V_{IL}$, $\overline{CE1s} = V_{IL}$ and $CE2s = V_{IH}$ at a time.

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■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Two 16 K byte, four 8 K bytes, two 32 K byte, and fourteen 64 K bytes.
- Individual-sector, multiple-sector, or bulk-erase capability.

	(×8)	(×16)		(×8)	(×16)
Bank 1	16K byte/8K word	FFFFFH 7FFFFH	Bank 2	64K byte/32K word	FFFFFH 7FFFFH
	32K byte/16K word	FC000H 7E000H		64K byte/32K word	F0000H 78000H
	8K byte/4K word	F4000H 7A000H		64K byte/32K word	E0000H 70000H
	8K byte/4K word	F2000H 79000H		64K byte/32K word	D0000H 68000H
	8K byte/4K word	F0000H 78000H		64K byte/32K word	C0000H 60000H
	8K byte/4K word	EE000H 77000H		64K byte/32K word	B0000H 58000H
	8K byte/4K word	EC000H 76000H		64K byte/32K word	A0000H 50000H
	32K byte/16K word	E4000H 72000H		64K byte/32K word	90000H 48000H
	16K byte/8K word	E0000H 70000H		64K byte/32K word	80000H 40000H
	64K byte/32K word	D0000H 68000H		64K byte/32K word	70000H 38000H
Bank 2	64K byte/32K word	C0000H 60000H	Bank 1	64K byte/32K word	60000H 30000H
	64K byte/32K word	B0000H 58000H		64K byte/32K word	50000H 28000H
	64K byte/32K word	A0000H 50000H		64K byte/32K word	40000H 20000H
	64K byte/32K word	90000H 48000H		64K byte/32K word	30000H 18000H
	64K byte/32K word	80000H 40000H		64K byte/32K word	20000H 10000H
	64K byte/32K word	70000H 38000H		16K byte/8K word	1C000H 0C000H
	64K byte/32K word	60000H 30000H		32K byte/16K word	14000H 0A000H
	64K byte/32K word	50000H 28000H		8K byte/4K word	12000H 09000H
	64K byte/32K word	40000H 20000H		8K byte/4K word	10000H 08000H
	64K byte/32K word	30000H 18000H		8K byte/4K word	0E000H 07000H
	64K byte/32K word	20000H 10000H		8K byte/4K word	0C000H 06000H
	64K byte/32K word	10000H 08000H		32K byte/16K word	04000H 02000H
	64K byte/32K word	00000H 00000H		16K byte/8K word	00000H 00000H

MB84VD2002 Sector Architecture

MB84VD2003 Sector Architecture

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Table 4 Sector Address Tables (MB84DV2002)

Bank	Sector	Sector Address							Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address			A ₁₅	A ₁₄	A ₁₃	A ₁₂			
		A ₁₈	A ₁₇	A ₁₆							
Bank 2	SA0	0	0	0	0	X	X	X	64/32	00000H to 0FFFFH	00000H to 07FFFFH
	SA1	0	0	0	1	X	X	X	64/32	10000H to 1FFFFH	08000H to 0FFFFH
	SA2	0	0	1	0	X	X	X	64/32	20000H to 2FFFFH	10000H to 17FFFFH
	SA3	0	0	1	1	X	X	X	64/32	30000H to 3FFFFH	18000H to 1FFFFH
	SA4	0	1	0	0	X	X	X	64/32	40000H to 4FFFFH	20000H to 27FFFFH
	SA5	0	1	0	1	X	X	X	64/32	50000H to 5FFFFH	28000H to 2FFFFH
	SA6	0	1	1	0	X	X	X	64/32	60000H to 6FFFFH	30000H to 37FFFFH
	SA7	0	1	1	1	X	X	X	64/32	70000H to 7FFFFH	38000H to 3FFFFH
	SA8	1	0	0	0	X	X	X	64/32	80000H to 8FFFFH	40000H to 47FFFFH
	SA9	1	0	0	1	X	X	X	64/32	90000H to 9FFFFH	48000H to 4FFFFH
	SA10	1	0	1	0	X	X	X	64/32	A0000H to AFFFFH	50000H to 57FFFFH
	SA11	1	0	1	1	X	X	X	64/32	B0000H to BFFFFH	58000H to 5FFFFH
	SA12	1	1	0	0	X	X	X	64/32	C0000H to CFFFFH	60000H to 67FFFFH
	SA13	1	1	0	1	X	X	X	64/32	D0000H to DFFFFH	68000H to 6FFFFH
Bank 1	SA14	1	1	1	0	0	0	X	16/8	E0000H to E3FFFFH	70000H to 71FFFFH
	SA15	1	1	1	0	0	1	X	32/16	E4000H to E7FFFFH, E8000H to EBFFFFH	72000H to 73FFFFH, 74000H to 75FFFFH
						1	0	X			
	SA16	1	1	1	0	1	1	0	8/4	EC000H to EDFFFFH	76000H to 76FFFFH
	SA17	1	1	1	0	1	1	1	8/4	EE000H to EFFFFH	77000H to 77FFFFH
	SA18	1	1	1	1	0	0	0	8/4	F0000H to F1FFFFH	78000H to 78FFFFH
	SA19	1	1	1	1	0	0	1	8/4	F2000H to F3FFFFH	79000H to 79FFFFH
	SA20	1	1	1	1	0	1	X	32/16	F4000H to F7FFFFH, F8000H to FBFFFFH	7A000H to 7BFFFFH, 7C000H to 7DFFFFH
1						0	X				
SA21	1	1	1	1	1	1	1	X	16/8	FC000H to FFFFFFH	7E000H to 7FFFFH

Note: The address range is A₁₈: A₋₁ if in byte mode (BYTE = V_{IL}). The address range is A₁₈: A₀ if in word mode (BYTE = V_{IH}).

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Table 5 Sector Address Tables (MB84DV2003)

Bank	Sector	Sector Address							Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address			A ₁₅	A ₁₄	A ₁₃	A ₁₂			
		A ₁₈	A ₁₇	A ₁₆							
Bank 2	SA21	1	1	1	1	X	X	X	64/32	F0000H to FFFFFH	78000H to 7FFFFH
	SA20	1	1	1	0	X	X	X	64/32	E0000H to EFFFFH	70000H to 77FFFFH
	SA19	1	1	0	1	X	X	X	64/32	D0000H to DFFFFH	68000H to 6FFFFH
	SA18	1	1	0	0	X	X	X	64/32	C0000H to CFFFFH	60000H to 67FFFFH
	SA17	1	0	1	1	X	X	X	64/32	B0000H to BFFFFH	58000H to 5FFFFH
	SA16	1	0	1	0	X	X	X	64/32	A0000H to AFFFFH	50000H to 57FFFFH
	SA15	1	0	0	1	X	X	X	64/32	90000H to 9FFFFH	48000H to 4FFFFH
	SA14	1	0	0	0	X	X	X	64/32	80000H to 8FFFFH	40000H to 47FFFFH
	SA13	0	1	1	1	X	X	X	64/32	70000H to 7FFFFH	38000H to 3FFFFH
	SA12	0	1	1	0	X	X	X	64/32	60000H to 6FFFFH	30000H to 37FFFFH
	SA11	0	1	0	1	X	X	X	64/32	50000H to 5FFFFH	28000H to 2FFFFH
	SA10	0	1	0	0	X	X	X	64/32	40000H to 4FFFFH	20000H to 27FFFFH
	SA9	0	0	1	1	X	X	X	64/32	30000H to 3FFFFH	18000H to 1FFFFH
	SA8	0	0	1	0	X	X	X	64/32	20000H to 2FFFFH	10000H to 17FFFFH
Bank 1	SA7	0	0	0	1	1	1	X	16/8	1C000H to 1FFFFH	0E000H to 0FFFFH
	SA6	0	0	0	1	1	0	X	32/16	14000H to 17FFFFH, 18000H to 1BFFFFH	0A000H to 0BFFFFH, 0C000H to 0DFFFFH
						0	1	X			
	SA5	0	0	0	1	0	0	1	8/4	12000H to 13FFFFH	09000H to 09FFFFH
	SA4	0	0	0	1	0	0	0	8/4	10000H to 11FFFFH	08000H to 08FFFFH
	SA3	0	0	0	0	1	1	1	8/4	0E000H to 0FFFFH	07000H to 07FFFFH
	SA2	0	0	0	0	1	1	0	8/4	0C000H to 0DFFFFH	06000H to 06FFFFH
	SA1	0	0	0	0	1	0	X	32/16	08000H to 0BFFFFH, 04000H to 07FFFFH	04000H to 05FFFFH, 02000H to 03FFFFH
0						1	X				
SA0	0	0	0	0	0	0	0	X	16/8	00000H to 03FFFFH	00000H to 01FFFFH

Note: The address range is A₁₈: A₋₁ if in byte mode (BYTE = V_{IL}). The address range is A₁₈: A₀ if in word mode (BYTE = V_{IH}).

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Table 6. 1 Flash Memory Autoselect Codes

Type			A ₆	A ₁	A ₀	A ₋₁ *1	Code (HEX)
Manufacturer's Code			V _{IL}	V _{IL}	V _{IL}	V _{IL}	04H
Device Code	MB84VD2002	Byte	V _{IL}	V _{IL}	V _{IH}	V _{IL}	4AH
		Word				X	224AH
	MB84VD2003	Byte	V _{IL}	V _{IL}	V _{IH}	V _{IL}	CBH
		Word				X	22CBH

*1: A₋₁ is for Byte mode.

Table 6. 2 Expanded Autoselect Code Table

Type		Code	DQ ₁₅	DQ ₁₄	DQ ₁₃	DQ ₁₂	DQ ₁₁	DQ ₁₀	DQ ₉	DQ ₈	DQ ₇	DQ ₆	DQ ₅	DQ ₄	DQ ₃	DQ ₂	DQ ₁	DQ ₀
Manufacturer's Code		04H	A ₋₁ /0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MB84VD2002 (B) (W)	4AH 224AH	A ₋₁ 0	HI-Z 0	HI-Z 1	HI-Z 0	HI-Z 0	HI-Z 0	HI-Z 1	HI-Z 0	0 0	1 1	0 0	0 0	1 1	0 0	1 1	0 0
	MB84VD2003 (B) (W)	CBH 22CBH	A ₋₁ 0	HI-Z 0	HI-Z 1	HI-Z 0	HI-Z 0	HI-Z 0	HI-Z 1	HI-Z 0	1 1	1 1	0 0	0 0	1 1	0 0	1 1	1 1

(B): Byte mode

(W): Word mode

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Table 7 Flash Memory Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	Word	1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/Reset	Word	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Autoselect	Word	3	555H	AAH	2AAH	55H	(BA) 555H	90H	—	—	—	—	—	—
	Byte		AAAH		555H		(BA) AAH							
Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Erase Suspend		1	BA	B0H	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	BA	30H	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Fast Program *	Word	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXXH											
Reset from Fast Mode *	Word	2	BA	90H	XXXH	F0H	—	—	—	—	—	—	—	—
	Byte		BA		XXXH									
Extended Sector Protect	Word	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—
	Byte													

Notes: 1. Address bits A₁₁ to A₁₈ = X = "H" or "L" for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA).

2. Bus operations are defined in Tables 2 and 3.

3. RA = Address of the memory location to be read

PA = Address of the memory location to be programmed

Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of A₁₈, A₁₇, A₁₆, A₁₅, A₁₄, A₁₃, and A₁₂ will uniquely select any sector.

BA = Bank Address (A₁₆ to A₁₈)

4. RD = Data read from location RA during read operation.

PD = Data to be programmed at location PA. Data is latched on the falling edge of write pulse.

5. SPA = Sector address to be protected. Set sector address (SA) and (A₆, A₁, A₀) = (0, 1, 0).

SD = Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotected sector addresses.

* : This command is valid while Fast Mode.

MB84VD2002-10/MB84VD2003-10

■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	–25°C to +85°C
Voltage with Respect to Ground All pins (Note)	–0.3 V to $V_{ccf} + 0.5$ V
	–0.3 V to $V_{ccs} + 0.5$ V
V_{ccf}/V_{ccs} Supply (Note)	–0.3 V to +4.6 V

Note: Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negativeovershoot V_{ss} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are $V_{ccf} + 0.5$ V or $V_{ccs} + 0.5$ V. During voltage transitions, outputs may positive overshoot to $V_{cc} + 2.0$ V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Commercial Devices

Ambient Temperature (T_A)–20°C to +85°C

V_{ccf}/V_{ccs} Supply Voltages.....+2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

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■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Unit
I _{LI}	Input Leakage Current	—			−1.0	—	+1.0	μA
I _{LO}	Output Leakage Current	—			−1.0	—	+1.0	μA
I _{CC1f}	Flash V _{CC} Active Current (Read)	V _{CCf} = V _{CC} Max., CE _f = V _{IL} OE = V _{IH}	Byte	t _{CYCLE} = 10 MHz	—	—	18	mA
			Word		—	—	20	
			Byte	t _{CYCLE} = 5 MHz	—	—	8	
			Word		—	—	10	
I _{CC2f}	Flash V _{CC} Active Current (Program/Erase)	V _{CCf} = V _{CC} Max., CE _f = V _{IL} , OE = V _{IH}			—	—	35	mA
I _{CC3f***}	Flash V _{CC} Active Current (Read-While-Program)	CE = V _{IL} , OE = V _{IH}		Byte	—	—	45	mA
				Word	—	—	45	
I _{CC4f***}	Flash V _{CC} Active Current (Read-While-Erase)	CE = V _{IL} , OE = V _{IH}		Byte	—	—	45	mA
				Word	—	—	45	
I _{CC5f}	Flash V _{CC} Active Current (Erase-Suspend-Program)	CE = V _{IL} , OE = V _{IH}			—	—	35	mA
I _{CC1S}	SRAM V _{CC} Active Current	V _{CCS} = V _{CC} Max., CE1s = V _{IL} , CE2s = V _{IH}		t _{CYCLE} =10 MHz	—	—	40	mA
				t _{CYCLE} = 1 MHz	—	—	12	mA
I _{CC2S}	SRAM V _{CC} Active Current	CE1s = 0.2 V, CE2s = V _{CCS} − 0.2 V, WE = V _{CCS} − 0.2 V		t _{CYCLE} = 10 MHz	—	—	35	mA
				t _{CYCLE} = 1 MHz	—	—	6	mA
I _{SB1f}	Flash V _{CC} Standby Current	V _{CCf} = V _{CC} Max., CE _f = V _{CCf} ± 0.3 V RESET = V _{CCf} ± 0.3 V			—	—	5	μA
I _{SB2f}	Flash V _{CC} Standby Current (RESET)	V _{CCf} = V _{CC} Max., RESET = V _{SS} ± 0.3 V			—	—	5	μA
I _{SB1S}	SRAM V _{CC} Standby Current	CE1s = V _{IH} or CE2s = V _{IL}			—	—	2	mA
I _{SB2S**}	SRAM V _{CC} Standby Current	CE1s = V _{CC} −0.2 V or CE2s = 0.2 V	V _{CCS} = 3.0 V ±10%	T _A = 25°C	—	1	2.5	μA
				T _A = −20 to +85°C	—	—	55	μA
			V _{CCS} = 3.3 V ±0.3 V	T _A = 25°C	—	1.5	3	μA
				T _A = −20 to +85°C	—	—	60	μA
			V _{CCS} = 3.0 V	T _A = 25°C	—	1	2	μA
				T _A = −20 to +40°C	—	—	5	μA
				T _A = −20 to +85°C	—	—	50	μA
			V _{IL}	Input Low Level	—			−0.3
V _{IH}	Input High Level	—			2.2	—	V _{CC} +0.3*	V
V _{OL}	Output Low Voltage Level	I _{OL} = 2.1 mA, V _{CCf} = V _{CCS} = V _{CC} Min.			—	—	0.4	V
V _{OH}	Output High Voltage Level	I _{OH} = −500 μA, V _{CCf} = V _{CCS} = V _{CC} Min.			V _{CC} − 0.5	—	—	V
V _{LKO}	Flash Low V _{CC} Lock-Out Voltage	—			2.3	—	2.5	V

* : V_{CC} indicate lower of V_{CCf} or V_{CCS} ** : During standby mode with $\overline{CE}1s = V_{CCS} - 0.2 \text{ V}$, $\overline{CE}2s$ should be $\overline{CE}2s < 0.2 \text{ V}$ or $\overline{CE}2s > V_{CCS} - 0.2 \text{ V}$

*** : Embedded Algorithm (program or erase) is in progress. (@5 MHz)

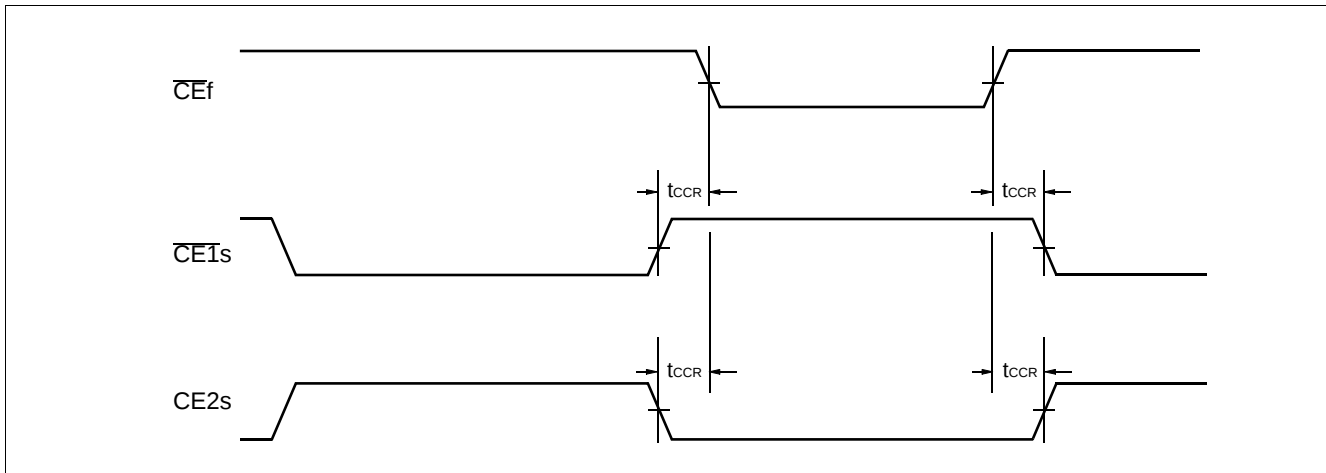
MB84VD2002-10/MB84VD2003-10

■ AC CHARACTERISTICS

• $\overline{\text{CE}}$ Timing

Parameter Symbols		Description	Test Setup		-10	Unit
JEDEC	Standard					
—	t_{CCR}	$\overline{\text{CE}}$ Recover Time	—	Min.	0	ns

• Timing Diagram for alternating SRAM to Flash



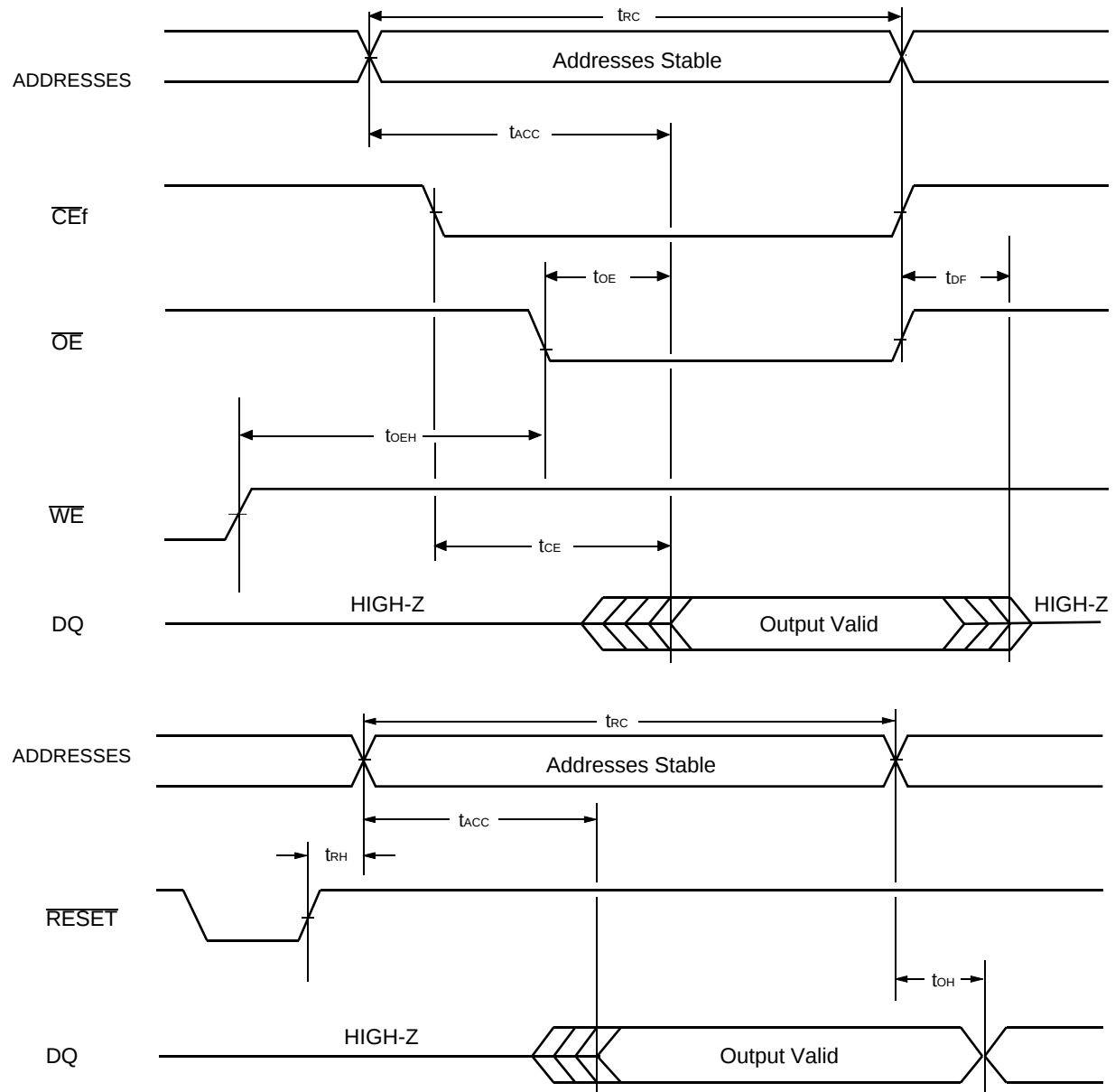
• Read Only Operations Characteristics (Flash)

Parameter Symbols		Description	Test Setup	-10 (Note)		Unit
JEDEC	Standard			Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	—	100	—	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{\text{CE}}_f = V_{\text{IL}}$ $\overline{\text{OE}} = V_{\text{IL}}$	—	100	ns
t_{ELQV}	t_{CEf}	Chip Enable to Output Delay	$\overline{\text{OE}} = V_{\text{IL}}$	—	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	—	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	—	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	—	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{\text{CE}}_f$ or $\overline{\text{OE}}$, Whichever Occurs First	—	0	—	ns
—	t_{READY}	$\overline{\text{RESET}}$ Pin Low to Read Mode	—	—	20	μs
—	t_{ELFL} t_{ELFH}	$\overline{\text{CE}}$ or $\overline{\text{BYTE}}$ Switching Low or High	—	—	5	ns

Note: Test Conditions—Output Load: 1 TTL gate and 30 pF
 Input rise and fall times: 5 ns
 Input pulse levels: 0.0 V to 3.0 V
 Timing measurement reference level
 Input: 1.5 V
 Output: 1.5 V

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• Read Cycle (Flash)



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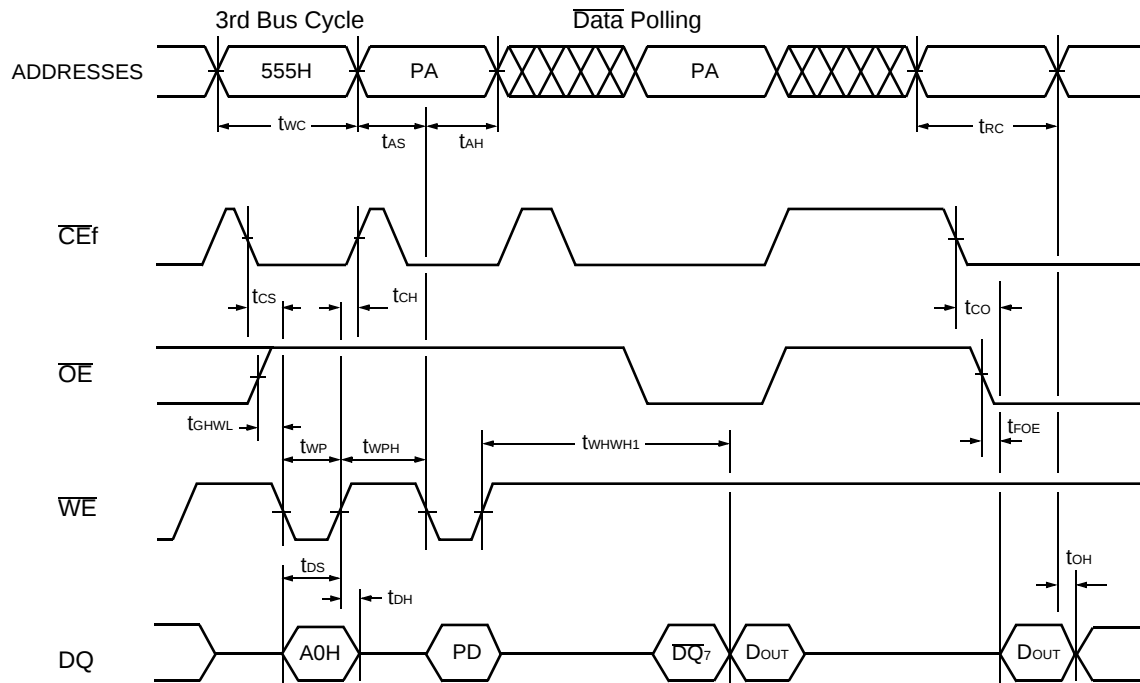
• Erase/Program Operations (Flash)

Parameter Symbols		Description	-10			Unit
JEDEC	Standard		Min.	Typ.	Max.	
t _{AVAV}	t _{WC}	Write Cycle Time	100	—	—	ns
t _{AVWL}	t _{AS}	Address Setup Time ($\overline{WE}$ to Addr.)	0	—	—	ns
t _{AVEL}	t _{AS}	Address Setup Time ($\overline{CEf}$ to Addr.)	0	—	—	ns
—	t _{ASO}	Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling	15	—	—	ns
t _{WLAX}	t _{AH}	Address Hold Time ($\overline{WE}$ to Addr.)	50	—	—	ns
t _{ELAX}	t _{AH}	Address Hold Time ($\overline{CEf}$ to Addr.)	50	—	—	ns
—	t _{AHT}	Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling	0	—	—	ns
t _{DVWH}	t _{DS}	Data Setup Time	50	—	—	ns
t _{WDHX}	t _{DH}	Data Hold Time	0	—	—	ns
—	t _{OEH}	Output Enable Hold Time Read	0	—	—	ns
		Toggle and Data Polling	10	—	—	ns
—	t _{CEPH}	$\overline{CE}$ High During Toggle Bit Polling	20	—	—	ns
—	t _{OEPH}	$\overline{OE}$ High During Toggle Bit Polling	20	—	—	ns
t _{GHEL}	t _{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CEf}$)	0	—	—	ns
t _{GHWL}	t _{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)	0	—	—	ns
t _{WLEL}	t _{WS}	$\overline{WE}$ Setup Time ($\overline{CEf}$ to $\overline{WE}$)	0	—	—	ns
t _{ELWL}	t _{CS}	$\overline{CEf}$ Setup Time ($\overline{WE}$ to $\overline{CEf}$)	0	—	—	ns
t _{EHWH}	t _{WH}	$\overline{WE}$ Hold Time ($\overline{CEf}$ to $\overline{WE}$)	0	—	—	ns
t _{WHEH}	t _{CH}	$\overline{CEf}$ Hold Time ($\overline{WE}$ to $\overline{CEf}$)	0	—	—	ns
t _{WLWH}	t _{WP}	Write Pulse Width	50	—	—	ns
t _{ELEH}	t _{CP}	$\overline{CEf}$ Pulse Width	50	—	—	ns
t _{WHWL}	t _{WPH}	Write Pulse Width High	30	—	—	ns
t _{EHEL}	t _{CPH}	$\overline{CEf}$ Pulse Width High	30	—	—	ns
t _{WHWH1}	t _{WHWH1}	Byte Programming Operation	—	8	—	μs
t _{WHWH2}	t _{WHWH2}	Sector Erase Operation (Note 1)	—	1	—	sec
			—	—	15	sec
—	t _{VCS}	V _{ccf} Setup Time	50	—	—	μs
—	t _{VLHT}	Voltage Transition Time (Note 2)	4	—	—	μs
—	t _{IDR}	Rise Time to V _{ID} (Note 2)	500	—	—	ns
—	t _{RB}	Recover Time from RY/ $\overline{BY}$	0	—	—	ns
—	t _{RP}	RESET Pulse Width	500	—	—	ns
—	t _{RH}	RESET Hold Time Before Read	200	—	—	ns
—	t _{EOE}	Delay Time from Embedded Output Enable	—	—	100	ns
—	t _{BUSY}	Program/Erase Valid to RY/ $\overline{BY}$ Delay	—	—	90	ns
—	t _{FLQZ}	BYTE Switching Low to Output High-Z	—	—	30	ns
—	t _{FHQV}	BYTE Switching High to Output Active	30	—	—	ns

Note : 1. This does not include the preprogramming time.

2. This timing is for Sector Protection Operation.

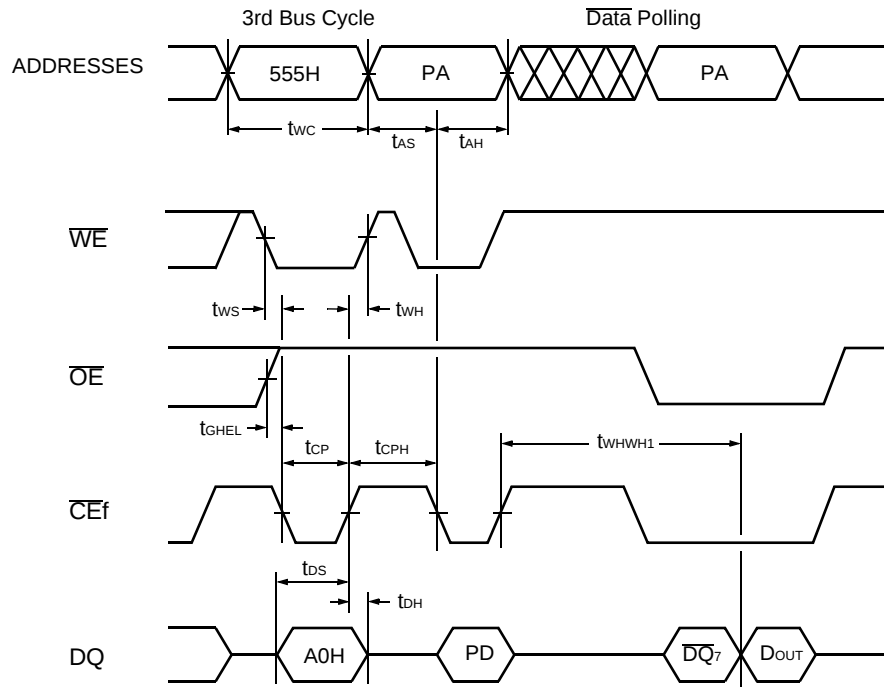
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• Write Cycle ($\overline{WE}$ control) (Flash)

- Notes:**
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
 4. D_{OUT} is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence
 6. These waveforms are for the x16 mode. The addresses differ from x8 mode.

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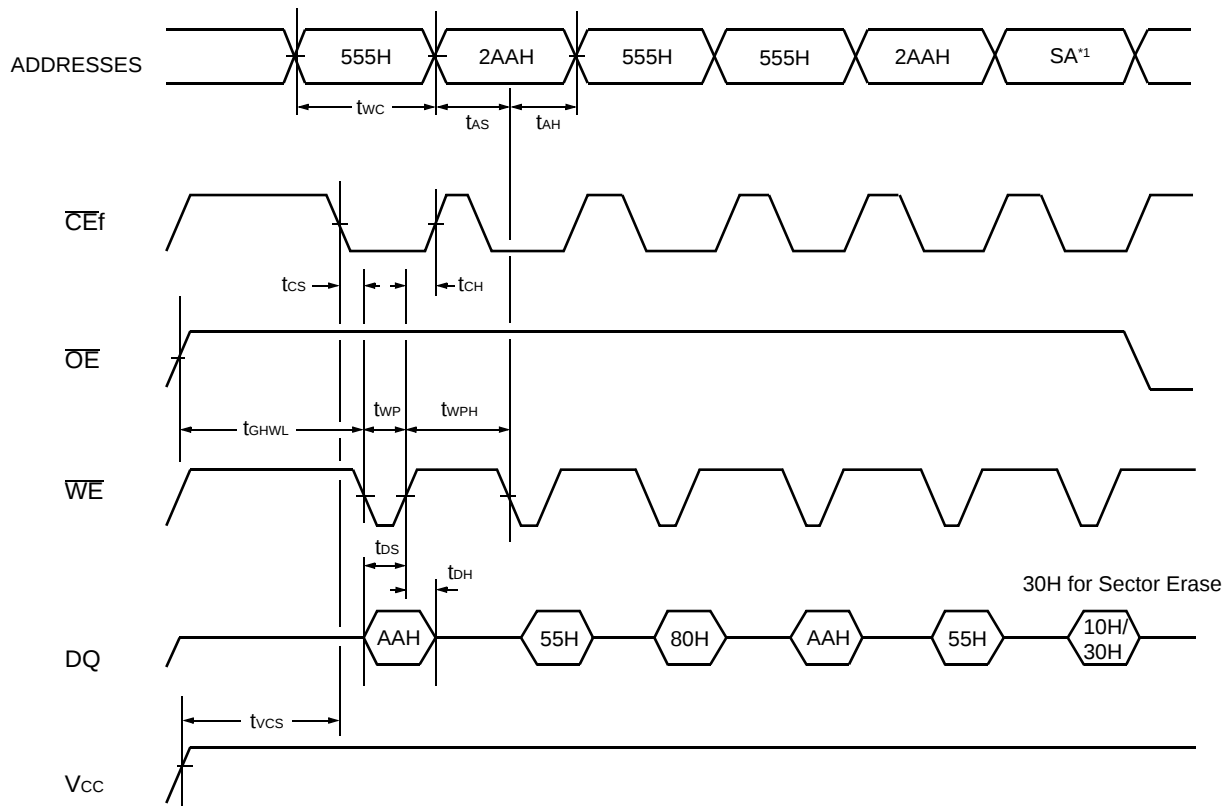
• Write Cycle ($\overline{\text{CEf}}$ control) (Flash)



- Notes:**
1. PA is address of the memory location to be programmed.
 2. PD is data to be programmed at byte address.
 3. $\overline{\text{DQ}}_7$ is the output of the complement of the data written to the device.
 4. DOUT is the output of the data written to the device.
 5. Figure indicates last two bus cycles out of four bus cycle sequence
 6. These waveforms are for the x16 mode. The addresses differ from x8 mode.

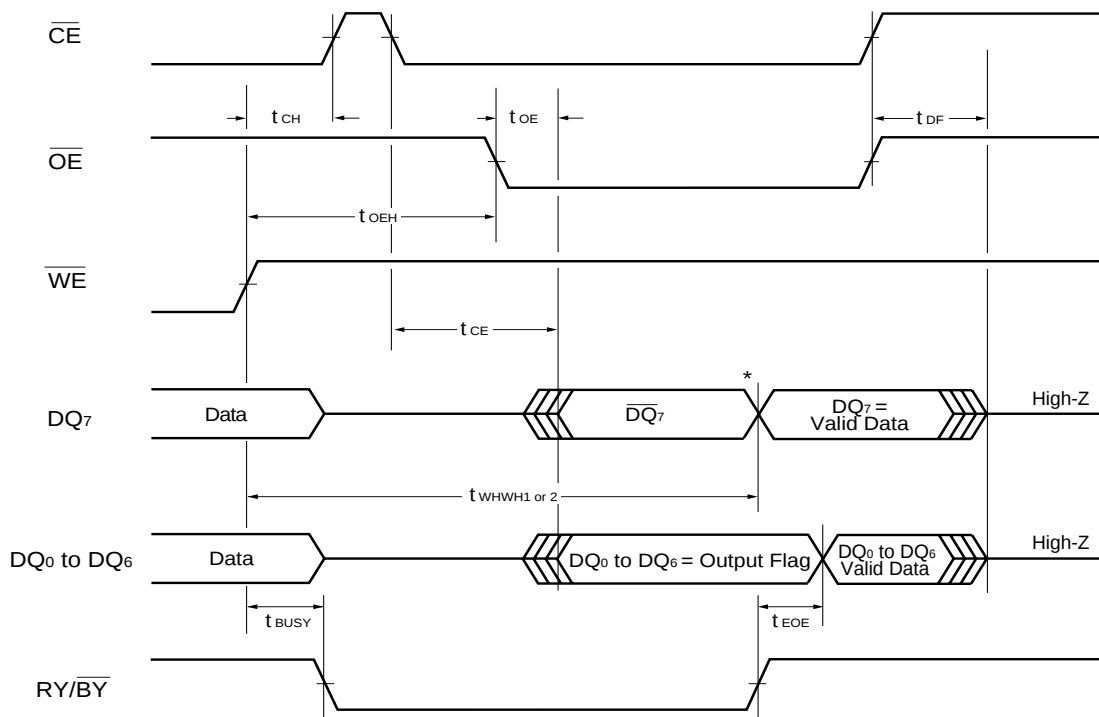
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• AC Waveforms Chip/Sector Erase Operations (Flash)



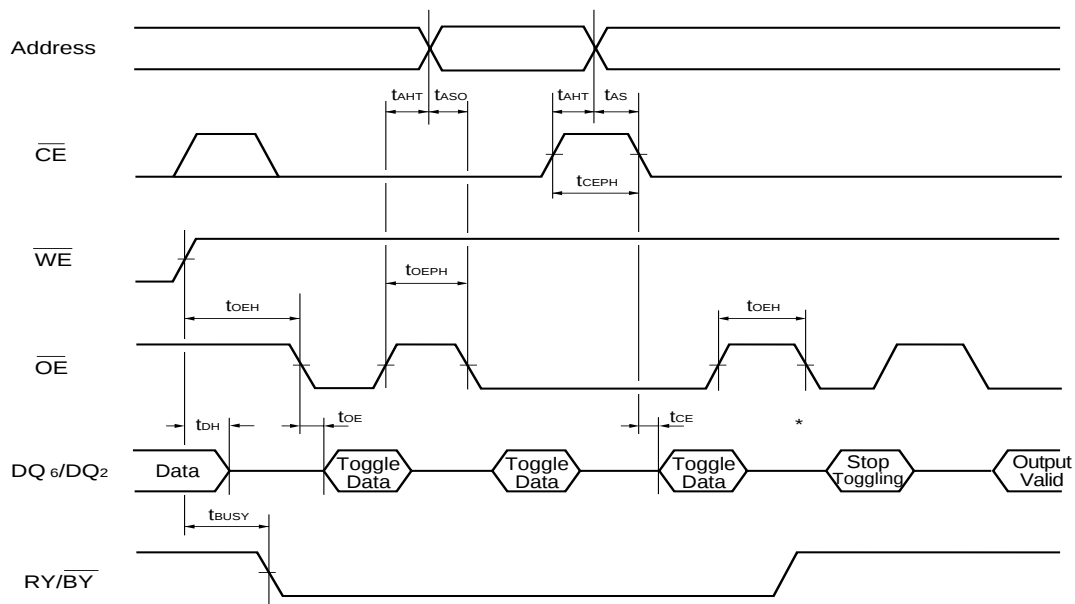
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• AC Waveforms for Data Polling during Embedded Algorithm Operations (Flash)



* : DQ_7 = Valid Data (The device has completed the Embedded operation).

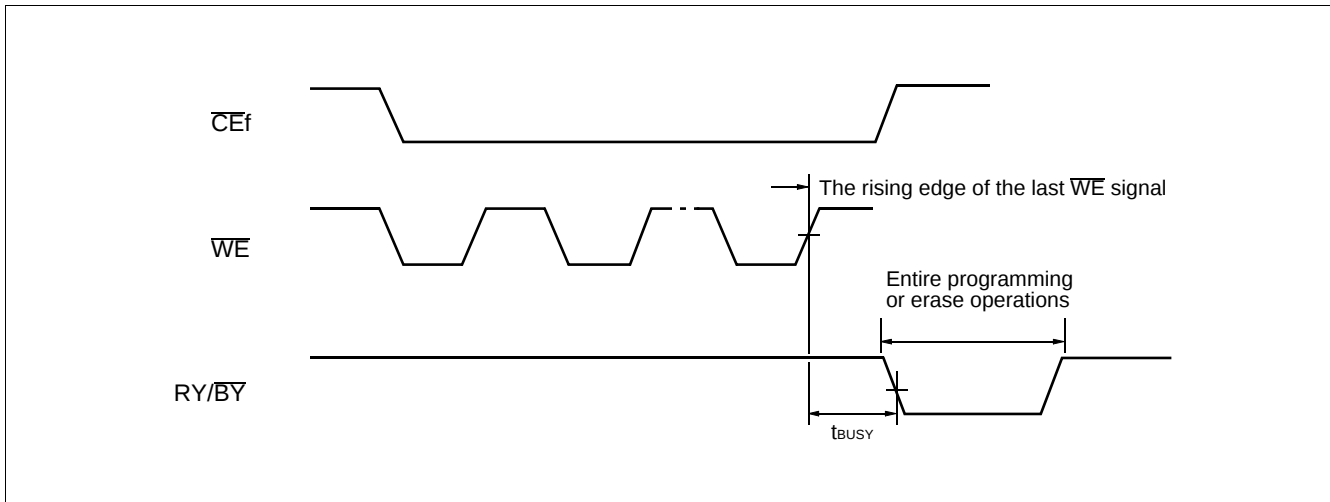
• AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)



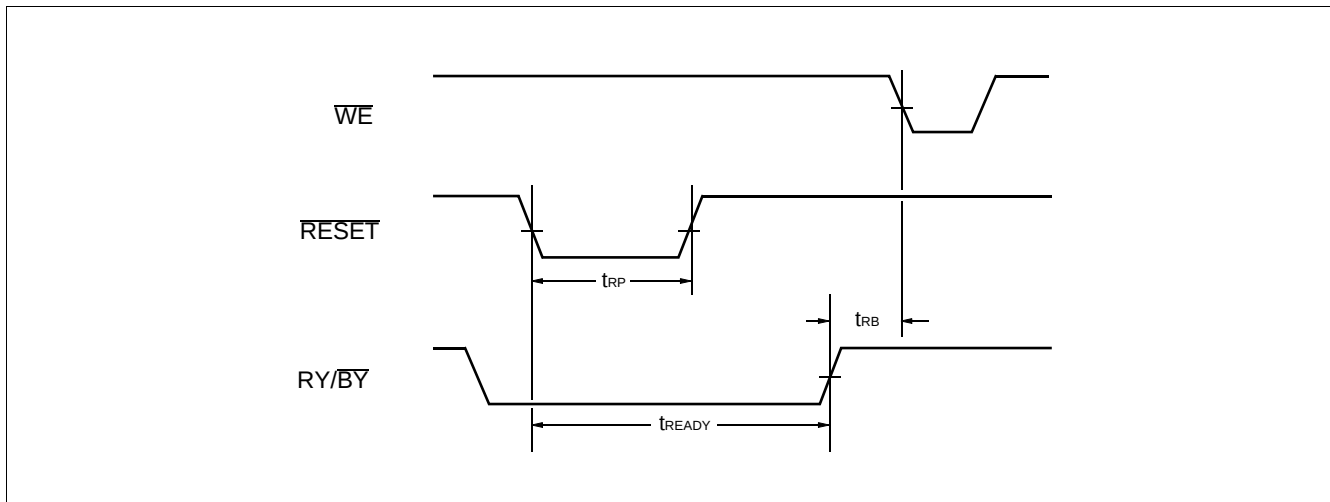
* : DQ_6 stops toggling (The device has completed the Embedded operation).

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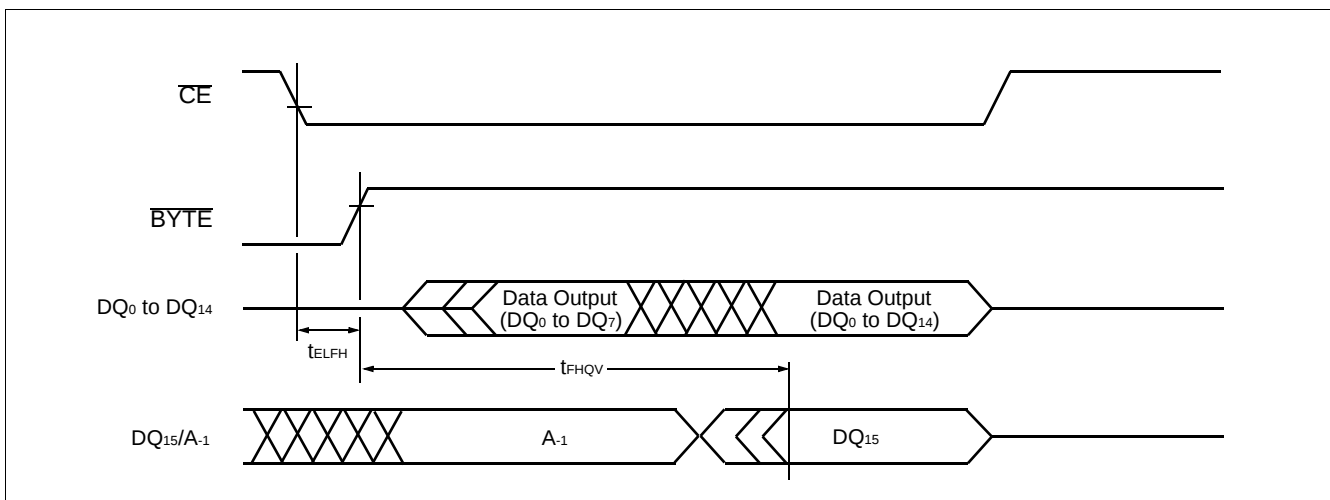
• RY/BY Timing Diagram during Write/Erase Operations (Flash)



• RESET, RY/BY Timing Diagram (Flash)

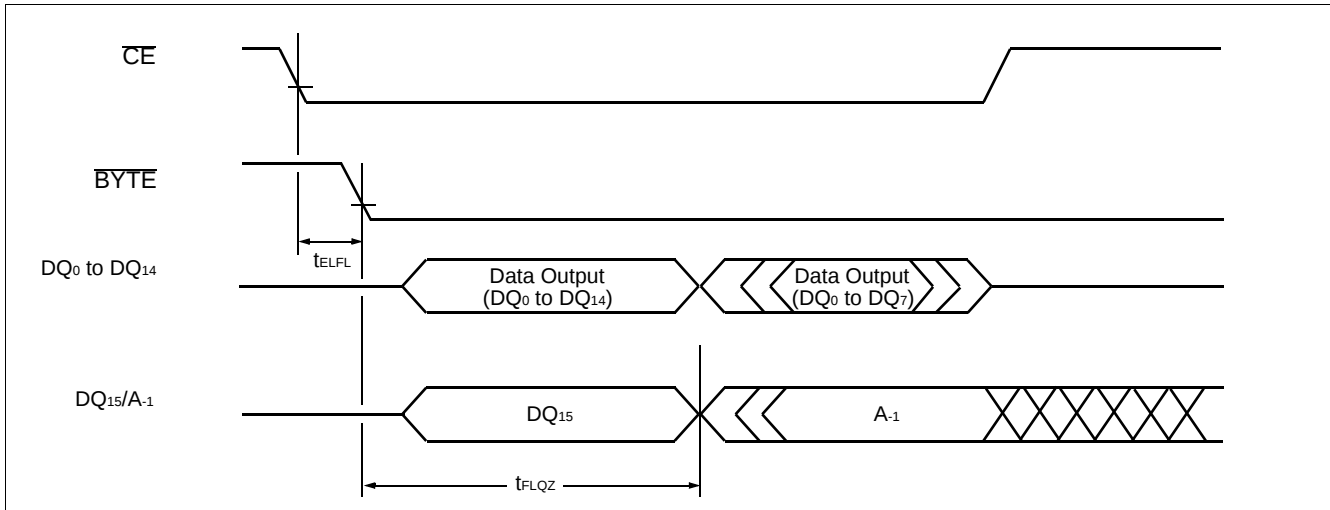


• Timing Diagram for Word Mode Configuration (Flash)

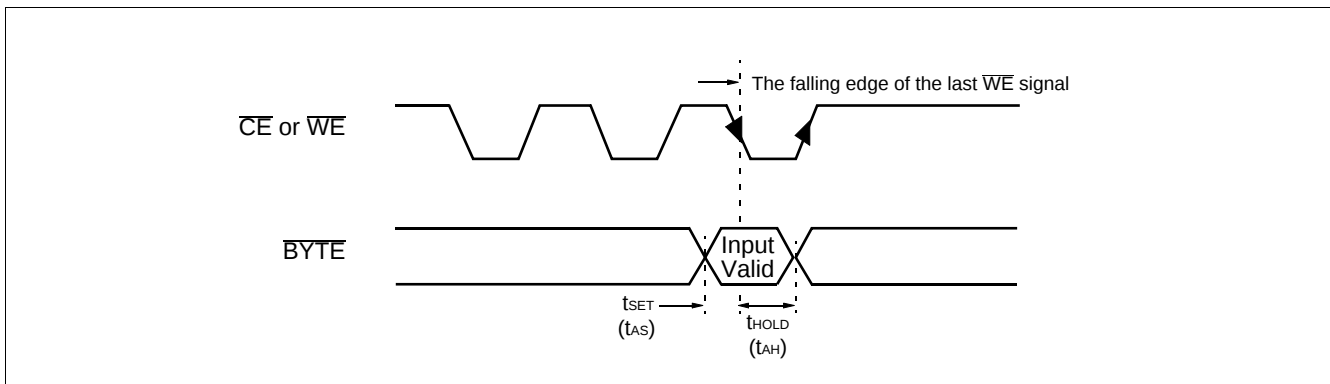


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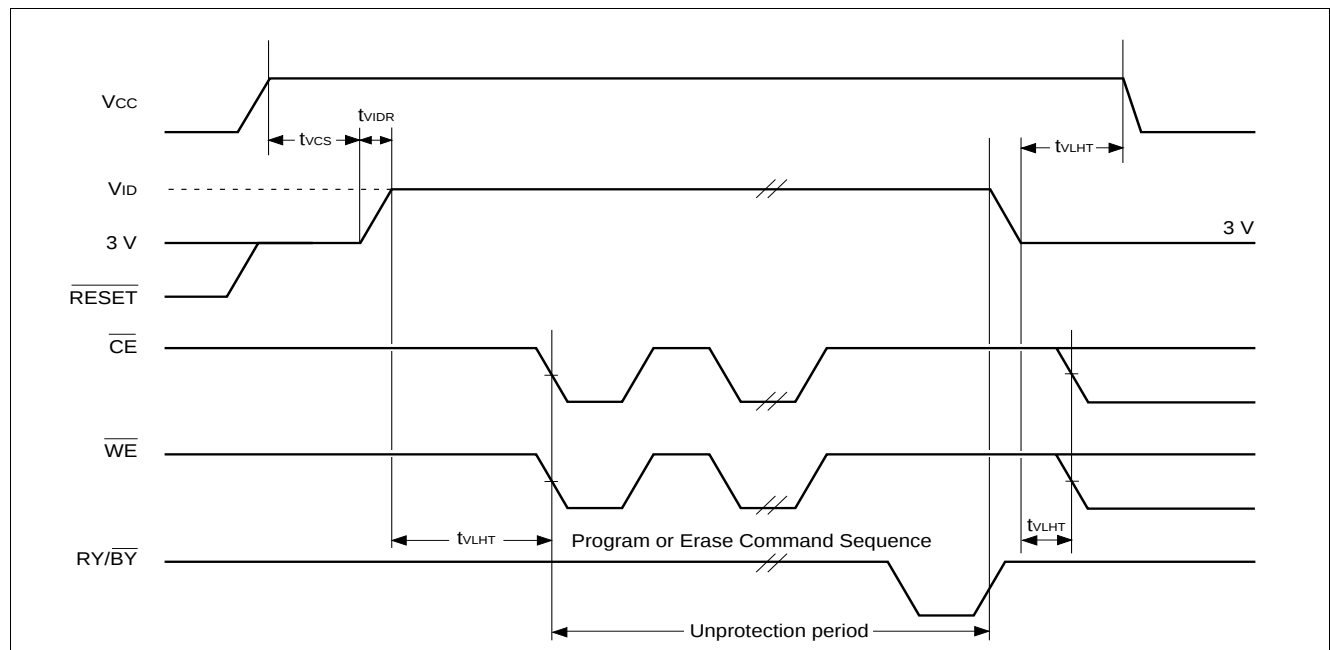
• Timing Diagram for Byte Mode Configuration (Flash)



• $\overline{BYTE}$ Timing Diagram for Write Operations (Flash)

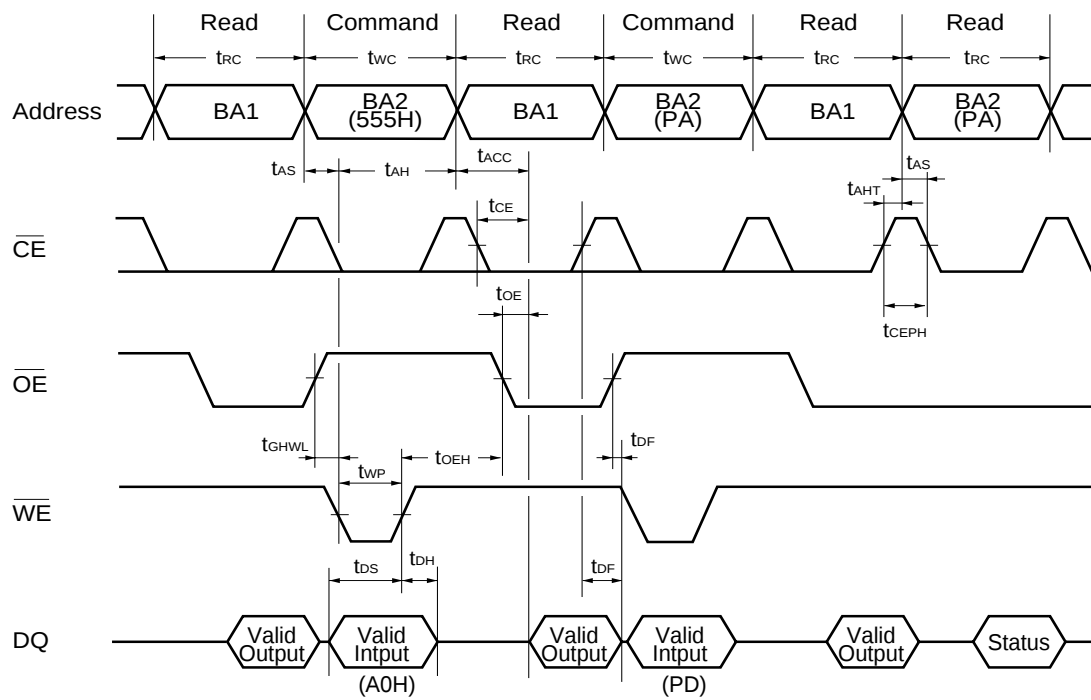


• Temporary Sector Unprotection (Flash)



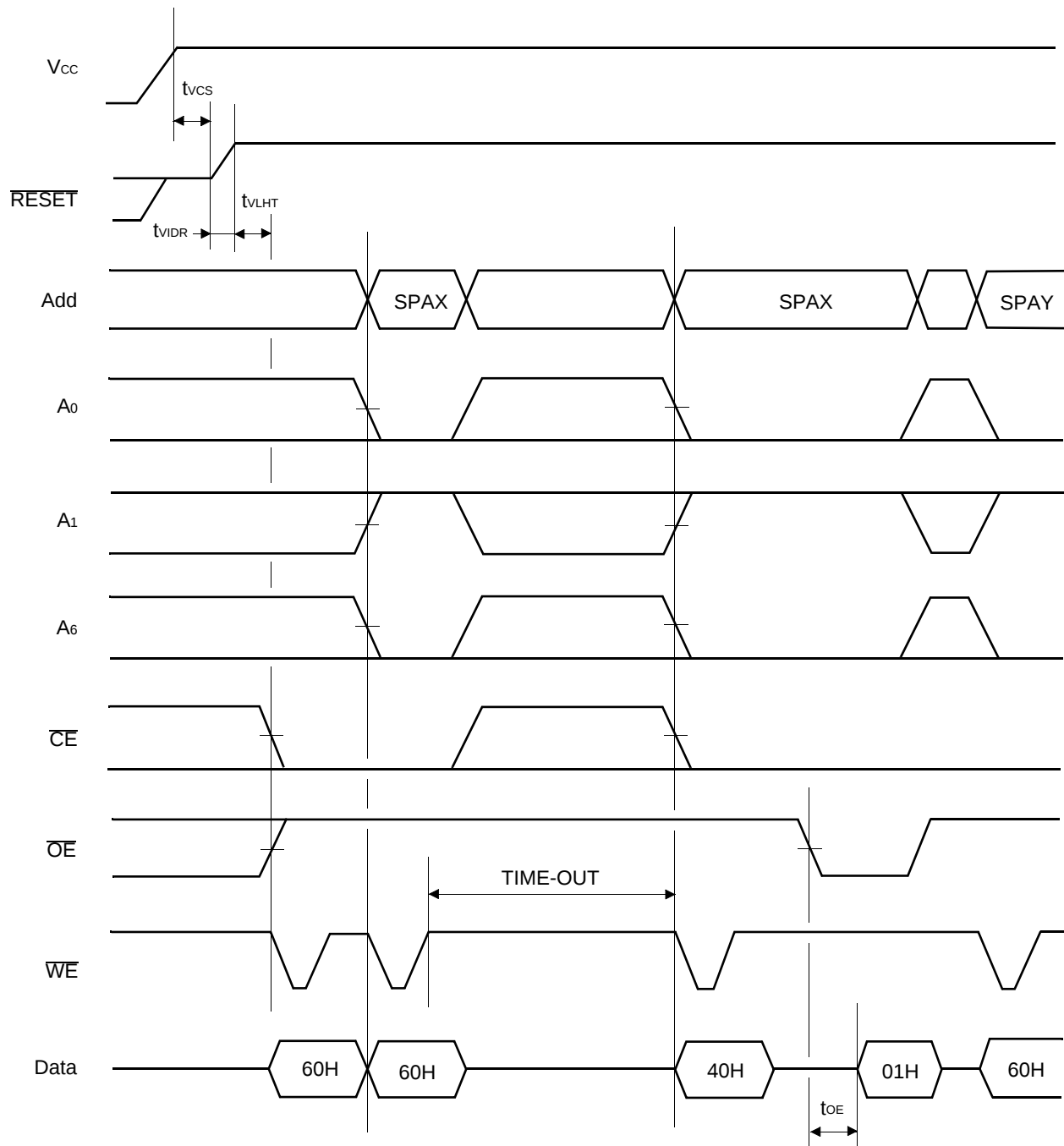
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• Back-to-back Read/Write Timing Diagram



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• Extended Sector Protection (Flash)



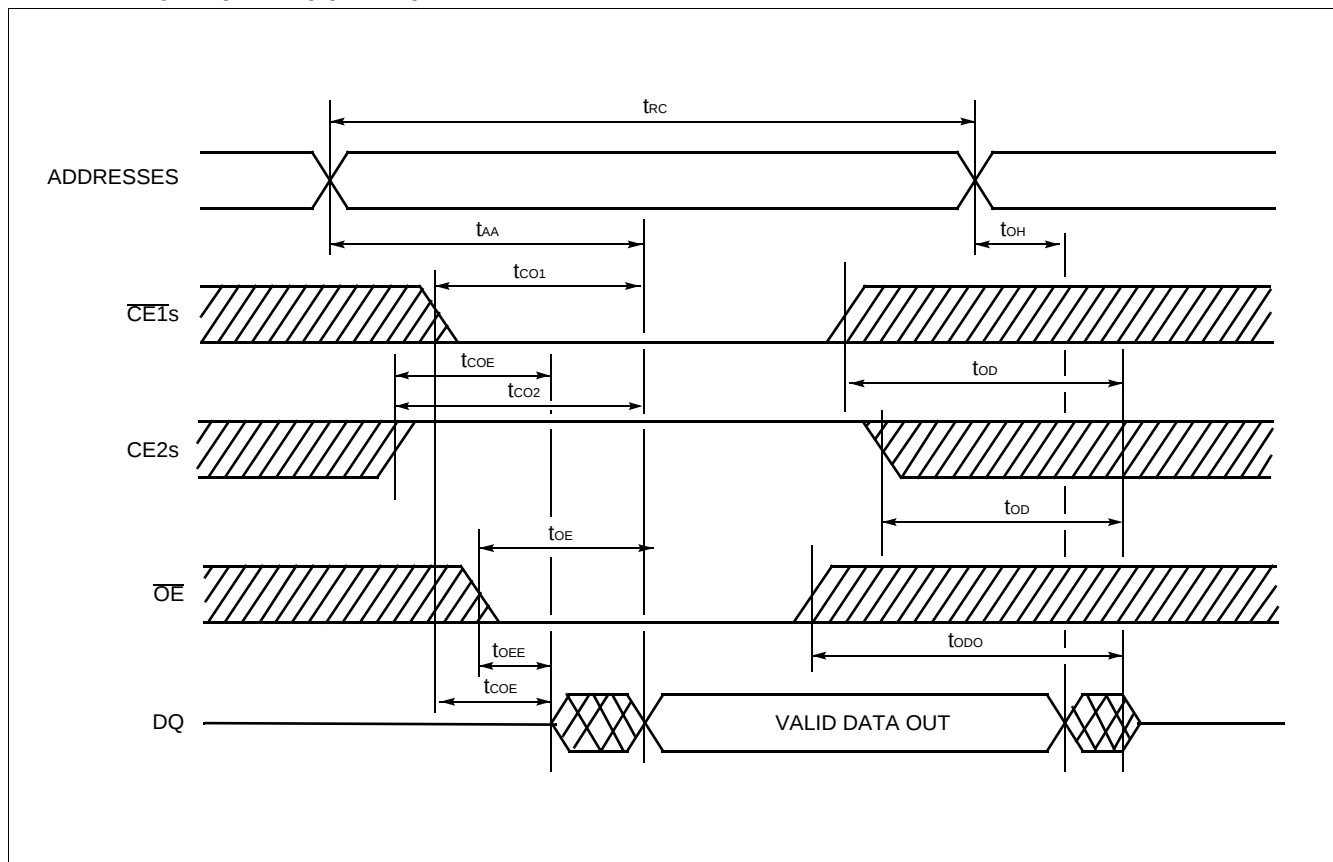
SPAX : Sector Address to be protected
 SPAY : Next Sector Address to be protected
 TIME-OUT : Time-Out window = 150 μ s (min)

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• Read Cycle (SRAM)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{RC}	Read Cycle Time	100	—	ns
t_{AA}	Address Access Time	—	100	ns
t_{CO1}	Chip Enable ($\overline{CE1}$ s) Access Time	—	100	ns
t_{CO2}	Chip Enable (CE2s) Access Time	—	100	ns
t_{OE}	Output Enable Access Time	—	50	ns
t_{COE}	Chip Enable ($\overline{CE1}$ s Low and CE2s High) to Output Active	5	—	ns
t_{OEE}	Output Enable Low to Output Active	0	—	ns
t_{OD}	Chip Enable ($\overline{CE1}$ s High or CE2s Low) to Output High-Z	—	40	ns
t_{ODO}	Output Enable High to Output High-Z	—	40	ns
t_{OH}	Output Data Hold Time	10	—	ns

• Read Cycle (Note 1) (SRAM)

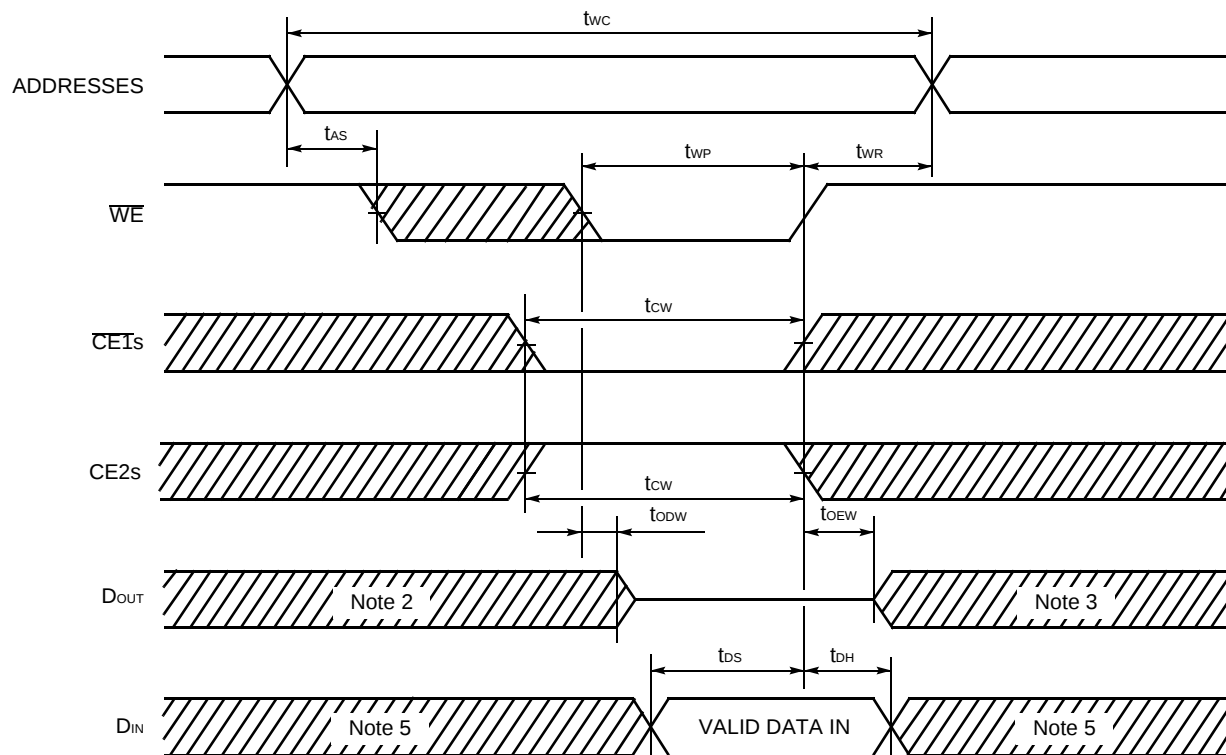


Note: 1. $\overline{WE}$ remains HIGH for the read cycle.

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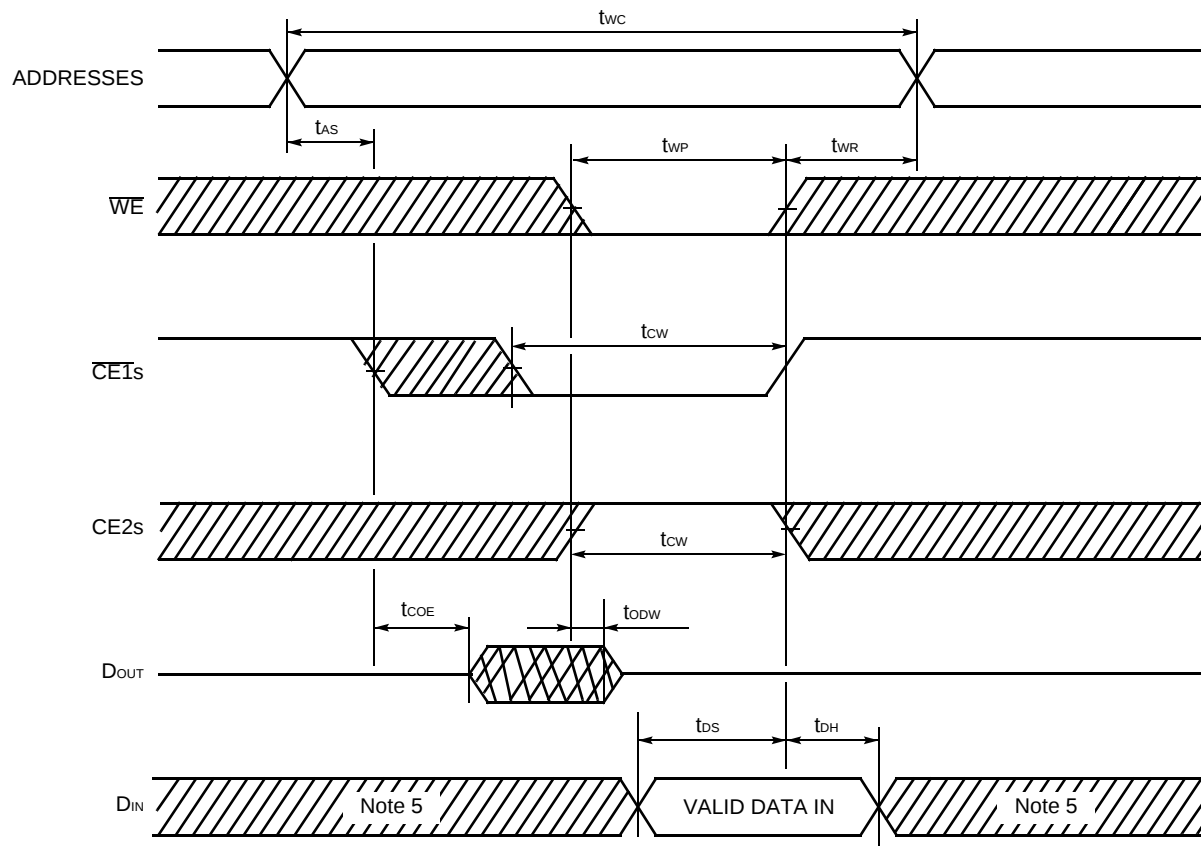
• Write Cycle (SRAM)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{WC}	Write Cycle Time	100	—	ns
t_{WP}	Write Pulse Width	60	—	ns
t_{CW}	Chip Enable to End of Write	80	—	ns
t_{AS}	Address Setup Time	0	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{ODW}	$\overline{WE}$ Low to Output High-Z	—	40	ns
t_{OEW}	$\overline{WE}$ High to Output Active	0	—	ns
t_{DS}	Data Setup Time	40	—	ns
t_{DH}	Data Hold Time	0	—	ns

• Write Cycle (Note 4) ($\overline{WE}$ control) (SRAM)

- Notes:**
2. If $\overline{CE1s}$ goes LOW (or $\overline{CE2s}$ goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.
 3. If $\overline{CE1s}$ goes HIGH (or $\overline{CE2s}$ goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
 4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
 5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

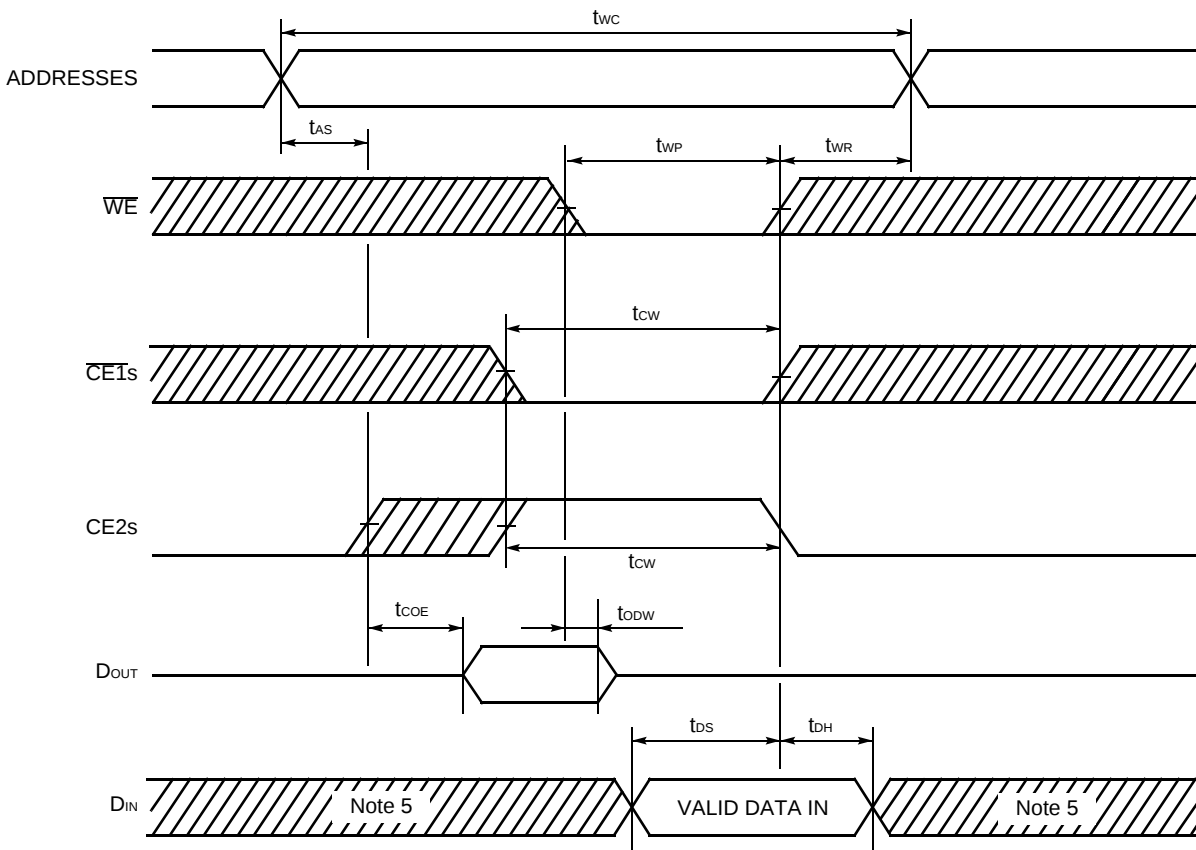
MB84VD2002-10/MB84VD2003-10

• Write Cycle (Note 4) ($\overline{CE1s}$ control) (SRAM)

- Notes:**
2. If $\overline{CE1s}$ goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.
 3. If $\overline{CE1s}$ goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
 4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
 5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

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• Write Cycle (Note 4) (CE2s Control) (SRAM)



- Notes:**
2. If $\overline{CE1s}$ goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.
 3. If $\overline{CE1s}$ goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
 4. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
 5. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

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■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

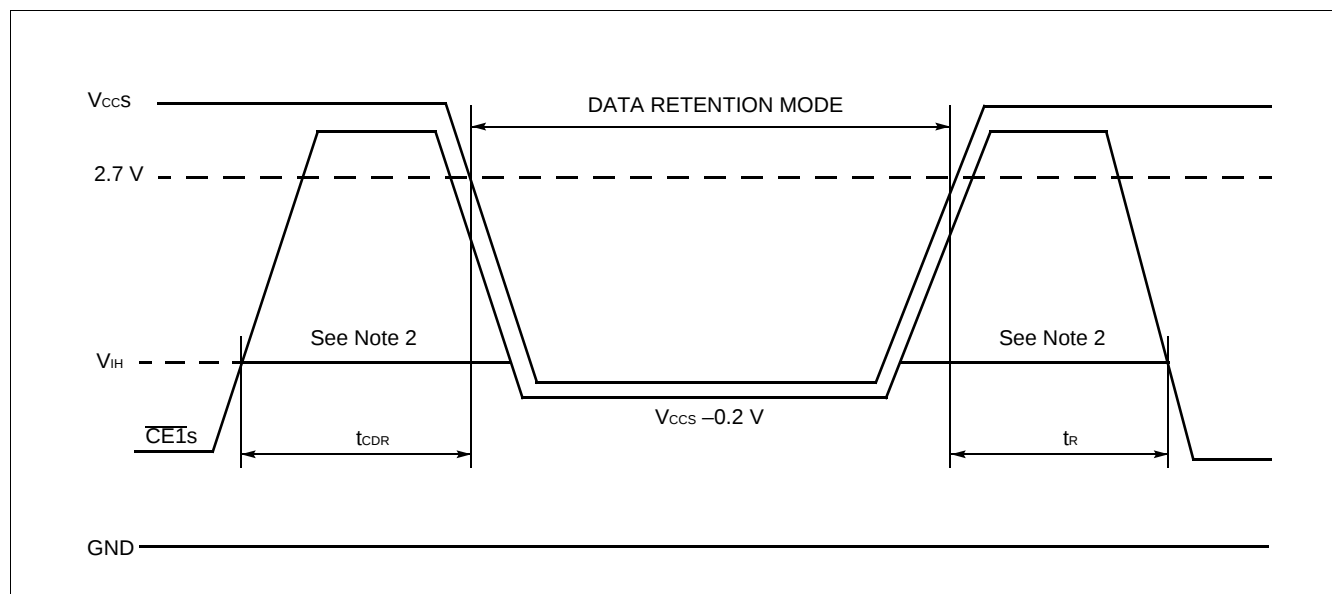
Parameter	Limits			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1	10	sec	Excludes programming time prior to erasure
Byte Programming Time	—	8	300	μs	Excludes system-level overhead
Word Programming Time	—	16	360	μs	
Chip Programming Time	—	8.4	T.B.D	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	

■ DATA RETENTION CHARACTERISTICS (SRAM)

Parameter Symbol	Parameter Description		Min.	Typ.	Max.	Unit
V _{DH}	Data Retention Supply Voltage		2.0	—	3.6	V
I _{DDS2}	Standby Current	V _{DH} = 3.0 V	—	—	50*	μA
		V _{DH} = 3.6 V	—	—	60	μA
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	ns
t _R	Recovery Time		5	—	—	ms

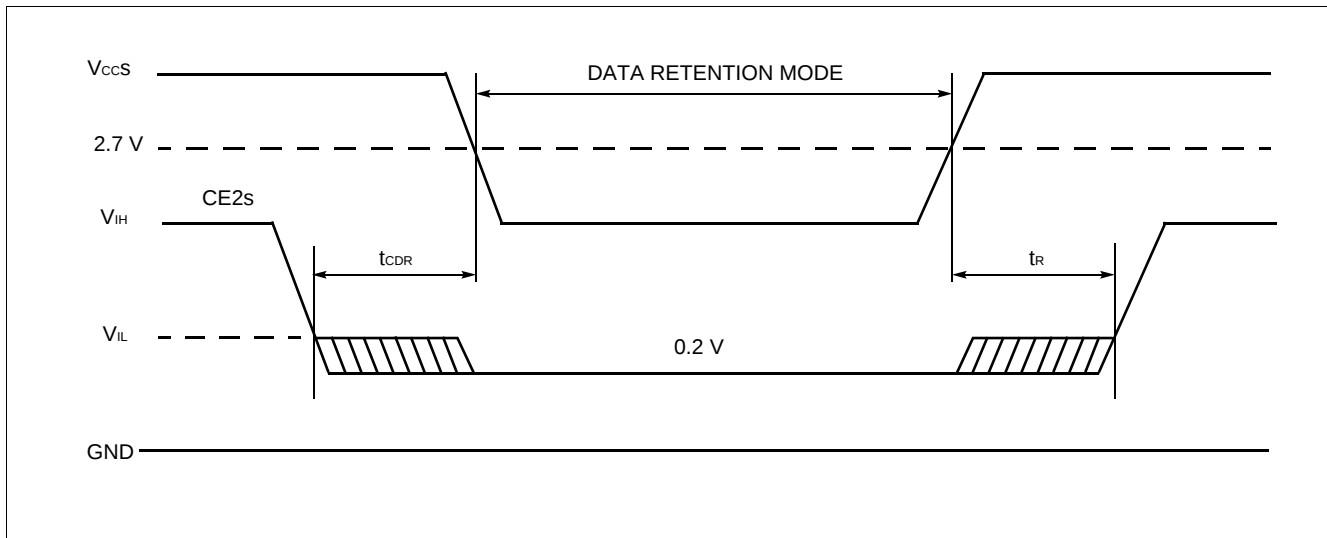
* : 5 μA (Max.) at T_A = −20°C to +40°C

• $\overline{CE1}$ s Controlled Data Retention Mode (Note 1)



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• CE2s Controlled Data Retention Mode (Note 3)



- Notes:**
1. In $\overline{CE1}$ s controlled data retention mode, input level of $CE2s$ should be fixed V_{CCS} to $V_{CCS}-0.2V$ or V_{SS} to 0.2V during data retention mode. Other input and input/output pins can be used between -0.3V to $V_{CCS}+0.3V$.
 2. When $\overline{CE1}$ s is operating at the V_{IH} min. level (2.2 V), the standby current is given by I_{SB1S} during the transition of V_{CCS} from 3.6 to 2.2 V.
 3. In $CE2s$ controlled data retention mode, input and input/output pins can be used between between -0.3V to $V_{CCS}+0.3V$.

■ PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	T.B.D	T.B.D	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	T.B.D	T.B.D	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	T.B.D	T.B.D	pF

Note: Test conditions $T_A = 25^\circ C$, $f = 1.0$ MHz

■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of packages are right angle.

■ CAUTION

- 1.)The high voltage (VID) can not apply to address pins and control pins except $\overline{RESET}$. Therefore, it can not use autoselect and sector protect function by applying the high voltage (VID) to specific pins.
- 2.)For the sector protection, since the high voltage (VID) can be applied to the $\overline{RESET}$, it can be protected the sector using "Extended sector protect" command.

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