

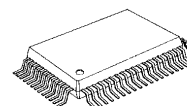
CMOS 8-Bit Microcontroller

TMP86PM74AFG

The TMP86PM74A is a OTP type MCU which includes 32-Kbyte one-time PROM. It is a pin compatible with a mask ROM product of the TMP86CK74A/CM74A. Writing the program to built-in PROM, the TMP86PM74A operates as the same way as the TMP86CK74A/CM74A. Using the Adapter socket, you can write and verify the data for the TMP86PM74A with a general-purpose PROM programmer same as TC571000D/AD.

Product No.	OTP	RAM	Package	Adapter Socket
TMP86PM74AFG	32 K × 8 bits	2 K × 8 bits	P-QFP80-1420-0.80M	BM11189

P-QFP80-1420-0.80M



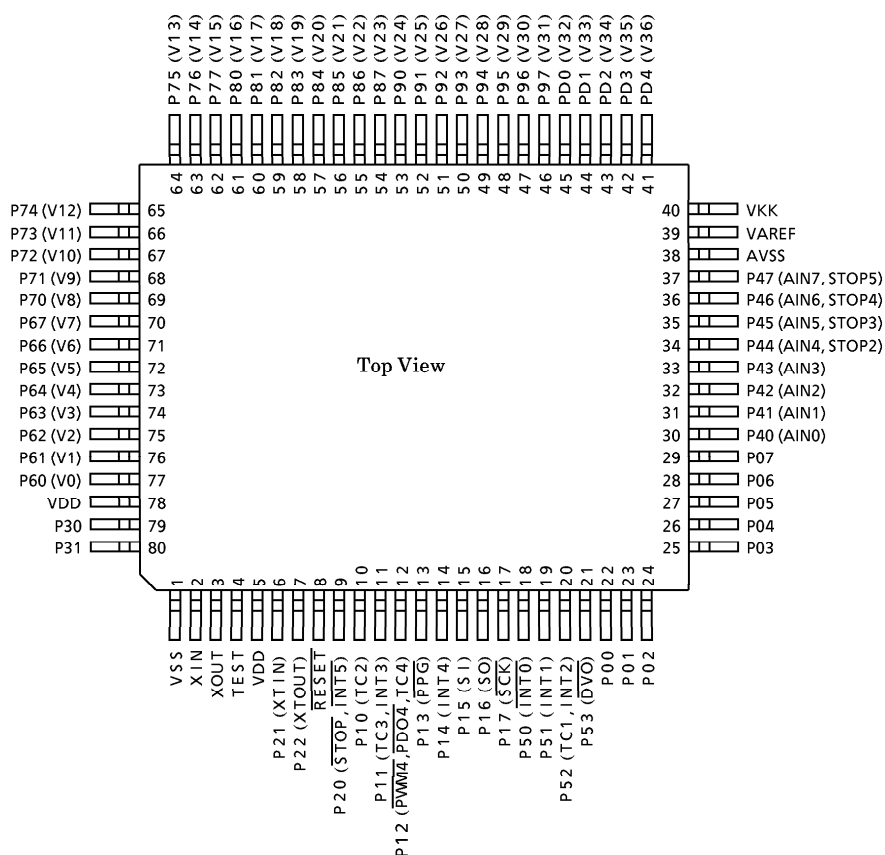
TMP86PM74AFG

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Pin Assignments (Top View)

P-QFP80-1420-0.80M



Pin Function

The TMP86PM74A has MCU mode and PROM mode.

(1) MCU mode

In the MCU mode, the TMP86PM74A is a pin compatible with the TMP86CK74A/CM74A (Make sure to fix the TEST pin to low level).

(2) PROM mode

Pin name (PROM mode)	Input/Output	Functions	Pin Name (MCU mode)
A16 to A12	Input	Input of Memory address for program	PD4 to PD0
A11 to A8			P53 to P50
A7 to A0			P47 to P40
D7 to D0	I/O	Input/Output of Memory data for program	P07 to P00
$\overline{CE}$	Input	Chip enable	P12
$\overline{OE}$		Output enable	P13
$\overline{PGM}$		Program control	P14
VPP	Power supply	+ 12.75 V/5 V (Power supply of program)	TEST
VDD		+ 6.25 V/5 V	VDD
GND		0 V	VSS
P11, P21	I/O	PROM mode setting pin. Fix to high.	
P10, P20, P22, AVSS, VAREF		PROM mode setting pin. Fix to low.	
RESET			
XIN	Input	Self oscillation with resonator (10 MHz)	
XOUT	Output		

Operation

This section describes the functions and basic operational blocks of TMP86PM74A.

The TMP86PM74A has PROM in place of the mask ROM which is included in the TMP86CK74A/CM74A.

In addition, TMP86PM74A operates as the single clock mode when releasing reset.

When using the dual clock mode, oscillate a low-frequency clock by [SET (SYSCR2). XTEN] command at the beginning of program.

1. Operating Mode

The TMP86PM74A has MCU mode and PROM mode.

1.1 MCU Mode

The MCU mode is set by fixing the TEST/VPP pin to the low level. (TEST/VPP pin cannot be used open because it has no built-in pull-down resistor).

1.1.1 Program memory

The TMP86PM74A has a 32 Kbyte built-in one time PROM (addresses 8000_H to FFFF_H in the MCU mode, addresses 0000_H to 7FFF_H in the PROM mode).

When using TMP86PM74A for evaluation of mask ROM products, the program is written in the program storing area shown in Figure 1-1.

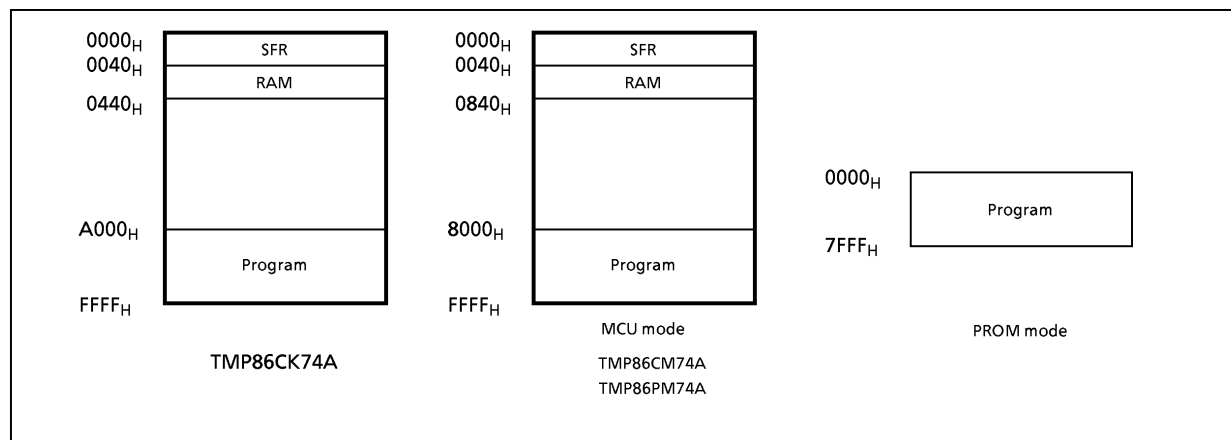


Figure 1-1. Program Memory Area

Note : The area that is not in use should be set data to FFH, or a general-purpose PROM programmer should be set only in the program memory area to access.

Electrical Characteristics

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter		Symbol	Pins	Rating	Unit
Supply Voltage		V _{DD}		– 0.3 to 6.5	V
Program Voltage		V _{PP}	TEST/V _{PP}	– 0.3 to 13.0	
Input Voltage		V _{IN}		– 0.3 to V _{DD} + 0.3	
Output Voltage		V _{OUT1}		– 0.3 to V _{DD} + 0.3	
		V _{OUT2}	Source open drain ports	V _{DD} – 41 to V _{DD} + 0.3	
Output Current (Per 1 pin)	IOL	I _{OUT1}	P0, P1, P2, P4, P5 ports	5	mA
		I _{OUT2}	P3 port	40	
	IOH	I _{OUT3}	P0, P1, P4, P5 ports	– 3	
		I _{OUT4}	P6, P7 ports	– 30	
		I _{OUT5}	P8, P9, PD ports	– 20	
	Output Current (Total)		ΣI _{OUT1}	P0, P1, P2, P3, P4, P5 ports	120
			ΣI _{OUT2}	P6, P7, P8, P9, PD ports	– 120
Power Dissipation [T _{opr} = 25°C]		PD		1200	mW
Soldering Temperature (time)		T _{sld}		260 (10 μ)	°C
Storage Temperature		T _{stg}		– 55 to 125	
Operating Temperature		T _{opr}		– 30 to 70	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition	($V_{SS} = 0\text{ V}$, $T_{opr} = -30\text{ to }70^{\circ}\text{C}$)
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Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply Voltage	V _{DD}		fc = 16 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz	NORMAL1, 2 mode	2.7		
				IDLE0, 1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
	STOP mode						
Output Voltage	V _{OUT3}	Source open drain ports			V _{DD} – 38	V _{DD}	
Input high Level	V _{IH1}	Except Hysteresis input	V _{DD} ≤ 4.5 V		V _{DD} × 0.70	V _{DD}	
	V _{IH2}	Hysteresis input			V _{DD} × 0.75		
	V _{IH3}	TTL input			V _{DD} × 0.90		
Input low Level	V _{IL1}	Except Hysteresis input	V _{DD} ≤ 4.5 V		0	V _{DD} × 0.30	
	V _{IL2}	Hysteresis input				V _{DD} × 0.25	
	V _{IL3}	TTL input			V _{DD} × 0.10	V _{DD}	
Clock Frequency	fc	XIN, XOUT	V _{DD} = 2.7 to 5.5 V		1.0	8.0	MHz
			V _{DD} = 4.5 to 5.5 V			16.0	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics (1)

(V_{DD} = 5 V)

[Condition] V_{DD} = 5.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, T_{opr} = -30~70°C
(Typ.: V_{DD} = 5.0 V, T_{opr} = 25°C, V_{in} = 5.0 V/0 V)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit	
Hysteresis Voltage	V _{HS}	Hysteresis input		–	0.9	–	V	
Input Current	I _{IN1}	TEST	V _{DD} = 5.5 V, V _{IN} = 5.5 V/0 V	–	–	± 2	μA	
	I _{IN2}	Sink Open Drain, Tri-st						
	I _{IN3}	RESET, STOP						
Input Resistance	R _{IN}	RESET Pull-Up		100	220	450	kΩ	
Pull-down Resistance	R _K	Source Open Drain, Tri-st	V _{DD} = 5.5 V, V _{KK} = – 30 V	50	80	110		
Output Leakage Current	I _{LO1}	Sink Open Drain, Tri-st	V _{DD} = 5.5 V, V _{OUT} = 5.5 V/0 V	–	–	± 2	μA	
	I _{LO2}	Source Open Drain	V _{DD} = 5.5 V, V _{KK} = – 32 V	–	–	± 2		
Output High Voltage	V _{OH}	Tri-st port	V _{DD} = 4.5 V, I _{OH} = – 0.7 mA	4.1	–	–	V	
Output Low Voltage	V _{OL1}	Except XOUT and P3 Port	V _{DD} = 4.5 V, I _{OL} = 1.6 mA	–	–	0.4		
Output High Current	I _{OH1}	P6, P7	V _{DD} = 4.5 V, V _{OH} = 2.4 V	– 18	– 28	–	mA	
	I _{OH2}	P8, P9, PD	V _{DD} = 4.5 V, V _{OH} = 2.4 V	– 9	– 14	–		
Output Low Current	I _{OL}	High Current Port (P3 port)	V _{DD} = 4.5 V, V _{OL} = 1.0 V	–	20	–		
Supply Current in NORMAL1, 2 mode	I _{DD}		f _c = 16.0 MHz f _s = 32.768 kHz	AD Converter Disable (IREF off)	–	12	18	
Supply Current in IDLE0, 1, 2 mode			f _c = 8.0 MHz f _s = 32.768 kHz		–	6	9	
			f _c = 16.0 MHz f _s = 32.768 kHz		–	6	9	
			f _c = 8.0 MHz f _s = 32.768 kHz		–	3	4.5	
Supply Current in NORMAL1, 2 mode			f _c = 16.0 MHz f _s = 32.768 kHz	AD Converter Enable	–	13	19	
			f _c = 8.0 MHz f _s = 32.768 kHz		–	7	10	
Supply Current in STOP mode			T _{opr} = to 50℃	AD Converter Disable	–	0.5	5	μA
			T _{opr} = to 70℃		–		10	

Note 1: Typical values show those at T_{opr} = 25°C, V_{DD} = 5 V.

Note 2: Input current (I_{IN1}, I_{IN3}); The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

DC Characteristics (2)

(V_{DD} = 3 V)

[Condition] V_{DD} = 3.0 V ± 10%, V_{SS} = A_{VSS} = 0 V, Topr = -30~70°C
(Typ.: V_{DD} = 3.0 V, Topr = 25°C, Vin = 3.0 V/0 V)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis Voltage	V _{HS}	Hysteresis input			–	0.4	–	V
Input Current	I _{IN1}	TEST	V _{DD} = 3.3 V, V _{IN} = 3.3 V/0 V		–	–	± 2	μA
	I _{IN2}	Sink Open Drain, Tri-st						
	I _{IN3}	RESET, STOP						
Input Resistance	R _{IN}	RESET Pull-Up			100	220	450	kΩ
Pull-down Resistance	R _K	Source Open Drain, Tri-st	V _{DD} = 3.3 V, V _{KK} = – 30 V		45	70	105	
Output Leakage Current	I _{LO1}	Sink Open Drain, Tri-st	V _{DD} = 3.3 V, V _{OUT} = 3.3 V/0 V		–	–	± 2	μA
	I _{LO2}	Source Open Drain	V _{DD} = 3.3 V, V _{KK} = – 32 V		–	–	± 2	
Output High Voltage	V _{OH}	Tri-st port	V _{DD} = 2.7 V, I _{OH} = – 0.6 mA		2.3	–	–	V
Output Low Voltage	V _{OL1}	Except XOUT and P3 Port	V _{DD} = 2.7 V, I _{OL} = 0.9 mA		–	–	0.4	
Output High Current	I _{OH1}	P6, P7	V _{DD} = 2.7 V, V _{OH} = 1.5 V		– 5.5	– 8	–	mA
	I _{OH2}	P8, P9, PD	V _{DD} = 2.7 V, V _{OH} = 1.5 V		– 3	– 4.5	–	
Output Low Current	I _{OL}	High Current Port (P3 port)	V _{DD} = 2.7 V, V _{OL} = 1.0 V		–	6	–	
Supply Current in NORMAL1, 2 mode	I _{DD}		fc = 8.0 MHz fs = 32.768 kHz	AD Converter Disable (IREF off)	–	3	4.5	mA
Supply Current in IDLE0, 1, 2 mode			fc = 8.0 MHz fs = 32.768 kHz		–	2	2.5	
Supply Current in NORMAL1, 2 mode			fc = 8.0 MHz fs = 32.768 kHz	AD Converter Enable	–	3.5	5	
Supply Current in SLOW1 mode			fs = 32.768 kHz	AD Converter Disable	–	30	60	μA
Supply Current in SLEEP0, 1 mode					–	15	30	
Supply Current in STOP mode					Topr = to 50°C	–	0.5	
	Topr = to 70°C	10						

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 3 V.

Note 2: Input current (I_{IN1}, I_{IN3}); The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent IDLE0, 1, 2.

AD Conversion Characteristics

(V_{SS} = 0.0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V _{AREF}		V _{DD} – 1.5	–	V _{DD}	V
Analog Reference GND	A _{VSS}		V _{SS}			
Analog Reference Voltage Range (Note 4)	Δ V _{AREF}		3.0	–	–	
Analog Input Voltage	V _{AIN}		V _{SS}	–	V _{AREF}	
Power Supply Current of Analog Reference Voltage	I _{REF}	V _{DD} = V _{AREF} = 5.5 V V _{SS} = A _{VSS} = 0.0 V	–	0.6	1.0	mA
Non linearity Error		V _{DD} = V _{AREF} = 4.5 to 5.0 V, V _{SS} = A _{VSS} = 0.0 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

(V_{SS} = 0.0 V, 2.7 V ≤ V_{DD} < 4.5 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage	V _{AREF}		V _{DD} – 1.5	–	V _{DD}	V
Analog Reference GND	A _{VSS}		V _{SS}			
Analog Reference Voltage Range (Note 4)	ΔV _{AREF}		2.5	–	–	
Analog Input Voltage	V _{AIN}		V _{SS}	–	V _{AREF}	
Power Supply Current of Analog Reference Voltage	I _{REF}	V _{DD} = V _{AREF} = 4.5 V V _{SS} = A _{VSS} = 0.0 V	–	0.5	0.8	mA
Non linearity Error		V _{DD} = A _{VDD} = 2.7 V to 4.5 V V _{SS} = A _{VSS} = 0.0 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to "2.11.2 Register Configuration".

Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} – V_{SS}.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range: ΔV_{AREF} = V_{AREF} – V_{SS}

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.25	–	4	μ s
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fc = 32.768 kHz	–	15.26	–	μ s
Low Level Clock Pulse Width	twcL					

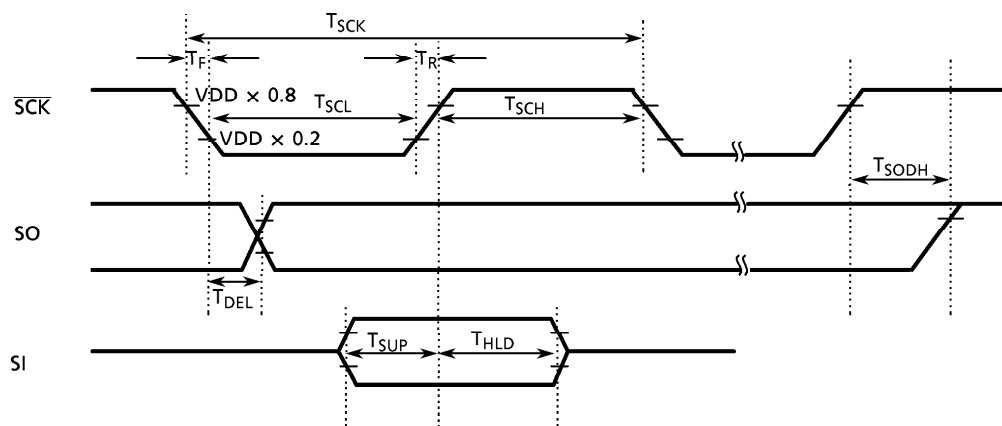
(V_{SS} = 0 V, V_{DD} = 2.7 to 4.5 V, T_{opr} = – 30 to 70°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1, 2 mode	0.5	–	8	μ s
		IDLE 1, 2 mode				
		SLOW 1, 2 mode	117.6	–	133.3	
		SLEEP 1, 2 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low Level Clock Pulse Width	twcL					
High Level Clock Pulse Width	twcH	For external clock operation (XTIN input) fc = 32.768 kHz	–	15.26	–	μ s
Low Level Clock Pulse Width	twcL					

HSIO AC Characteristics

 $(V_{SS} = 0\text{ V}, 2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}, T_{opr} = -30\text{ to }70^{\circ}\text{C})$

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
$\overline{\text{SCK}}$ output period (internal clock)	T_{SCK1}	$8\text{ MHz} < f_c \leq 16\text{ MHz}$ $V_{DD} = 4.5\text{ V to }5.5\text{ V}$	$16/f_c$	—	—	s
$\overline{\text{SCK}}$ output low width (internal clock)	T_{SCL1}		$8/f_c - 100\text{ ns}$	—	—	
$\overline{\text{SCK}}$ output high width (internal clock)	T_{SCH1}		$8/f_c - 100\text{ ns}$	—	—	
$\overline{\text{SCK}}$ output period (internal clock)	T_{SCK2}	$4\text{ MHz} < f_c \leq 8\text{ MHz}$ $V_{DD} = 2.7\text{ V to }5.5\text{ V}$	$8/f_c$	—	—	
$\overline{\text{SCK}}$ output low width (internal clock)	T_{SCL2}		$4/f_c - 100\text{ ns}$	—	—	
$\overline{\text{SCK}}$ output high width (internal clock)	T_{SCH2}		$4/f_c - 100\text{ ns}$	—	—	
$\overline{\text{SCK}}$ output period (internal clock)	T_{SCK3}	$f_c \leq 4\text{ MHz}$ $V_{DD} = 2.7\text{ V to }5.5\text{ V}$	$4/f_c$	—	—	
$\overline{\text{SCK}}$ output low width (internal clock)	T_{SCL3}		$2/f_c - 100\text{ ns}$	—	—	
$\overline{\text{SCK}}$ output high width (internal clock)	T_{SCH3}		$2/f_c - 100\text{ ns}$	—	—	
$\overline{\text{SCK}}$ input period (external clock)	T_{SCK4}	$f_c \leq 8\text{ MHz}$ ($V_{DD} = 2.7\text{ V to }5.5\text{ V}$)	1000	—	—	ns
$\overline{\text{SCK}}$ input low width (external clock)	T_{SCL4}		400	—	—	
$\overline{\text{SCK}}$ input low width (external clock)	T_{SCH4}		400	—	—	
SI input setup time	T_{SUP}	$V_{DD} = 3.0\text{ V}, CL = 50\text{ pF}$ (Note)	200	—	—	ns
SI input hold time	T_{HLD}		200	—	—	
SO output delay time	T_{DEL}		—	—	200	
Rising time	T_{R}		—	—	100	
Falling time	T_{F}		—	—	100	
SO last bit hold time	T_{SODH}		$16.5/f_c$	—	$32.5/f_c$	

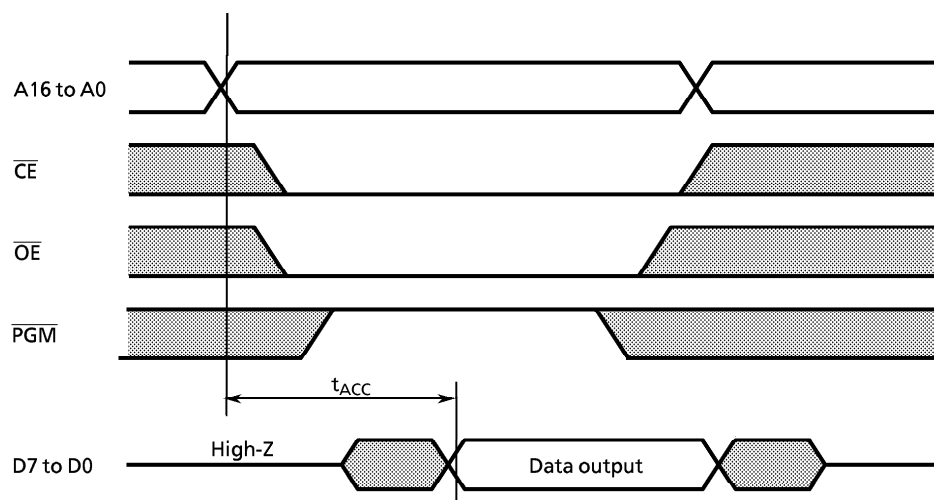
Note : CL , External Capacitance

DC Characteristics, AC Characteristics (PROM Mode) ($V_{SS} = 0\text{ V}$, $T_{opr} = 25 \pm 5^\circ\text{C}$)

(1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V _{IH3}		2.2	–	V _{DD}	V
Low leve input voltage (TTL)	V _{IL3}		0	–	0.8	
Power supply	V _{DD}		4.75	5.0	5.25	
Power supply of program	V _{PP}					
Address access time	t _{ACC}	V _{DD} = 5.0 ± 0.25 V	–	1.5t _{cyc} + 300	–	ns

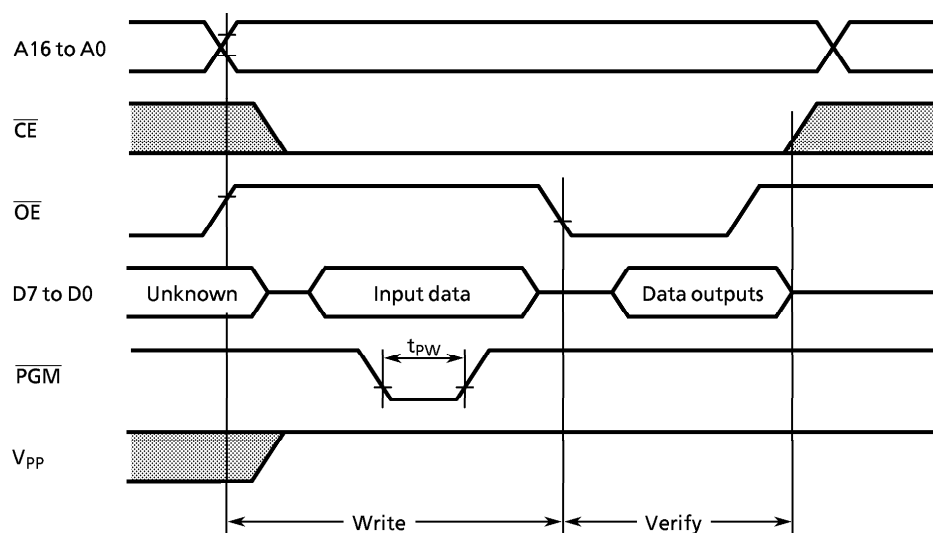
Note: $t_{cyc} = 400\text{ ns}$ at 10 MHz



(2) Program operation (High-speed) ($T_{opr} = 25 \pm 5^\circ\text{C}$)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage (TTL)	V_{IH3}		2.2	–	V_{DD}	V
Low level input voltage (TTL)	V_{IL3}		0	–	0.8	
Power supply	V_{DD}		6.0	6.25	6.5	
Power supply of program	V_{PP}		12.5	12.75	13.0	
Pulse width of initializing program	t_{PW}	$V_{DD} = 6.0\text{ V}$	0.095	0.1	0.105	ms

High-speed program writing



Note 1: The power supply of V_{PP} (12.75 V) must be set power-on at the same time or the later time for a power supply of V_{DD} and must be clear power-on at the same time or early time for a power supply of V_{DD} .

Note2 : The pulling up/down device on the condition of $V_{PP} = 12.75\text{ V} \pm 0.25\text{ V}$ causes a damage for the device. Do not pull up/down at programming.

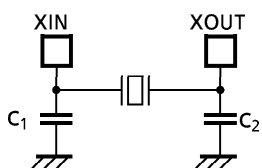
Note3 : Use the recommended adapter and mode.

Using other than the above condition may cause the trouble of the writting.

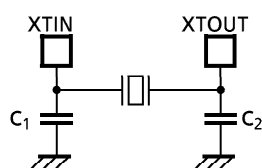
Recommended Oscillating Conditions

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	VDD	Recommended Oscillator	Recommended Constant	
					C ₁	C ₂
High-frequency Oscillation	Ceramic Resonator	16 MHz	4.5 V to 5.5 V	MURATA CSA16.00MXZ040	10 pF	10 pF
		8 MHz	2.7 V to 5.5 V	MURATA CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	2.7 V to 5.5 V	MURATA CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note2: When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.

Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change.

For up-to-date information, please refer to the following URL;

<http://www.murata.co.jp/search/index.html>