

T6M19, JT6M19-AS

T6M19, JT6M19-AS SINGLE-CHIP CMOS LSI FOR LCD CALCULATORS

The T6M19, JT6M19-AS is single-chip microcomputer for 10-digit + 2-digit scientific calculation.

T6M19, JT6M19-AS is the complete single-chip CMOS LSI for calculator with 10 digits, 67 functions, 3 expression and hexadecimal, octal and binary, statistic calculation, fractional number calculation, and logic operation with the following features.

FEATURES

- 12-digit display plus 2-digit code at the right margin.

- Scientific and engineering display.

Mantissa 10 digits plus exponent 2 digits plus negative code 2 digits.

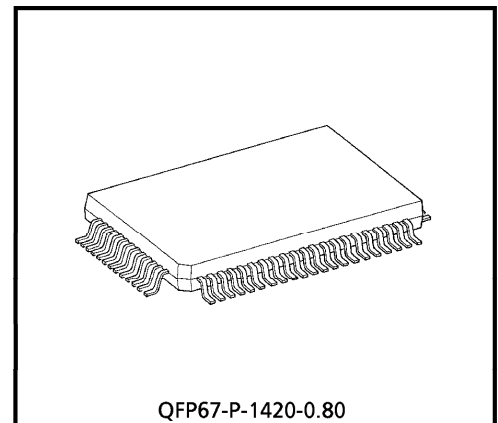
- Other than above

Mantissa 10 digits plus negative code 1 digit.

- 13 kinds of special display

M	Memory	HEX	Hexadecimal mode
-	Mantissa and exponent Minus	SD	Statistic calculation mode
E	Error	DEG	Degree
INV	Inverse	RAD	Radian
HYP	Hyperbolic	GRAD	Gradian
BIN	Binary mode	()	Parenthesis calculation
OCT	Octal mode		

- The minus sign of the mantissa is floating minus.
- The arithmetic key operation in clouding Y^x or $\sqrt[x]{Y}$ has same sequence as mathematical equation. 6 pending operations are allowed and () are up to continuous 15 levels.
- Fractional number calculation.
- It is possible to convert mutually between decimal, binary, octal and hexadecimal, and the 4 operations in arithmetic in binary, octal and hexadecimal.
- One independent accumulating memory.
- It is possible to convert or fix the display number system by FLO (Floating), SCI (Scientific) or ENG (Engineering) key.

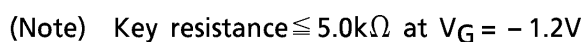


Weight : 1.20g (Typ.)

980910EBA2

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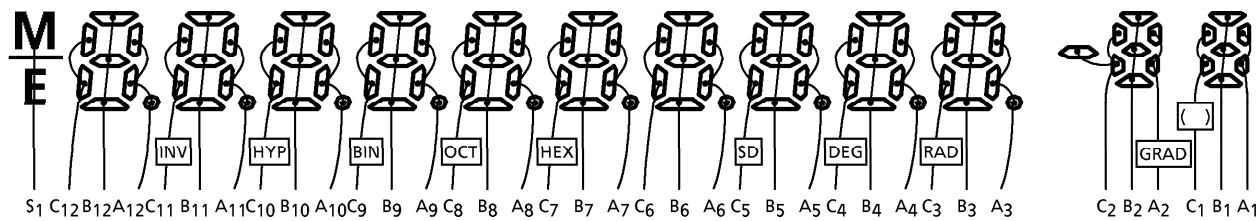
- ### SYSTEM BLOCK DIAGRAM



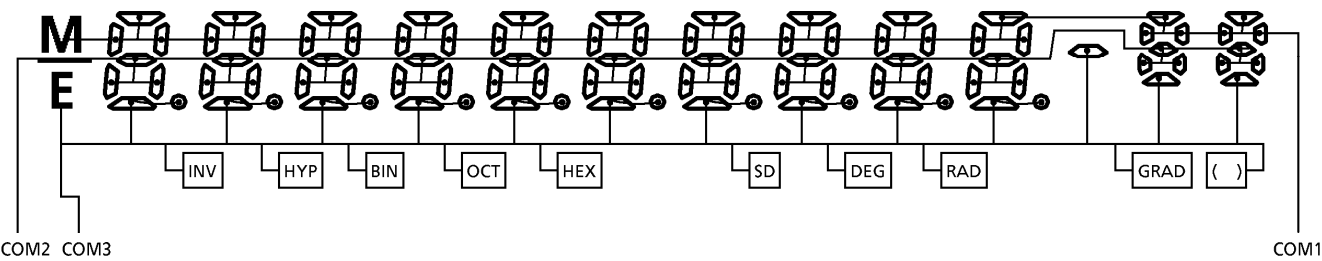
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CONNECTION OF LCD

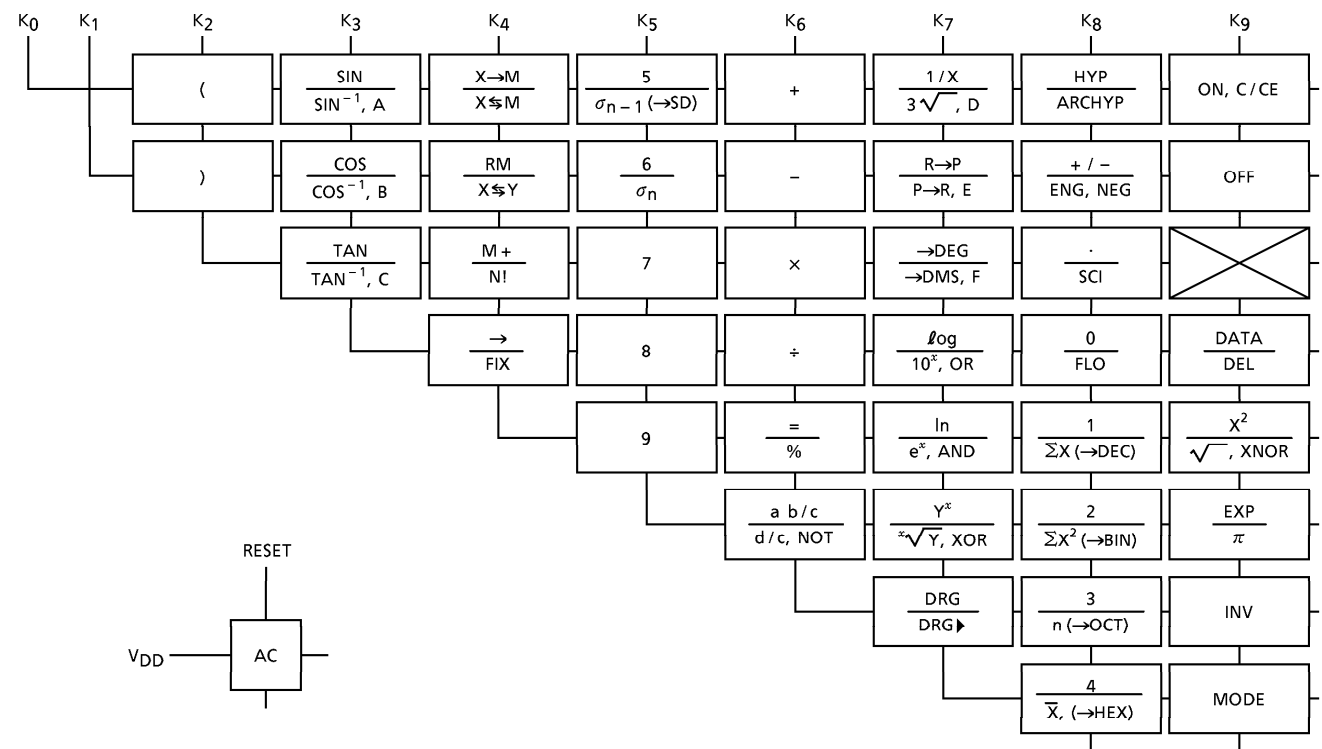
SEGMENT



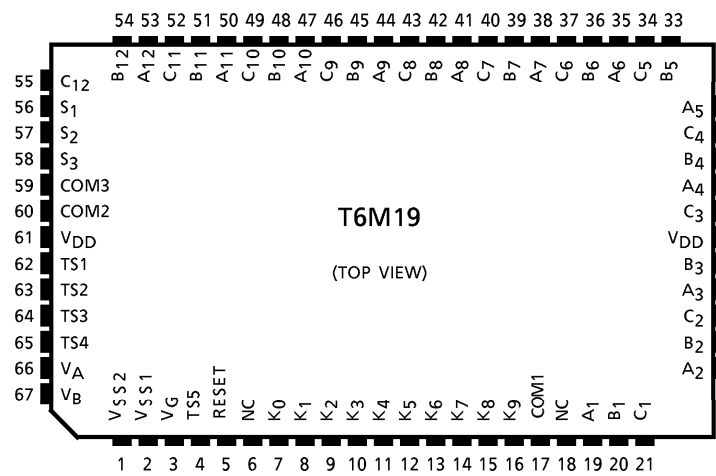
COMMON



KEY CONNECTION



PIN ASSIGNMENT



MAXIMUM RATINGS (Ta = 25°C)

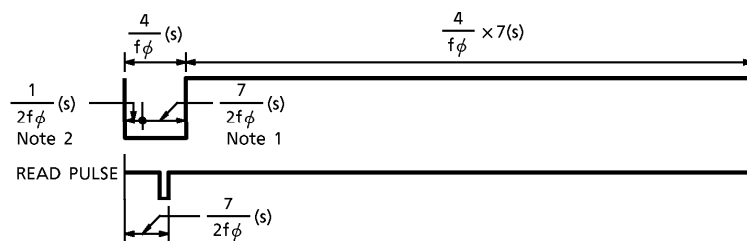
CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	VG	+ 0.3 ~ - 2.2	V
Input Voltage	VIN	+ 0.3 ~ VG - 0.3	V
Operating Temperature	Topr	0 ~ 40	°C
Storage Temperature	Tstg	- 55 ~ 125	°C

ELECTRICAL CHARACTERISTICS (VG = - 1.5V ± 0.2V, VSS2 = - 3.0 ± 0.4V, VDD = 0V, Ta = 25°C)

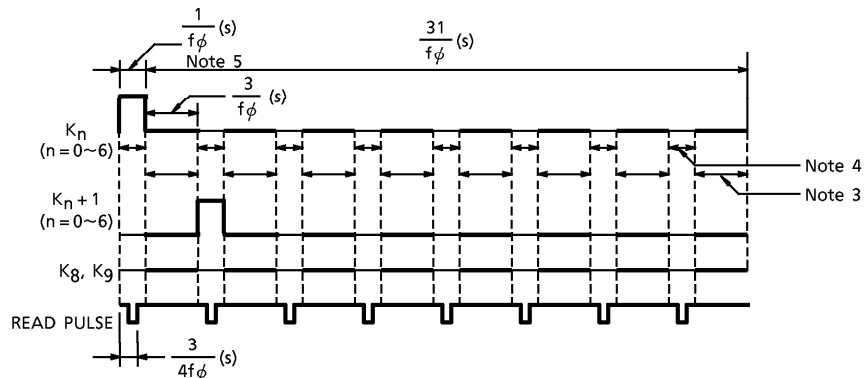
CHARACTERISTICS	SYMBOL	TEST CIR- CUIT	PIN NAME	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Voltage	VG	—	—	—	- 1.2	- 1.5	- 2.0	V
Supply Current (I)	IDD WAIT	—	—	VG = - 1.5V, wait	—	2.0	3.0	μA
Supply Current (II)	IDD OP	—	—	VG = - 1.2V, operate	—	4.5	7.0	μA
Supply Current (III)	IDD OFF	—	—	VG = - 1.5V, off	—	—	2.0	μA
Oscillating Frequency (I)	fφ WAIT	—	—	VG = - 1.5V, wait	5.4	9.0	12.6	kHz
Oscillating Frequency (II)	fφ OP	—	—	VG = - 1.5V, operate	14.4	24.0	33.6	kHz
Frame Frequency	fF	—	—	VG = - 1.5V, wait	56.3	93.8	131.3	Hz
"1" Input Voltage	VIH	—	K2~K9 RESET	—	VG + 0.4	—	VG	V
"0" Input Voltage	VIL	—	K2~K9 RESET	—	VSS	—	- 0.4	V
"1" Output Voltage	VOH (I)	—	SEGMENT COM1~3	—	VSS2 + 0.2	—	VSS2	V

CHARACTERISTICS	SYMBOL	TEST CIR- CUIT	PIN NAME	TEST CONDITION	MIN	TYP.	MAX	UNIT
"0" Output Voltage	$V_{OL} (I)$	—	SEGMENT COM1~3	—	V_{DD}	—	-0.2	V
"M" Output Voltage	V_{OH}	—	COM1~3	—	$V_{SS1} + 0.2$	—	$V_{SS1} - 0.2$	V
"1" Output Voltage	$V_{OH} (II)$	—	$K_0 \sim K_9$ RESET	—	$V_{SS1} + 0.2$	—	V_{SS1}	V
"0" Output Voltage	$V_{OL} (II)$	—	$K_0 \sim K_9$ RESET	—	V_{DD}	—	-0.2	V
"1" Output Resistance	R_{OH}	—	SEGMENT COM1~3	$V_{OUT} = V_{SS2} + 0.5V$	—	—	70	$k\Omega$
"0" Output Resistance	R_{OL}	—	SEGMENT COM1~3	$V_{OUT} = -0.5V$	—	—	70	$k\Omega$
RESET Pull Up Resistance (I)	$R_{RESETH} (I)$	—	RESET	$V_{OUT} = 0V$ (Note 1)	156	260	364	$k\Omega$
RESET Pull Up Resistance (II)	$R_{RESETH} (II)$	—	RESET	$V_{OUT} = 0V$ (Note 2)	18	75	300	$k\Omega$
Key Pull Up Resistance (I)	$R_{KEYH} (I)$	—	$K_0 \sim K_9$	$V_{OUT} = V_G + 0.5V$ (Note 3)	—	—	500	$k\Omega$
Key Pull Up Resistance (II)	R_{KEYH}	—	$K_0 \sim K_9$	$V_{OUT} = 0V$ (Note 4)	60	300	1500	$k\Omega$
Key RESET Pull Down Resistance	R_{KEYL} RESETL	—	$K_0 \sim K_9$ RESET	$V_{OUT} = -0.5V$ (Note 5)	—	—	25	$k\Omega$

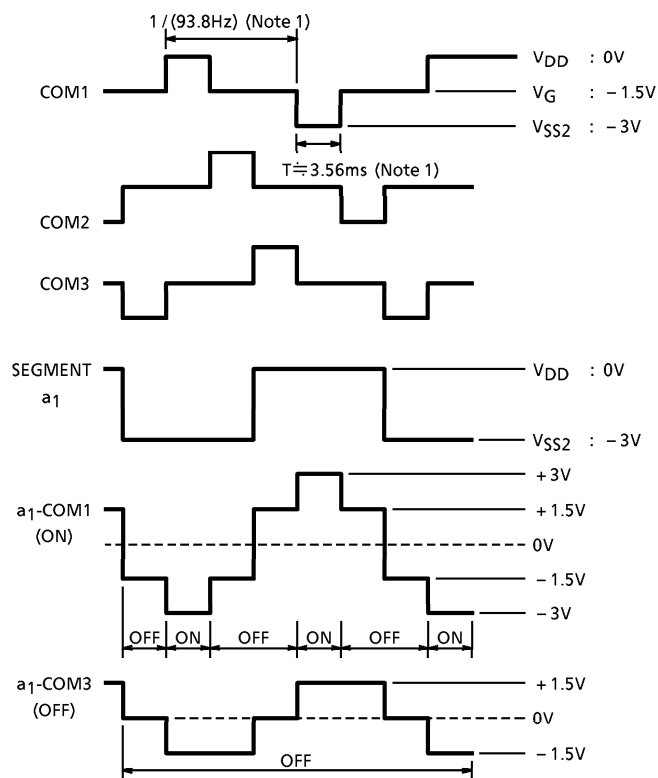
(Note 1, 2, 5) RESET Waveform, 1-cycle



(Note 3, 4, 5) KEY Waveform, 1-cycle



WAVEFORMS FOR DISPLAY



(Note 1) f_{ϕ} WAIT = 9kHz

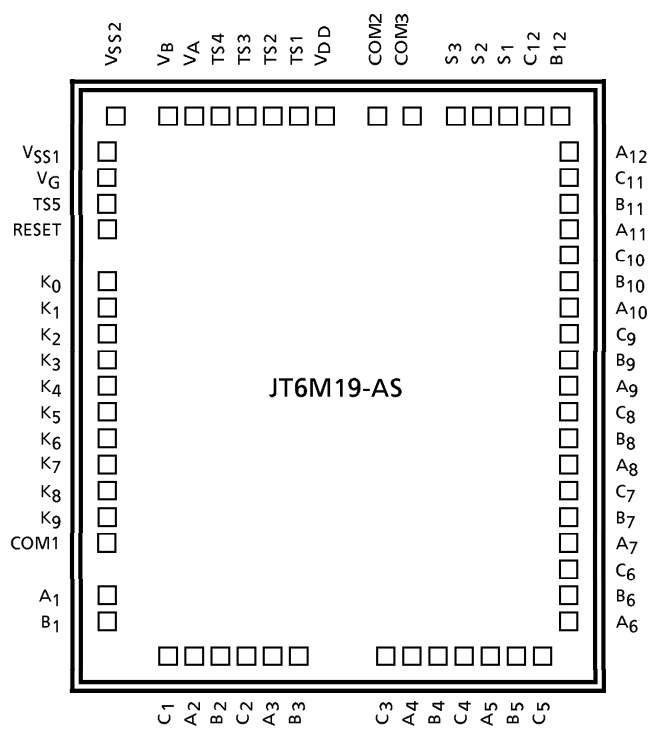
PAD LOCATION TABLE

(μm)

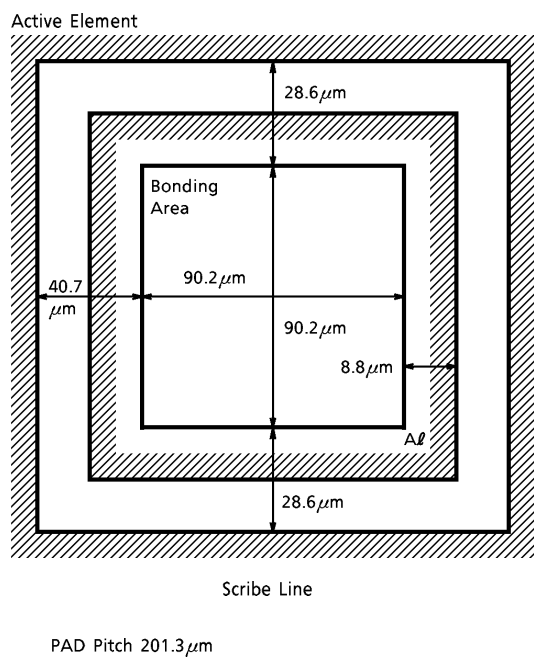
NAME	X POINT	Y POINT
V _{SS2}	- 1783	2330
V _{SS1}	- 1894	2102
V _G	- 1894	1901
TS5	- 1894	1690
RESET	- 1894	1469
K ₀	- 1894	1070
K ₁	- 1894	789
K ₂	- 1894	547
K ₃	- 1894	265
K ₄	- 1894	23
K ₅	- 1894	- 259
K ₆	- 1894	- 501
K ₇	- 1894	- 782
K ₈	- 1894	- 1024
K ₉	- 1894	- 1306
COM1	- 1894	- 1602
A ₁	- 1894	- 2023
B ₁	- 1894	- 2258
C ₁	- 1513	- 2330
A ₂	- 1277	- 2330
B ₂	- 1042	- 2330
C ₂	- 806	- 2330
A ₃	- 571	- 2330
B ₃	- 336	- 2330
C ₃	118	- 2330
A ₄	353	- 2330
B ₄	589	- 2330
C ₄	824	- 2330
A ₅	1059	- 2330
B ₅	1295	- 2330
C ₅	1530	- 2330
A ₆	1894	- 2234

NAME	X POINT	Y POINT
B ₆	1894	- 1937
C ₆	1894	- 1709
A ₇	1894	- 1482
B ₇	1894	- 1254
C ₇	1894	- 1026
A ₈	1894	- 799
B ₈	1894	- 571
C ₈	1894	- 343
A ₉	1894	- 116
B ₉	1894	112
C ₉	1894	332
A ₁₀	1894	557
B ₁₀	1894	784
C ₁₀	1894	1012
A ₁₁	1894	1240
B ₁₁	1894	1467
C ₁₁	1894	1695
A ₁₂	1894	1920
B ₁₂	1839	2330
C ₁₂	1606	2330
S ₁	1373	2330
S ₂	1140	2330
S ₃	902	2330
COM3	565	2330
COM2	295	2330
V _{DD}	- 51	2330
TS1	- 263	2330
TS2	- 484	2330
TS3	- 681	2330
TS4	- 888	2330
V _A	- 1124	2330
V _B	- 1371	2330

CHIP LAYOUT



PAD LAYOUT



QFP67-P-1420-0.80

Technical drawing of a rectangular PCB layout. The overall dimensions are 24.1±0.4 (width) and 18.1±0.4 (height). The layout features a central rectangular area with dimensions 20.0±0.2 (width) and 14.0±0.2 (height). The layout includes several component footprints, labeled with numbers: 54, 33, 55, 67, 32, 22, 1, 21, and 2. The layout is defined by a series of parallel lines, with dimensions indicating the spacing between them. Key dimensions include 2.0TYP, 1.2TYP, 2.2TYP, 3.8TYP, 2.0TYP, 0.3±0.1, 0.8, 2.0TYP, 0.15±0.1, 1.85±0.2, 2.25MAX, 0.2+0.1/-0.05, and 1.35±0.2.

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