0.6 Micron Sea of Gates

Introduction

The MG1 series is a 0.6 micron, array based, CMOS product family offering a new frontier in integration and speed. Several arrays up to 500k cells cover all system integration needs. The MG1 is manufactured using SCMOS 2/2, a 0.6 micron drawn, 3 metal layers CMOS process.

The MG1 series base cell architecture provides high routability of logic with extremely dense compiled memories : RAM, DPRAM and FIFO, ROM can be generated using synthesis tools. For instance, the largest array is capable of integrating 128K bits of DPRAM with 128K bits of ROM and over 200,000 random gates.

Accurate control of clock distribution can be achieved by PLL hardware and CTS (Clock Tree Synthesis) software. New noise prevention techniques are applied in the array and in the periphery : Three or more independent supplies, internal decoupling, customisation dependent supply routing, noise filtering, skew controlled I/Os, low swing differential I/Os, all contribute to improve the noise immunity and reduce the emission level.

The MG1 is supported by an advanced software environment based on industry standards linking proprietary and commercial tools. Cadence, Compass, Mentor, Synopsys and VHDL are the reference front end tools. Floor planning associated with timing driven layout provides a short back end cycle.

The MG1 family continues the Atmel Wireless & Microcontrollers offering in array based commercial, automotive, industrial, military and space circuits.

Features

- Full Range of Matrices up to 500k Cells
- 0.6 µm Drawn CMOS, 3 Metal Layers, Sea of Gates
- RAM, DPRAM, FIFO Compilers
- Library Optimised for Synthesis, Floor Plan & Automatic Test Generation (ATG)
- High Speed Performances :
  - 250 ps Typical Gate Delay @5 V
  - 350 MHz Toggle Frequency @5 V
- High System Frequency Skew Control :
  - 250 MHz PLL for Clock Generation
  - Clock Tree Synthesis Software
- 3 & 5 Volts Operation; Single or Dual Supply Modes
- Low Power Consumption :
  - 0.9 µW/Gate/MHz @3 V
  - 2.4 µW/Gate/MHz @5 V
- Integrated Power on Reset
- Matrices With More than 500 Pads
- Standard 3, 6, 12m, 24mA I/Os, parallelism up to 48mA
- Versatile I/O Cell : Input, Output, I/O, Supply, Oscillator
- CMOS/TTL/PCI Interface
- ESD (2 kV) And Latch-up Protected I/O
- High Noise & EMC Immunity :
  - I/O with Slew Rate Control
  - Internal Decoupling
  - Signal Filtering between Periphery & Core
  - Application Dependent Supply Routing & Several Independent Supply Sources
- Wide Range of Packages Including PGA & CQFP
- Delivery in Die Form
- Advanced CAD Support : Floor Plan, Proprietary Delay Models, Timing Driven Layout, Power Management
- Cadence, Compass, Mentor & Synopsys Reference Platforms
- EDIF & VHDL Reference Formats
- Upward Compatibility With MC & MF Gate Arrays, MCM Composite Arrays.
- Full Compatibility with MG1M Composite Sea of Gates Series
- Available In Commercial, Industrial, Automotive, Military & Space Quality Grades
- Special Versions on Radiation Tolerant Process
- QML Q

Product Outline

Type*	Total Cells	Maximum Usable Cells**	Full Programmable I/ Os***	Total Pads	Total Die Size with scribe line (um)
MG1001	1 829	1 371	30	50	2250x2260
MG1004	3 608	2 706	48	66	2710x2700
MG1009	9 100	6 825	72	91	3380x3360
MG1014*	13 846	10 384	88	106	3800x3790
MG1020	19 879	14 909	104	123	4240x4230
MG1033	32 984	24 738	130	148	5020x4990
MG1042*	42 000	31 500	146	165	5620x5590
MG1052	52 104	39 078	162	181	6070x6030
MG1070	70 059	52 544	188	206	6740x6730
MG1090*	89 162	66 871	212	231	7230x7370
MG1120	118 472	88 854	244	262	8090x8240
MG1140*	140 049	105 036	264	282	8660x8640
MG1200*	196 384	147 288	312	331	9960x10110
MG1265*	264 375	198 281	360	378	11460x11440
MG1480*	480 255	360 191	484	503	14690x14850

* Must be used when Ceramic Package is mandatory
** The maximum number of usable gates is application dependant
*** I/O pads may be configured as VSS or VDD supplies according to circuit requirements

Libraries

The MG1 cell library has been designed to take full advantage of the features offered by both logic and test synthesis tools.

Design testability is assured by the full support of SCAN, JTAG (IEEE 1149) and BIST methodologies.

More complex macro functions are available in VHDL, as example : I2C, UART, Timer, ...

Block Generators

Block generators are used to create a customer specific simulation model and metallisation pattern for regular functions like RAM, DPRAM & FIFO. The basic cell architecture allows one bit per cell for RAM and DPRAM. The main characteristics of these generators are summarised below.

Function	Maximum Size (bits)	bits/word	Typical characteristics (16 k bits)		
			access time (ns)	consumption (mA/MHz)	Used cells
RAM	72 k	1-144	8	1.6	20 k
DPRAM	72 k	1-144	8	3.3	23 k
FIFO	72 k	1-144	8	2.1	23 k

I/O buffer interfacing

I/O Fexibility

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator is located close to each buffer.

Inputs

Input buffers with CMOS or TTL thresholds are non inverting and feature versions with and without hysteresis. The CMOS and TTL input buffers may incorporate pull-up or pull down terminators. For special purposes, a buffer allowing direct input to the matrix core is available.

Outputs

Several kinds of CMOS and TTL output drivers are offered : fast buffers with 3, 6, 12 and 24 mA drive, low noise buffers with 12 mA drive.

Clock generation & PLL

Clock generation

Atmel Wireless & Microcontrollers offers 4 different types of oscillators : low power 32KHz crystal oscillator (up to Industrial Range), high frequency crystal oscillator and 2 RC oscillators. For all devices, the mark-space ratio is better than 40/60 and the start-up time less than 10 ms; the other characteristics are summarised below :

	Frequency (MHz)		Typical consumption (µA)
	Minimum	Maximum	
Xtal 32K	0.03	0.034	30
Xtal 50 M	2	50	2 000
RC 10M	0.02	10	15 00
RC 32 M	10	32	2 500

PLL

Two independent PLL devices are located in upper left and lower right corners. Each may be used for the following functions :

– Synchronisation of an internal clock on a reference system clock.

– Skew control : the internal clock transitions are synchronous with the reference clock whatever the load and the depth of logic in the clock tree.

– Frequency synthesis : two frequency dividers are included in each PLL. One divides the reference clock frequency F0 by a factor M and the other divides the internal clock frequency F by N. The internal clock frequency is :

$$F = F0 * M / N$$

Both M and N can take values from 1 to 16.

The maximum frequency at the PLL input after division by M is 70 MHz.

The maximum internal clock frequency is 250 MHz at 5 V and 150 MHz at 3 V ; the minimum frequency is 20 MHz.

Each PLL corner block has 6 dedicated pads : 2 VDD, 3 VSS and a filtering I/O connected to an RC network.

Power supply & noise protection

The speed and density of the SCMOS 2/2 technology causes large switching current spikes for example either when :

16 high current output buffers switch simultaneously,
or
10% of the 500 000 gates are switching within a window of 1ns .

Sharp edges and high currents cause some parasitic elements in the packaging to become significant. In this frequency range, the package inductance and series resistance should be taken into account. It is known that an inductor slows down the settling time of the current and causes voltage drops on the power supply lines. These drops can affect the behaviour of the circuit itself or disturb the external application (ground bounce).

In order to improve the noise immunity of the MG core matrix, several mechanisms have been implemented inside the MG arrays. Two kinds of protection have been added : one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the matrix.

I/O Buffers switching protection

Three features are implemented to limit the noise generated by the switching current :

The power supplies of the input and output buffers are separated.

The rise and fall times of the output buffers can be controlled by an internal regulator.

A design rule concerning the number of buffers connected on the same power supply line has been imposed.

Matrix switching current protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added :

Some decoupling capacitors are integrated directly on the silicon to reduce the power supply drop.

A power supply network has been implemented in the matrix. This solution lessens the parasitic elements such as inductance and resistance and constitutes an artificial VDD and Ground plane. One mesh of the network supplies approximately 150 cells.

A low pass filter has been added between the matrix and the input to the output buffer. This limits the transmission of the noise coming from the ground or the VDD supply of the matrix to the external world via the output buffers.

Power consumption

The power consumption of an MG1 array is due to three factors : leakage (P1), core (P2) and I/O (P3) consumption.

$$P = P1 + P2 + P3$$

Standby Power Consumption

The consumption due to leakage currents may be defined as :

$$P1 = (VDD - VSS) * I_{CCSB} * N_{CELL}$$

Where I_{CCSB} is the leakage current through a polarised basic gate and N_{CELL} is the number of used cells.

Core Power Consumption

The consumtion due to the switching of cells in the core of the matrix is bounded by :

$$P2 = N_{CELL} * P_{GATE} * C_{ACTIVITY} * F$$

Where N_{CELL} is the number of used cells, F the data toggling frequency is equal to half the clock frequency for random data and P_{GATE} is the power consumption per cell.

$$P_{GATE} = P_{CA} + P_{CO}$$

ACTIVITY is the fraction of the total number of cells toggling per cycle.

Capacitance Power

$$P_{CA} = C * (VDD - VSS)^2/2$$

C is the total output capacitance and may be expressed as the sum of the drain capacitance of the driver, the wiring capacitance and the gate capacitance of the inputs.

Worst case value : PCA # 1.8 µW/gate/MHz @ 5 V

Commutation Power

$$P_{CO} = (VDD - VSS) * I_{dsohm}$$

Where I_{dsohm} is the current flowing into the driver between supply and ground during the commutation. I_{dsohm} is about 15 % of the Pmos saturation currrent. Worst case value : Pco # 0.7 µW/gate/MHz @ 5 V

I/O Power Consumption

The power consumption due to the I/Os is :

$$P3 = Ni * C_O * (VDD - VSS)^2 * Fi/2$$

With Ni equals to the number of buffers running at Fi and C_O is the output capacitance.

Note : If a signal is a clock, Fi = F, if it is a data with random values, Fi = F/4.

Power Consumption Example

Matrix	MG1265
Used gates (70 %)	185 k
Voltage	5 V**
Frequency	40 MHz
Standby Power	
Iccsb (125°C)	1 nA
$P1 = (VDD - VSS) * I_{CCSB} * N_{CELL}$	1 mW
Core Power	
Power Consumption per Cell	2.4 µW/Gate/MHz
$C_{activity}$	20 %
$P2 = N_{CELL} * P_{GATE} * C_{activity} * F$	1775 mW
I/O Power	
Total Number of Buffers	364
Number of Outputs and I/O Buffers	100
Output Capacitance	50 pF
$P3 = Ni * C_O * (VDD - VSS)^2 * Fi/2$	625 mW
Total Power	
P = P1 + P2 + P3	2.41 W

** Using 3V supply the power consumption will be reduced to 900mW

Packaging

Atmel Wireless & Microcontrollers offers a wide range of packaging options which are listed below :

Package Type	Pins min/max**	Lead spacing (inch*)	Dimension (inch*)
DQFP	100 128	0.0256 0.0315	0.546x0.782 1.102^2
PLCCJ	28 84	0.050 0.050	0.453^2 0.653^2
PQFP	44 240	0.0315 0.0197	0.389^2 1.26^2
TQFB	44 64	0.0394 0.0315	0.394^2 0.551^2
VQFP	64 140	0.0197 0.0197	0.390^2 0.787^2
SSOP	16	0.0256	0.209x0.244
PSO	8 28	0.050 0.050	0.153x0.194 0.705x0.295
MLCC	68 84	0.050 0.050	0.950^2 1.150^2
MQFP	100 352	0.0256 0.020	0.787x0.551 1.889^2
CQFP	44	0.050	0.650^2
MPGA	176 256	0.10 0.10	1.5^2 2.0^2

* To get the linear values in milimeters, multiply by 25.4

** Please contact Atmel Wireless & Microcontrollers Local Design Contes to check the availability of the use matrix and the plan package.

Design flows & tools

Design Flows and modes

A generic design flow for an MG1 array is sketched on next page.

A top down design methodology is proposed which starts with high level system description and is refined in successive design steps. At each step, structural verification is performed which includes the following tasks :

– Gate level logic simulation and comparison with high level simulation results.

– Design and test rule check.

– Power consumption analysis.

– Timing analysis (only after floor plan).

The main design stages are :

– System specification, preferably in VHDL form.

– Functional description at RTL level.

– Logic synthesis.

– Floor planning and bonding diagram generation.

– Test insertion, ATG and/or fault simulation.

– Physical cell placement, JTAG insertion and clock tree synthesis.

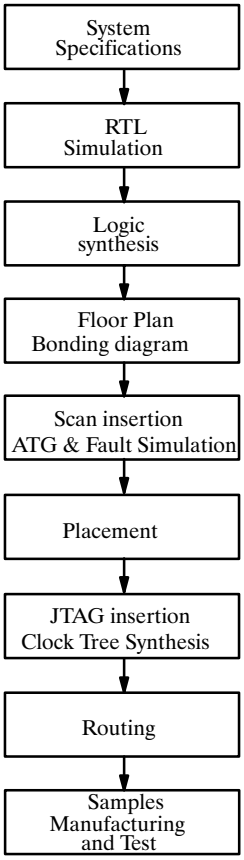
– Routing

To meet the various requirements of designers, several interface levels between the customer and Atmel Wireless & Microcontrollers are possible.

For each of the possible design modes a review meeting is required for data transfer from the user to Atmel Wireless & Microcontrollers. In all cases the final routing and verifications are performed by Atmel Wireless & Microcontrollers.

The design acceptance is formalised by a design review which authorises Atmel Wireless & Microcontrollers to proceed with sample manufacturing.

MG1 Design Flow



Design tool and design kits (DK)

The basic content of a design kit is described in the table on the right.

The interface formats to and from Atmel Wireless & Microcontrollers rely on IEEE or industry standard :

– VHDL for functional descriptions

– VHDL or EDIF for netlists

– Tabular or .CAP for simulation results

– SDF (VITAL format) and SPF for backannotation

– LEF and DEF for physical floor plan information

The design kit supported for several commercial tools is outlined in the table below.

Design Kit Support	VHDL	Gate
Cadence	*	*
Mentor	*	*
Synopsys	*	*
Compass	*	
Viewlogic	*	

Design kit Description

Design Tool or library	Atmel Software Name
Design manual & libraries	
VHDL library for blocks	
Synthesis library	
Gate level simulation library	
Design rules analyser	STAR
Power consumption analyser	COMET
Floor plan library	
Timing analyser library	
Package & bonding software	PIM
Scan path & JTAG insertion	ASIS/AJIS
ATG & fault simulation library	

Operating characteristics

Absolute Maximum Ratings

Ambient temperature under bias (TA)
Military . . . . . –55 to +125°C
Junction temperature . . . . . TJ < TA + 20°C
Storage temperature . . . . . –65 to +150°C
TTL/CMOS :

Supply voltage VDD . . . . . –0.5 V to +7 V
I/O voltage . . . . . –0.5 V to VDD + 0.5 V
Stresses above those listed may cause permanent damage to the device. Explosure to absolute maximum rating conditions for extended period may affect device reliability.

DC Characteristics

Specified at VDD = +5 V +/– 10 %

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input LOW voltage CMOS input TTL input	 0 0		 0.3VDD 0.8	 V	
VIH	Input HIGH voltage CMOS input TTL input	 0.7VDD 2.2		 VDD VDD	 V	
VOL	Output low voltage CMOS input TTL input			 0.1VDD 0.4	V	IOL = –12, 6, 3 mA*
VOH	Output high voltage CMOS input TTL input	 3.9 2.4			V	IOH = –12, 6, 3 mA*
VT+	Schmitt trigger positive threshold CMOS input TTL input		 2.6 1.7	 3.2 1.9	V	
VT–	Schmitt trigger negative threshold CMOS input TTL input	 1.3 1.1	 1.4 1.2		V	
IL	Input leakage No pull up/down Pull up Pull down	 –250	 +/–1 –50 +180	 +/–5 +450	 µA µA µA	
IOZ	3-State Output Leakage current		+/–1	+/–5	µA	
IOS	Output Short circuit current IOSN IOSP			 48 36	 mA mA	VOUT = VDD VOUT = VSS
ICCSB	Leakage current per cell		0.35	5	nA	
ISSOP	Operating current per cell		0.5		µA/MHz	

* For each of the following buffers: Bout12, Bout6, Bout3

DC Characteristics

Specified at VDD = +3 V – 10 % or 3.3 +/– 10%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input LOW voltage CMOS input TTL input	 0 0		 0.3VDD 0.8	 V	
VIH	Input HIGH voltage CMOS input TTL input	 0.7VDD 2.2		 VDD VDD	 V	
VOL	Output LOW voltage CMOS input TTL input			 0.1VDD 0.4	V	IOL = –6, 3, 1.5 mA*
VOH	Output HIGH voltage TTL input	 2.4			V	IOH = –4, 2, 1 mA*
VT+	Schmitt trigger positive threshold CMOS input TTL input		 1.8 1.3	 2.0 1.4	V	
VT–	Schmitt trigger negative threshold CMOS input TTL input	 0.9 0.9	 1.0 1.0		V	
IL	Input leakage No pull up/down Pull up Pull down	 –50 –50	 –10 20	 +/–1 +100	 µA µA µA	
IOZ	3–State Output Leakage current			+/–1	µA	
IOS	Output Short circuit current IOSN IOSP			 24 12	 mA mA	 VOUT = VDD VOUT = VSS
ISSDP	Leakage current per cell		0.1		nA	
ISSOP	Operating current per cell		0.3		µA/MHz	

* For each of the following buffers : Bout12, Bout6, Bout3

AC Characteristics

TJ = 25°C, Process typical (all values in ns)

Buffer	Description	Load	Transition	VDD	
				5V	3V
BOUT12	Output buffer with 12 mA drive	60pf	Tplh	2.72	4.72
			Tphl	2.77	4.42

Cell	Description	Load	Transition	VDD	
				5V	3V
BINCMOS	CMOS input buffer	15	Tplh	1.28	1.96
			Tphl	1.21	1.78
BINTTL	TTL input buffer	16	Tplh	1.43	2.10
			Tphl	1.58	1.75
INV	Inverter	12	Tplh	0.84	1.36
			Tphl	0.42	0.64
FDFF	D flip–flop, Clk to Q	8	Tplh	1.06	1.82
			Tphl	0.87	1.47
			Ts	0.46	1.11
			Th	0.10	0.22