Atmel is manufacturing the DMILL technology in its Nantes' factory. Primarily developed to serve the High Energy Physics market, the technology offers versatile components suitable for any advanced mixed or pure digital conception. Taking advantage of SOI use and trench insulators, the SCR structures inherently present in std CMOS technology and responsible for LATCH-UP is totally eliminated. Moreover, in association with outstanding radiation properties, product designed and fabricated with DMILL offers total security for use in highly energetic particle environments.

WIRELESS & µC

Rad Hard Mixed Signal Technology

DMILL

DMILL Process

Introduction

DMILL is a BiCMOS technology fabricated using Silicon On Insulator (SOI) substrate. The decision to develop new equipment for High Energy Physics (HEP) research has lead to the need of ultra hard technology. The detector electronics adjacent to the collision areas can accumulate radiation doses above 10Mrad. Furthermore, the low level of the detector signals imposes very high signal to noise ratios. To meet these new requirements, the French Commissariat à l'Energie Atomique (CEA), an organization highly involved in almost all advanced nuclear Physics research, has, by taking advantage of its extensive experience in SOI hardened technologies, developed the DMILL technology, a mixed analog/digital technology hardened to tolerate more than 10Mrad and 10^{14} neutrons/cm².

DMILL Performance

Active and passive devices

The DMILL process offers a designer the possibility to use 4 different active devices, i.e. NMOS, PMOS, NPN Bipolar and PJFET. With regards to advanced analog needs, several passive elements are also available, such as resistors and capacitors. For interconnect, 1 low-rho polysilicon and 2 AlSi layers can be used. Table 1 lists the electrical performance of DMILL.

Integration

For Radiation hardness reasons, DMILL uses several features, which are silicon consuming. However, trench is efficient to reduce the critical dimension, which is common in BULK CMOS technologies. Thus, the overall layout-inflating factor is limited to 30% compared to a similar 0.8µm BiCMOS technology. Today, mixed complex designs have achieved 1Million transistors/cm².

Speed

Thanks to SOI, parasitic capacitors are reduced. Therefore, the intrinsic speed of the devices is increased compared to similar BULK technology:

- - Propagation delay = 150pS @ ambient temperature (180pS @ 150°C) (1)
- - Bipolar Ft = 5.0GHz at ambient temperature

1. inverter made of NMOS (4.0x0.8) and PMOS (8.0/0.8)

Rev. B – 24-Aug-01

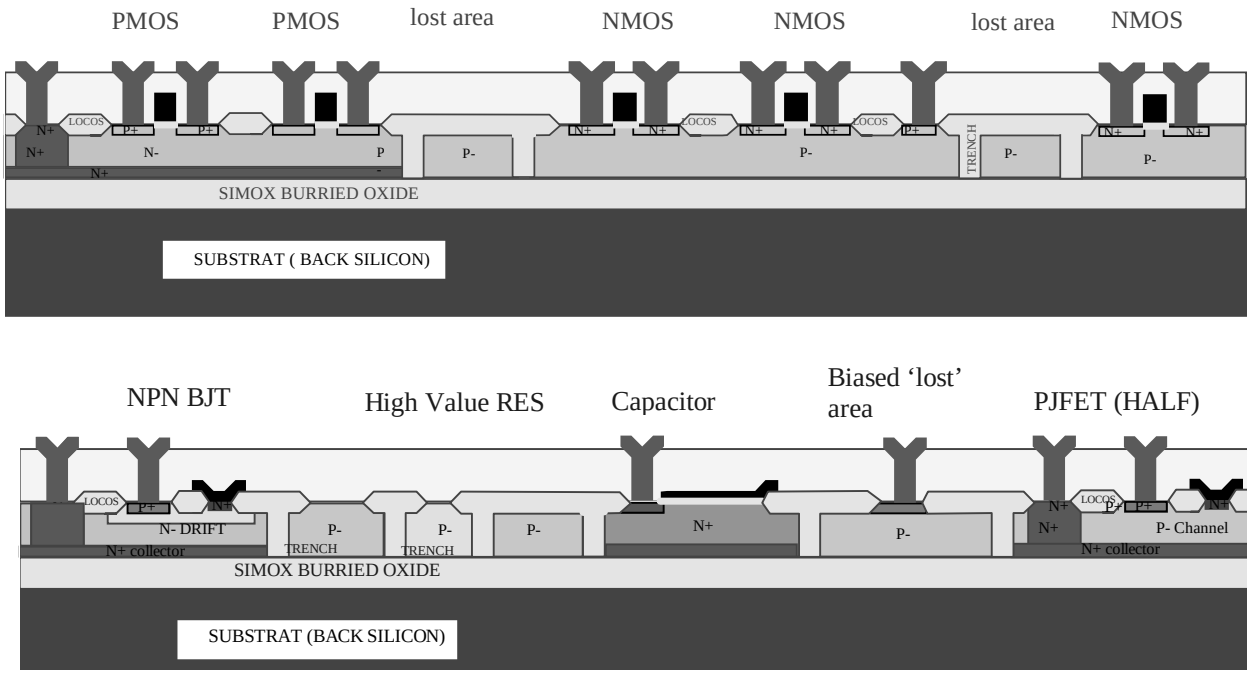
Table 1. DMILL basic parameters

Parameter	Typ value	Unit	Description
MOS transistors			
Leff N	0.72	µm	Electrical length of a 0.8µm N channel transistor
Leff P	0.70	µm	Electrical length of a 0.8µm N channel transistor
VTN	0.93	V	Threshold voltage of a 0.8µm N channel transistor
VTP	-0.80	V	Threshold voltage of a 0.8µm P channel transistor
IDSN (0.8µm)	8.30	mA	Drain current for a 25/0.8µm N transistor with VGS=VDS=5.0V
IDSP (0.8µm)	4.60	mA	Drain current for a 25/0.8µm P transistor with VGS=VDS=-5.0V
BVDSS (1µA)	>8.00	V	Drain / Source breakdown voltage at ID = 1.0µA
VTN Field	>10.0	V	
VTP Field	>10.0	V	
NPN bipolar			
Beta (1.2x1.2)	250	NU	NPN 1.2x1.2 ideal forward beta
V_{EARLY}	96	V	NPN Forward early voltage
BVCE0	5.70	V	Breakdown of collector/emitter with base open
BVCB0	17.0	V	Breakdown of collector/base with emitter open
P-JFET			
VPPJ (1.2µm)	1.20	V	Pinch-off voltage of a 100/1.2 P-JFET
GDPJ (1.2µm)	1.135	µS/µm	Drain transconducatnce of a 100/1.2 PJFET (VGS=0V; VDS=-3V)
Oxides			
E_{ox}	17.5	nm	Gate oxide thickness
E_{Field}	470	nm	Gate oxide thickness
E_{capa}	42.0	nm	Gate oxide thickness
Resistors			
R_{P+}	118	Ω/square	P+ resistivity
R_{P-}	3550	Ω/square	P- resistivity
$R_{extrins}$	1650	Ω/square	Extrinsic base resistivity
R_{POL}	2.35	Ω/square	Poly gate resistivity
R_{M1}	0.050	Ω/square	Metal 1 resistivity
R_{M2}	0.040	Ω/square	Metal2 resistivity

Cross sections

Technology cross-section in Figure 1 gives an indication of how the devices are built on top of the insulator layer of the SOI substrate.

Figure 1. DMILL Technology Cross Section



No Latch-Up

The use of combined SOI substrate and lateral isolation by trench removes the usual three-dimensional SRC parasitic structure inherent to CMOS/Bulk technologies. Thus, no Latch-up can be triggered, either by electrical injection or prompt charges deposited by heavy particles during their travel across silicon.

Radiation properties

The proximity of the electronics from the area the protons collide in HEP experiments makes the radiation requirements extremely high. Some of the circuits will suffer from 30Mrad combined with a fluence of 6.0E14 neutrons/cm² after 10 years lifetime! Therefore, particular attention is paid to make all devices radiation hard. Characterizations are conducted using various ionizing particles because of HEP bombarding cocktails. Of particular interest, X and Gamma rays as well as proton and neutron. Cumulated doses up to 30Mrad are regularly deposited to measure post radiation parameter's variation. Hardness demonstration up to 350Mrad was done with a 16bit sliced µprocessor. The following figures give some indication on the repeatability of the radiation hardness of the DMILL process. Notice that Radiation induced drifts are continuously verified and Statistical Process Control is in force, as for any other technological parameter (thickness, electrical, dimension…).

Figure 2. NMOS transistor thrshold voltage with dose over production

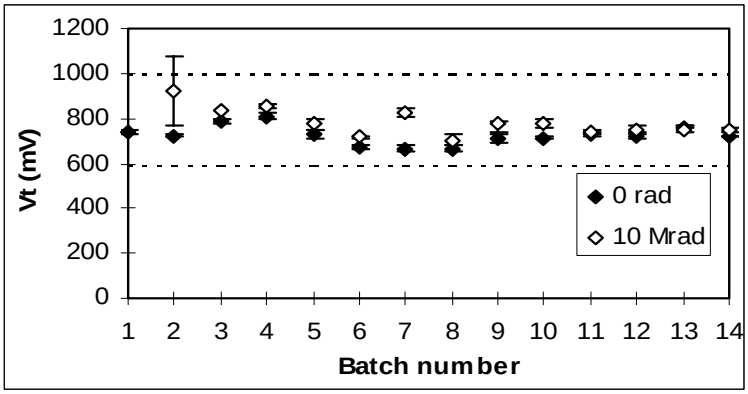


Figure 3. PMOS transistor thrshold voltage with dose over production

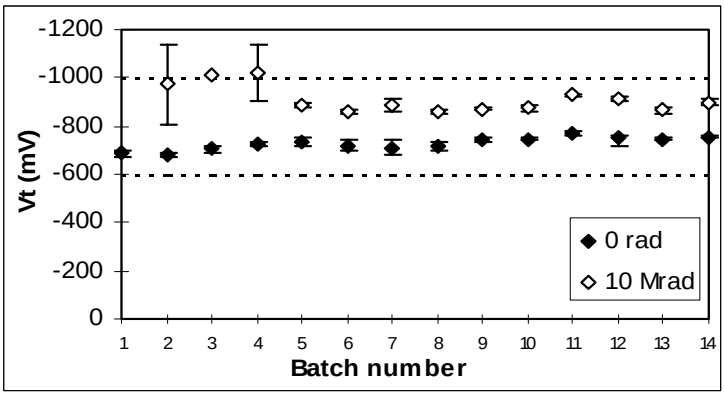


Figure 4. NPN gain versus batch numberft

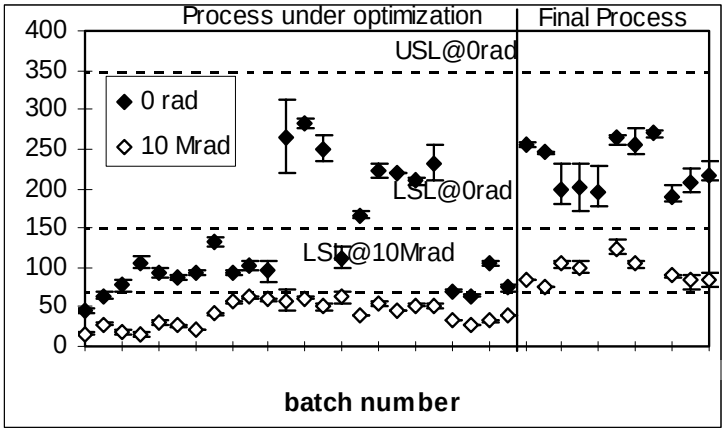


Figure 5. NPN gain versus 1MeV equivalent neutron fluence

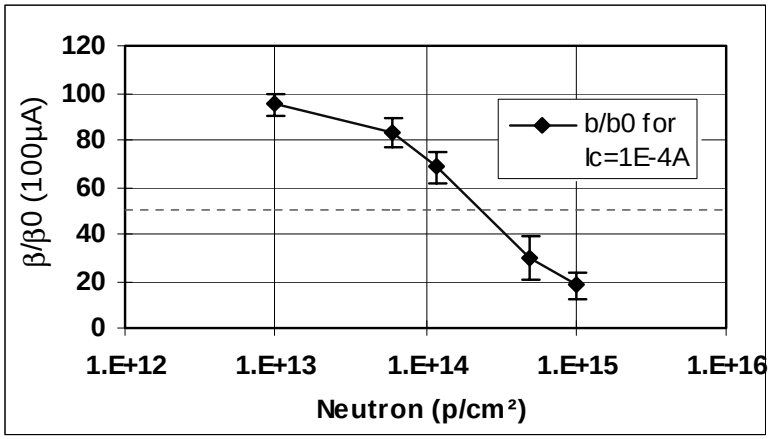
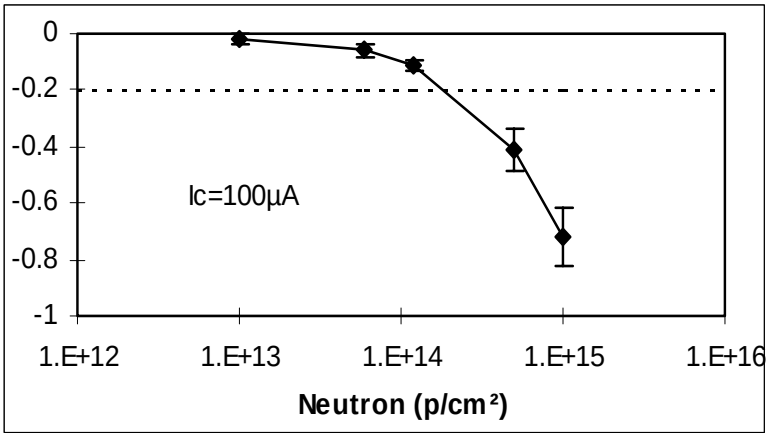


Figure 6. PJFET ΔVp versus 1MeV equivalent neutron fluence



Post 10Mrad parameter drifts

To allow designer to assess design robustness, Atmel offers, in the design kit, a set of 10Mrad post irradiation drifts. Therefore, sensitive parameters drift is injected in the simulation. It is recommended to use these numbers in combination with typical technology parameters to avoid over-pessimistic simulation.

Since no significant degradation is observed before 1Mrad accumulated dose, most of the space design will not require any post-rad simulation.

Radiation Hardness Assurance

In order to verify the process stability over the production period, Atmel has installed a Radiation Hardness Assurance (RHA) program. Each and every DMILL production run is irradiated up to 10Mrad with 10keV X-rays. This is a non-destructive test performed at wafer level on process control monitors located in the street line (scribe lines) of the wafers. Irradiation is collimated so that customer's circuits are not damaged. Wafers are delivered with a Radiation Certificate of Conformance (CoC) to post radiation specifications that are scheduled in the Electrical Design Rules. The possibility exists to remove this control when not necessary.

SEU characteristics

Single Event Upset is a temporary event that can occur in storing elements by highly energetic particles crossing over the silicon layer. If the quantity of charges deposited by this particle is higher than the stored charge, then, the information contained in the storing element is corrupted. This error is not permanent and can be restored.

DMILL is intrinsically hardened against SEU because the silicon layer on top of the insulator is very thin (1.2µm). So, deposited charge is very small. Thus, compared to standard Bulk CMOS technology, DMILL offers improved SEU figures:

Storing element	SEU threshold (MeV/(mg/cm²))	Reduction factor (*)
Memory Cell	15	200
DFF cell	70	130
Combinatorial	70	40

Note: (*) By comparison to standard BULK CMOS technology with similar lithography.

Most importantly for this mixed analog/digital application, Atmel offers SEU hardened cells (DFFs, SRAM) by use of additional logic. Demonstration of the applicability of this technique to various technologies has been done by irradiating cells up to 115 MeV/(mg/cm2) without any SEU detection.

SEU must be evaluated on a case-by-case basis. From a digital standpoint, the process provides for latchup-free operation up to the specified radiation limits. If Customer requires performance beyond the radiation parameters, either in Total Dose, or in flux, a fault-tolerant design approach can be adopted.

From an analog standpoint, SEU is a more complex issue. SEU depends on a number of variables such as the amount and duration of transients on signal lines, charge stored on (or dissipated from) capacitors, etc. Essentially, this becomes a tradeoff issue where, for instance, capacitors can be made larger so that SEU's have a proportionally smaller effect. Similar tradeoffs exist in almost every type of analog circuit.

Noise Characteristics

DMILL devices have particularly low noise properties. This is illustrated in the figures below. Even after 10Mrad accumulated dose, noise figures remain lower than a few nV/√Hz. This property is of very high importance for analog designers dealing with low input signals as well as harsh environments.

In addition, substrate partitioning is possible with DMILL technology. The use of a lateral trench is a way to reduce noise and parasitic coupling between analog and digital portions of a mixed design. A specific “User’s Guide” (RDER2402) is available to give designers techniques to reduce spurious effects and to take into account parasitic elements in complex designs.

Figure 7. Noise properties of NMOS transistors up to 10 Mrad

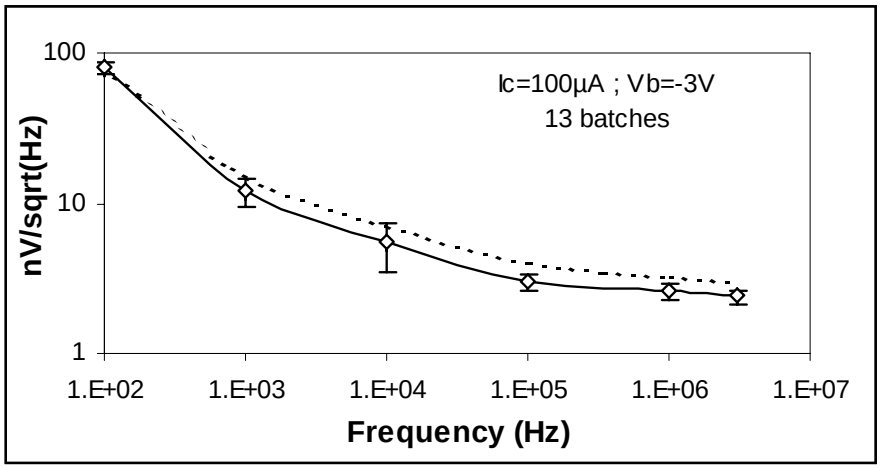


Figure 8. Noise properties of PMOS transistors up to 10 Mrad

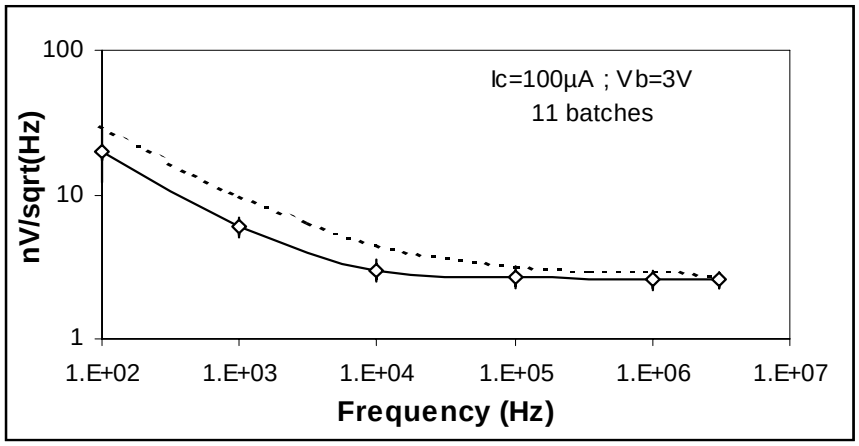


Figure 9. Noise properties of PJFET transistors up to 10 Mrad

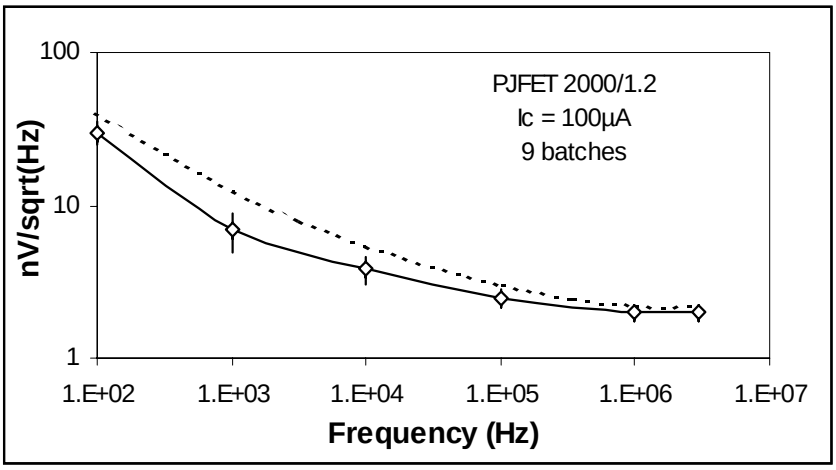
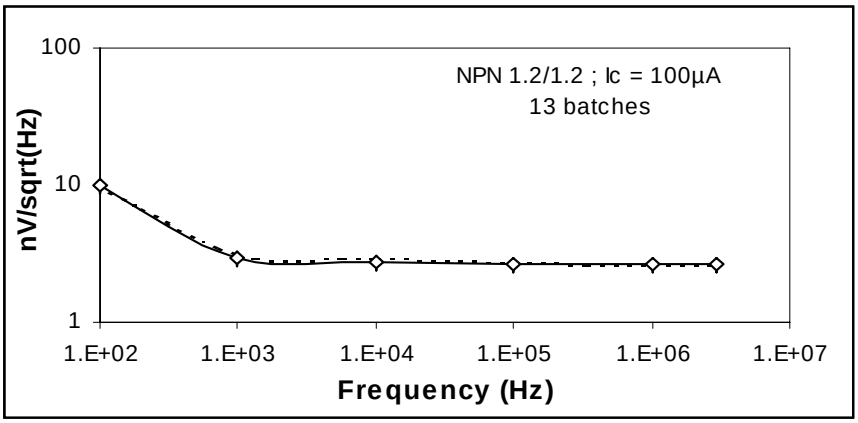


Figure 10. Noise properties of NPN transistors up to 10 Mrad



Development Tools

Atmel offers, for free, a DMILL design kit. This set of tools allows the designer to develop advanced and highly integrated circuits for mixed analog/digital applications. The design kit, which is being distributed to Customer under the signed Non Disclosure Agreement (NDA), is comprised of several files and paper documents that are included in the Cadence 9502 environment. Part of the content is described in 18.4.1.

List of specifications and files

Topological design rules (RDTR2401)

- Design rules for layout
- Specific rules for ESD protection
- Mask generation for drawn layers

Electrical design rules (RDER2401)

- Electrical parameters (resistance, capacitance, currents, etc.)
- Electrical models for simulation including –55 to +150°C and 250°C
- MOS transistors: BSIM3v3 for ELDO
- NPN Bipolar: Gummel & Poon
- PJFET: Spice
- Corner files (typN / typP; fastN / fastP; slowN / slowP; slowN / fastP; fastN / slowP)
- Reliability characteristics (Electromigration, Hot Carrier Injection, etc.)
- DMILL specific characteristics (noise, radiation, etc.)

SOI/DMILL design users guide (RDER2402)

Included is a set of design rules and techniques to get a first pass yield design with particular focus on parasitic and cross talk effects.

Cadence library (v9502)

The Cadence library is composed of several files including:

DDK	Cadence library root directory
DDK.lib	Cadence library file
DDK.drc	DMILL technology Cadence file DRC format
Parameters	ELDO BSIM3v3 parameters for DMILL in Cadence format
Basic	Framework independent basic DMILL information

ESD Protection

DMILL design kit offers several types of ESD protection depending on I/O structure:

Type	Description / test
Digital Input Protection	Diode & resistor / Specific Poly-contact spacing / > 4000V
Analog Input Protection	Grounded gate NMOS transistors / Specific Poly-contact spacing / > 4000V
Output Buffer	NMOS & PMOS / Specific Poly-contact spacing / > 4000V
Power Supply protection	Grounded gate NMOS transistors / Specific Poly-contact spacing / > 4000V

ASSEMBLY rules

Bonding Pads are defined and verified by DRC. However, specific rules can be adapted for modern assembly techniques.

Scribe lines are defined according to Atmel HIgh RELiability rules. No waiver is accepted since Process Control Monitors must be inserted in those lines.

Digital library

In the frame of one CERN funding, a digital std-cell library for automatic place and route has been developed. The content of the library is listed in Table 2. VERILOG and SYNOPSYS libraries are provided.

Table 2. Digital Library

Cell function	Symbol
Inverter	Jiv1
Power inverter (double drive)	Jiv2
Power inverter (triple drive)	Jiv3
Power inverter (four-time drive)	Jiv4
2-Input AND	Jan2
3-Input AND	Jan3
2-Input NAND	Jnd2
3-Input NAND	Jnd3
4-Input NAND	Jnd4
6-Input NAND	Jnd6
8-Input NAND	Jnd8
2-Input OR	Jor2
3-Input OR	Jor3
2-Input NOR	Jnr2
3-Input NOR	Jnr3
4-Input NOR	Jnr4
2- Input exclusive OR	Jxo2
2- Input exclusive NOR	Jxn2
2 x 2 input AND into 2 input NOR	Jaoi1
2 input AND into 3 input NOR	Jaoi2
2 input OR into 3 input NAND	Joai1
2 x 2 input OR into 2 input NAND	Joai2
Fulladder	Jfuadd
2 to 1 multiplexer	Jmx2
4 to 1 multiplexer	Jmx4
8 to 1 multiplexer	Jmx8
1 to 2 decoder with active low enable	Jdec2e
2 to 4 decoder with active low enable	Jdec4e
Tristate buffer	Jtbuf
Non inverting buffer	Jbuf
D latch with active low reset	Jldrl

Cell function	Symbol
D latch with active high set	Jldsh
D Flip-Flop	Jfd
Scan D Flip-Flop	Jfd1s
D Flip-Flop with active high reset	Jfdrh
D Flip-Flop with active low set	Jfdsl
D Flip-Flop with active low set & active high reset	Jfdslrh
JK Flip-Flop with active high reset	Jfjkrh
JK Flip-Flop with active low set	Jfjksl
Schmitt trigger	Jbis1
TTL input	Jbit1
TTL input with pull-up resistor	Jbit2
CMOS input	Jbic1
CMOS input with pull-up resistor	Jbic2
CMOS input with pull-down resistor	Jbic3
TTL output	Jbot1
CMOS output	Jboc1
Open drain with pull-up resistor	Jbo2
Open drain with pull-down resistor	Jbo3
Tri-state output	Jbto1
Bidirection: Tri-state out + Schmitt trigger in	Jbtbs1
Bidirection: Tri-state out + Schmitt trigger In + pull-up	Jbtbs2
Bidirection: Tri-state out + TTL in	Jbtb1
Bidirection: Tri-state out + TTL in + pull-up	Jbtb2
Bidirection: Tri-state out + CMOS in	Jbcb1
Analog signal pad with ESD	Jbia1
Analog signal pad	Jboa1
Digital VDD pad	Jpdd1
Analog VDD pad	Jpdda1
Digital VSS pad	Jpss1
Analog VSS pad	Jpssa1

Analog library

To answer immediate needs, Atmel gives access to a limited set of analog cells. 9 cells are available and described in the Table 3.

Table 3. Analog library

Cell function	Symbol
Trimable Band-gap Voltage Reference	BGP01
Band-Gap Voltage Reference	BGP02
40nA Current generator	IG01
50µA Current Generator	IG02
Low Power, Low Voltage High DC Gain Operational Amplifier	OPA01
High DC Gain Folded Cascade Operational Amplifier	OPA02
CMOS Operational Amplifier with class AB output stage	OPA03
Low Noise Charge preamplifier	PRE01

Note: This list is not exhaustive.

Program Management

Atmel will designate a program manager, with necessary authority for planning and management of financial resources. A program manager will provide Customer with one overall schedule. The schedule will be maintained throughout the life of the contract. Monthly reports, teleconferences, or other reports will be generated as mutually agreed. Any particular event will be immediately reported to Customer when a schedule is affected.

Prototyping

Mixed analog/digital development often requires prototyping for function or architecture validation. It is also accepted that analog debug requires several loops to refine design. The prototyping phase allows assessing yield figures before larger scale production. Considering the high Non Recurrent Expenses (NRE) necessary to access ASIC prototyping, Atmel is offering the Multi-Project Wafer (MPW) service. The objective of this approach is to group circuits from different customers together on one single reticule. Thus, sets of masks and numbers of wafers are minimized.

MPW organization

The MPW service is organized for DMILL either at Atmel or through IMEC, a Belgium company in the frame of the Europractice projects context. Starting 4 times a year, MPW runs collect DMILL designs. Under Atmel responsibility, IMEC will receive tape or FTP files. Then, DRC verification will be done on the net-lists and reticule physical placement will be done prior to sending the GDSII tape to Atmel for further mask manufacturing and wafer processing. The lead-time is generally 14 weeks from submission date to die delivery. In addition to pure foundry, additional test and assembly services are possible. More information can be gathered at:

www.imec.be/europractice/

More wafer runs can also be organized when requested.

Debug / extended characterization

In case the design of the chip is sub-contracted, the design house can handle several design validation and prototype evaluation. First silicon will be used to verify and characterize the basic functionality as well as electrical performances. Extended verifications

can also be conducted over the Military (-55°C; +125°C) temperature and power supply ranges. A detailed report will be furnished to Customer with available functional and performance margins.

When necessary, specific radiation tests such as heavy ion induced Single Event Upset (SEU) sensitivity will be tested on several parts according to the existing standards.

When a non-qualified assembly technique or package is used, extended thermal and mechanical characterization can be performed to give Customer proof of suitable quality and reliability.

Price and delivery for prototyping

Basic MPW offer:

- Fixed price of $800 per mm².
- Minimum dimension of 10mm²
- No maximum dimension but maximal edge dimension will be limited to 10mm
- 20 prototypes (non-tested or packaged) will be sent to the customer
- Quality level is Engineering thus Atmel in-house specifications are in force

Several options are possible and must be clearly identified in the Purchase order, based on prior negotiation with Atmel:

- Maximum quantity up to 500 parts
- Inspection level can be done according to the MIL-std 883, tm 2010 cond.B.
- Parts can be packaged in either hermetic or plastic
- Wafer can be sent to any subcontractor for any modern assembly technique
- Wafer can be tested provided positive answer to prior test feasibility study is given
- etc…

Large scale production

If the MPW approach is not acceptable (confidentiality, quantity, etc.), dedicated runs can be ordered directly with Atmel. The netlist is transferred to the Atmel design center for DRC verification. A GDSII tape is made available for mask generation. The Quantity of wafers necessary to deliver the requested quantity of final products is calculated taking into account manufacturing, test, visual inspection and assembly yields. DMILL maximum production is 150 wafers per week.

DMILL production

Different possibilities exist to produce DMILL circuits:

- Pure foundry: Wafers are manufactured according to in-house procedures and delivered with a CoC.
- Tested wafers: Provided a test program is validated, Atmel can either test or sub-contract test of the wafers to sort Good dice.
- Tested dice: Probed wafers are diced to extract and deliver only good dice.
- Packaged dice: Provided bonding diagram and prior feasibility study is concluded positively, Atmel can make or can sub-contract assembly of good die to a quality grade selected by Customer.
- Screened parts: Atmel can conduct or subcontract part screening from commercial up to highest quality level required for space applications.
- Any combination of the above possibilities

Test

The test program is developed according to the requirements of the Source Control Drawing (customer specification). Prototypes coming from previous MPW runs are used to debug both test program and hardware. The final test program will use the frame developed during the prototyping phase with a possible extension according to the final specification. A review of the test program content will be done with Customer representatives prior to production release.

Customer Source Inspection

Customer may require a Customer Source Inspection (CSI) at any step of the fabrication. Notification to Customer representative will be made at least 15 days prior to the CSI.

Design background

Atmel customers widely use the DMILL technology for various final applications. Today, more than 20cm² of different designs have been fabricated for High Energy Physics and Nuclear Industry applications. The application breakdown is roughly 70% HEP, 15% nuclear and 15% misc.

Examples of DMILL designs

1. Advanced Synthesizer Local oscillator: It realizes a PLL Frequency synthesizer based on fractional division, including spurious cancellation technique (Sigma-Delta). RF input frequency up to 400MHz.
2. Low noise charge Preamplifier with DC coupling for Large Hadron Collider Experiment
3. Mixed-signal data receiver/clock synchronizer ASIC for analog front end
4. Analog readout for position sensitive radiation detectors
5. Four-channel rad-hard delay generator with 1ns minimum time step
6. 80MHz clock and data recovery circuit
7. Analog signal processor for a calorimeter with a multi-gain preamplifier
8. Sample and hold multiplexer
9. Clock and Digital logic for front end rad-hard electronics
10. Analog memory
11. 12-bit, 5 MHz ADC
12. 4-channel tri-gain shaper
13. 128 channel analog pipeline for MSGC detectors
14. 128 channel preamplifier, shaper, and buffer
15. Analog pulse shape processor
16. 128 x 1 multiplexer
17. Bias generator/pulse generator
18. 128 channel binary readout
19. Bipolar front end preamplifier and comparator
20. Dynamic FIFO
21. De-randomizer and data compressor
22. Charge sensitive preamplifier and shaper
23. 12-bit 40 MHz ADC
24. Satellite thermal controller/multiplexer
25. Bus driver for satellite on-board systems
26. Sun sensor system using Silicon photodiodes
27. Front-end for astrophysics experiment
28. Angular coder for nuclear industry (10Mrad)
29. Nuclear robotics component

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