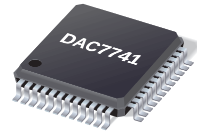


SBAS248A – DECEMBER 2001 – REVISED JULY 2003

16-Bit, Single Channel DIGITAL-TO-ANALOG CONVERTER With Internal Reference and Parallel Interface

FEATURES

- LOW POWER: 150mW MAXIMUM
- +10V INTERNAL REFERENCE
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 5μs to ±0.003% FSR
- 16-BIT MONOTONICITY, –40°C TO +85°C
- ±10V, ±5V OR +10V CONFIGURABLE VOLTAGE OUTPUT
- RESET TO MIN-SCALE OR MID-SCALE
- DOUBLE-BUFFERED DATA INPUT
- INPUT REGISTER DATA READBACK
- SMALL LQFP-48 PACKAGE

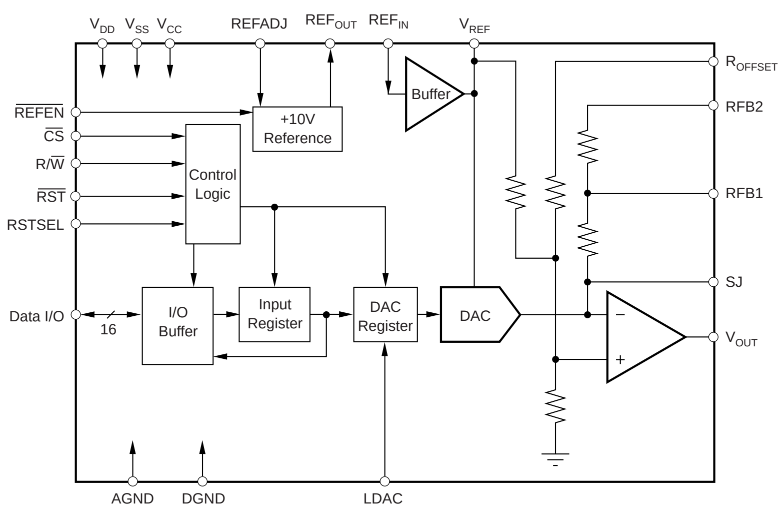
APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS
- CLOSED-LOOP SERVO CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The DAC7741 is a 16-bit Digital-to-Analog Converter (DAC) which provides 16 bits of monotonic performance over the specified operating temperature range and offers a +10V, low-drift internal reference. Designed for automatic test equipment and industrial process control applications, the DAC7741 output swing can be configured in a ±10V, ±5V, or +10V range. The flexibility of the output configuration allows the DAC7741 to provide both unipolar and bipolar operation by pin strapping. The DAC7741 includes a high-speed output amplifier with a maximum settling time of 5μs to ±0.003% FSR for a 20V full-scale change and only consumes 100mW (typical) of power.

The DAC7741 features a standard 16-bit parallel interface with double buffering to allow asynchronous updates of the analog output and data read-back to support data integrity verification prior to an update. A user-programmable reset control allows the DAC output to reset to min-scale (0000_H) or mid-scale (8000_H) overriding the DAC register values. The DAC7741 is available in a LQFP-48 package and four performance grades specified to operate from 0°C to +70°C and –40°C to +85°C.



ABSOLUTE MAXIMUM RATINGS(1)

V_{CC} to V_{SS}	–0.3V to +34V
V_{CC} to AGND	–0.3V to +17V
V_{SS} to AGND	–17V to +0.3V
AGND to DGND	–0.3V to +0.3V
REF_{IN} to AGND	–9V to +11V
V_{DD} to DGND	0V to V_{CC} – 1.4V
Digital Input Voltage to DGND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to DGND	–0.3V to V_{DD} + 0.3V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	LINEARITY ERROR (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
DAC7741Y	±6	±4	LQFP-48	PT	–40°C to +85°C	DAC7741Y/250	DAC7741Y	Tape and Reel, 250
"	"	"	"	"	"	DAC7741Y/2K	"	Tape and Reel, 2000
DAC7741YB	±4	±2	LQFP-48	PT	–40°C to +85°C	DAC7741YB/250	DAC7741YB	Tape and Reel, 250
"	"	"	"	"	"	DAC7741YB/2K	"	Tape and Reel, 2000
DAC7741YC	±3	±1	LQFP-48	PT	–40°C to +85°C	DAC7741YC/250	DAC7741YC	Tape and Reel, 250
"	"	"	"	"	"	DAC7741YC/2K	"	Tape and Reel, 2000
DAC7741YL	±2	±1	LQFP-48	PT	0°C to +70°C	DAC7741YL/250	DAC7741YL	Tape and Reel, 250
"	"	"	"	"	"	DAC7741YL/2K	"	Tape and Reel, 2000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15V, V_{SS} = –15V, V_{DD} = +5V, internal reference enabled, unless otherwise noted.

		DAC7741Y			DAC7741YB			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ACCURACY								
Linearity Error (INL)				±6			±4	LSB
	T_A = 25°C			±5			±3	LSB
Differential Linearity Error (DNL)				±4			±2	LSB
Monotonicity		14			15			Bits
Offset Error				±0.1			*	% of FSR
Offset Error Drift			±2			*		ppm/°C
Gain Error	With Internal REF			±0.4			±0.25	% of FSR
	With External REF			±0.25			±0.1	% of FSR
Gain Error Drift	With Internal REF		±15			±10		ppm/°C
PSRR (V_{CC} or V_{SS})	At Full-Scale		50	200		*	*	ppm/V
ANALOG OUTPUT(1)								
Voltage Output(2)	+11.4/–4.75(1)		0 to 10			*		V
	+11.4/–11.4(1)		±10			*		V
	+11.4/–6.4(1)		±5			*		V
Output Current		±5			*			mA
Output Impedance			0.1			*		Ω
Maximum Load Capacitance			200			*		pF
Short-Circuit Current			±15			*		mA
Short-Circuit Duration	AGND		Indefinite			*		
REFERENCE								
Reference Output		9.96	10	10.04	9.975	*	10.025	V
REF_{OUT} Impedance			400			*		Ω
REF_{OUT} Voltage Drift			±15			±10		ppm/°C
REF_{OUT} Voltage Adjustment(3)		±25			*			mV
REF_{IN} Input Range(4)		4.75		V_{CC} – 1.4	*		*	V
REF_{IN} Input Current			10			*		nA
REFADJ Input Range	Absolute Max Value that can be applied is V_{CC}	0		10	*		*	V
REFADJ Input Impedance			50			*		kΩ
V_{REF} Output Current		–2		+2	*		*	mA
V_{REF} Impedance			1			*		Ω

ELECTRICAL CHARACTERISTICS (Cont.)

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15V, V_{SS} = –15V, V_{DD} = +5V, internal reference enabled, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7741Y MIN	DAC7741Y TYP	DAC7741Y MAX	DAC7741YB MIN	DAC7741YB TYP	DAC7741YB MAX	UNITS
DYNAMIC PERFORMANCE								
Settling Time to ±0.003%	20V Output Step R_L = 5kΩ, C_L = 200pF, with external REF_{OUT} to REF_{IN} filter(5)		3	5		*	*	µs
Digital Feedthrough			2			*		nV-s
Output Noise Voltage	at 10kHz		100			*		nV/√Hz
DIGITAL INPUT								
V_{IH}	$\lvert I_H \rvert < 10\mu A$	0.7 • V_{DD}			*			V
V_{IL}	$\lvert I_L \rvert < 10\mu A$			0.3 • V_{DD}			*	V
DIGITAL OUTPUT								
V_{OH}	I_{OH} = –0.8mA	3.6			*			V
V_{OL}	I_{OL} = 1.6mA			0.4			*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+11.4		+15.75	*		*	V
V_{SS}	Bipolar Operation	–15.75		–11.4	*		*	V
	Unipolar Operation	–15.75		–4.75	*		*	V
I_{DD}			100			*		µA
I_{CC}	Unloaded		4	6		*	*	mA
I_{SS}	Unloaded	–4	–2.5		*	*		mA
Power	No Load, Ext. Reference		85			*		mW
	No Load, Int. Reference		100	150		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Specifications same as grade to the left.

NOTES: (1) With minimum V_{CC}/V_{SS} requirements, internal reference enabled.
(2) Please refer to the “Theory of Operation” section for more information with respect to output voltage configurations.
(3) See Figure 7 for gain and offset adjustment connection diagrams when using the internal reference.
(4) The minimum value for REF_{IN} must be equal to the greater of V_{SS} +14V and +4.75V, where +4.75V is the minimum voltage allowed.
(5) Reference low-pass filter values: 100kΩ, 1.0µF (See Figure 10).

ELECTRICAL CHARACTERISTICS

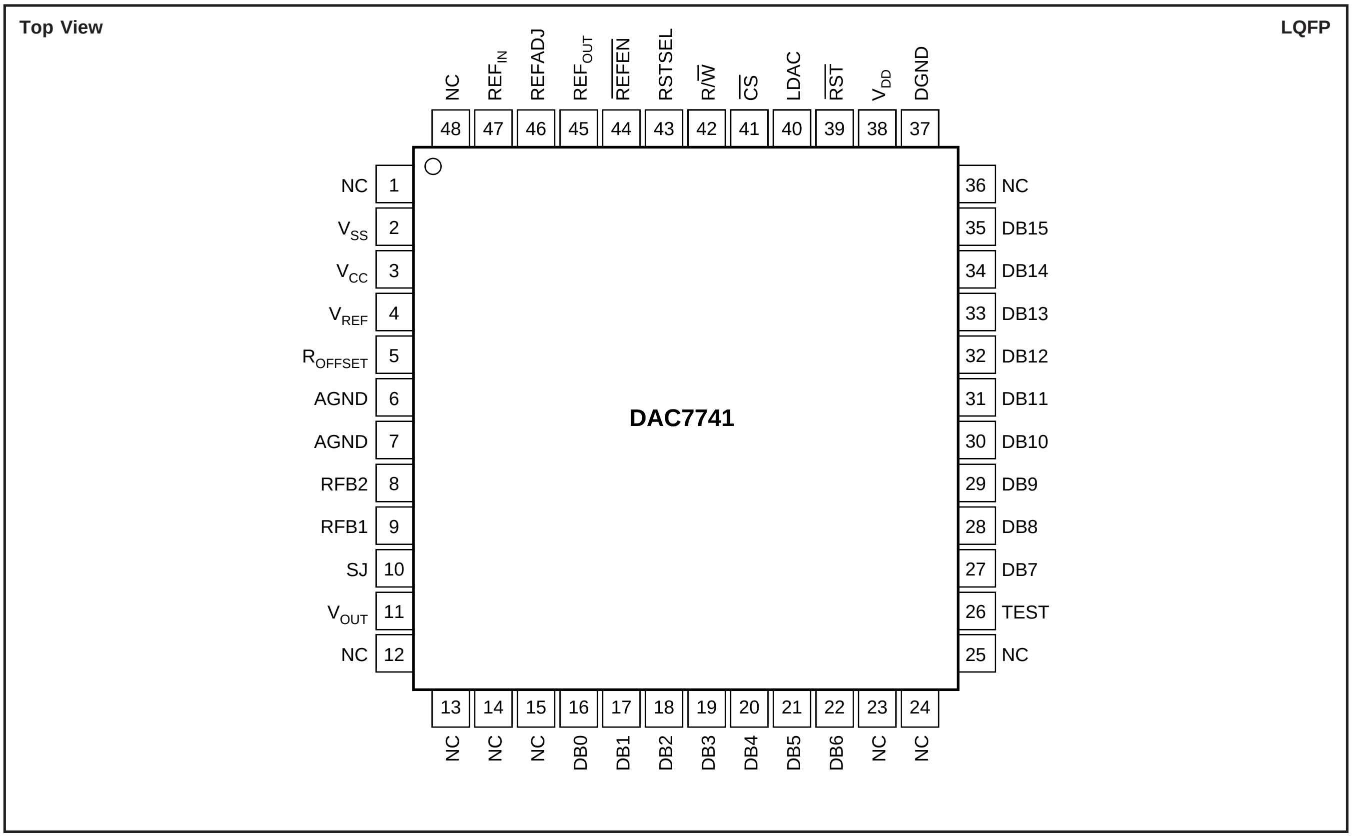
All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15V, V_{SS} = –15V, V_{DD} = +5V, internal reference enabled, unless otherwise noted.

		DAC7741YL			DAC7741YC			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ACCURACY								
Linearity Error (INL)				±2			±3	LSB
	T_A = 25°C		±1				±2	LSB
Differential Linearity Error (DNL)				±1			±1	LSB
Monotonicity		16			16			Bits
Offset Error				±0.1			*	% of FSR
Offset Error Drift			±2			*		ppm/°C
Gain Error	With Internal REF			±0.4			±0.2	% of FSR
	With External REF			±0.25			±0.1	% of FSR
Gain Error Drift	With Internal REF		±15			±7		ppm/°C
PSRR (V_{CC} or V_{SS})	At Full-Scale		50	200		*	*	ppm/V
ANALOG OUTPUT(1)								
Voltage Output(2)	+11.4/–4.75(1)		0 to 10			*		V
	+11.4/–11.4(1)		±10			*		V
	+11.4/–6.4(1)		±5			*		V
Output Current		±5			*			mA
Output Impedance			0.1			*		Ω
Maximum Load Capacitance			200			*		pF
Short-Circuit Current			±15			*		mA
Short-Circuit Duration	AGND		Indefinite			*		
REFERENCE								
Reference Output		9.96	10	10.04	9.975	*	10.025	V
REF_{OUT} Impedance			400			*		Ω
REF_{OUT} Voltage Drift			±15			±7		ppm/°C
REF_{OUT} Voltage Adjustment(3)		±25			*			mV
REF_{IN} Input Range(4)		4.75		V_{CC} – 1.4	*		*	V
REF_{IN} Input Current			10			*		nA
REFADJ Input Range	Absolute Max Value that can be applied is V_{CC}	0		10	*		*	V
REFADJ Input Impedance			50			*		kΩ
V_{REF} Output Current		–2		+2	*		*	mA
V_{REF} Impedance			1			*		Ω
DYNAMIC PERFORMANCE								
Settling Time to ±0.003%	20V Output Step R_L = 5kΩ, C_L = 200pF, with external REF_{OUT} to REF_{IN} filter(5)		3	5		*	*	µs
Digital Feedthrough			2			*		nV-s
Output Noise Voltage	at 10kHz		100			*		nV/√Hz
DIGITAL INPUT								
V_{IH}	$\lvert I_H \rvert < 10\mu A$	0.7 • V_{DD}			*			V
V_{IL}	$\lvert I_L \rvert < 10\mu A$			0.3 • V_{DD}			*	V
DIGITAL OUTPUT								
V_{OH}	I_{OH} = –0.8mA	3.6			*			V
V_{OL}	I_{OL} = 1.6mA			0.4			*	V
POWER SUPPLY								
V_{DD}		+4.00	+5.0	+5.25	+4.75	*	*	V
V_{CC}		+11.4		+15.75	*		*	V
V_{SS}	Bipolar Operation	–15.75		–11.4	*		*	V
	Unipolar Operation	–15.75		–4.75	*		*	V
I_{DD}			100			*		µA
I_{CC}	Unloaded		4	6		*	*	mA
I_{SS}	Unloaded	–4	–2.5		*	*		mA
Power	No Load, Ext. Reference		85			*		mW
	No Load, Int. Reference		100	150		*	*	mW
TEMPERATURE RANGE								
Specified Performance		0		70	–40		+85	°C

* Specifications same as grade to the left.

NOTES: (1) With minimum V_{CC} / V_{SS} requirements, internal reference enabled.
(2) Please refer to the "Theory of Operation" section for more information with respect to output voltage configurations.
(3) See Figure 7 for gain and offset adjustment connection diagrams when using the internal reference.
(4) The minimum value for REF_{IN} must be equal to the greater of V_{SS} +14V and +4.75V, where +4.75V is the minimum voltage allowed.
(5) Reference low-pass filter values: 100kΩ, 1.0µF (See Figure 10).

PIN CONFIGURATION



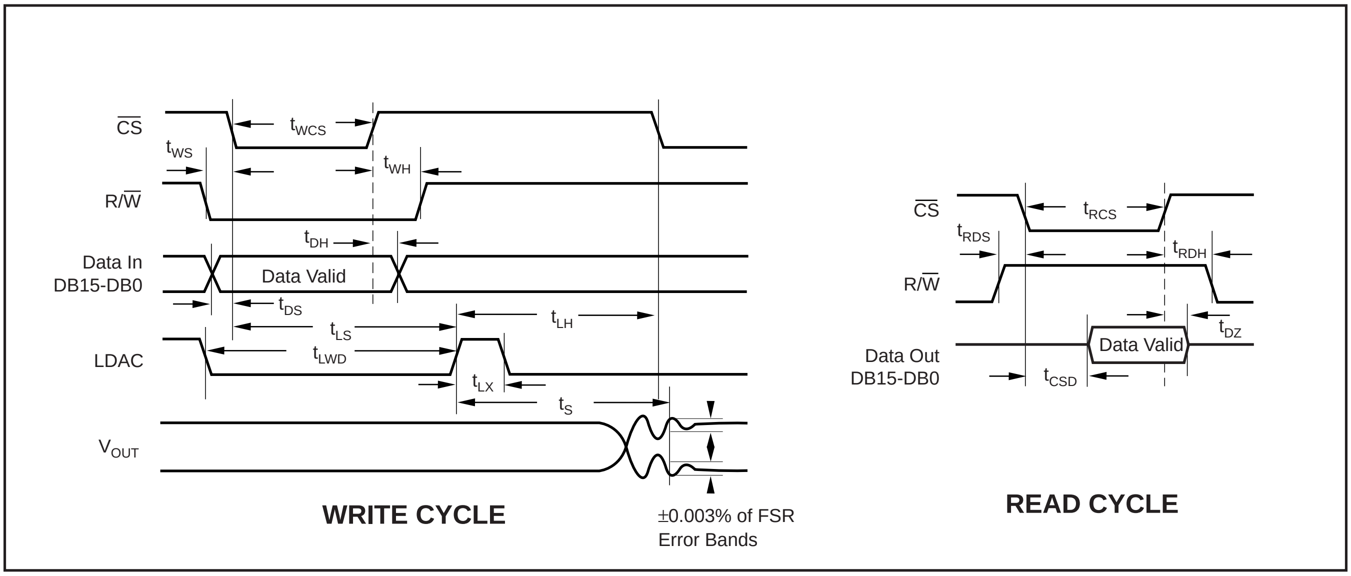
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	NC	No Connection
2	V_{SS}	Negative Analog Power Supply.
3	V_{CC}	Positive Analog Power Supply.
4	V_{REF}	Buffered Output from REF_{IN}, can be used to drive external devices. Internally, this pin directly drives the DAC circuitry.
5	R_{OFFSET}	Offsetting Resistor
6	AGND	Analog ground (Must be tied to analog ground)
7	AGND	Analog ground (Must be tied to analog ground)
8	RFB2	Feedback Resistor 2, used to configure DAC output range.
9	RFB1	Feedback Resistor 1, used to configure DAC output range.
10	SJ	Summing Junction of the Output Amplifier
11	V_{OUT}	DAC Voltage Output
12	NC	No Connection
13	NC	No Connection
14	NC	No Connection
15	NC	No Connection
16	DB0	Data Bit 0 (LSB)
17	DB1	Data Bit 1
18	DB2	Data Bit 2
19	DB3	Data Bit 3
20	DB4	Data Bit 4
21	DB5	Data Bit 5
22	DB6	Data Bit 6
23	NC	No Connection
24	NC	No Connection
25	NC	No Connection
26	TEST	Reserved, Connect to DGND
27	DB7	Data Bit 7
28	DB8	Data Bit 8
29	DB9	Data Bit 9
30	DB10	Data Bit 10
31	DB11	Data Bit 11
32	DB12	Data Bit 12
33	DB13	Data Bit 13
34	DB14	Data Bit 14
35	DB15	Data Bit 15 (MSB)
36	NC	No Connection
37	DGND	Digital Ground
38	V_{DD}	Digital Power Supply
39	$\overline{RST}$	V_{OUT} reset; active LOW, depending on the state of RSTSEL, the DAC register is either reset to mid-scale or min-scale.
40	LDAC	DAC register load control, rising edge triggered. Data is loaded from the input register to the DAC register.
41	$\overline{CS}$	Chip Select, active LOW
42	$R/\overline{W}$	Enabled by $\overline{CS}$, controls data read (HIGH) and write (LOW) from or to the input register.
43	RSTSEL	Reset Select; determines the action of $\overline{RST}$. If HIGH, $\overline{RST}$ will reset the DAC register to mid-scale. If LOW, $\overline{RST}$ will reset the DAC register to min-scale.
44	$\overline{REFEN}$	Enables internal +10V reference (REF_{OUT}), active LOW.
45	REF_{OUT}	Internal Reference Output
46	REFADJ	Internal Reference Trim. (Acts as a gain adjustment input when the internal reference is used.)
47	REF_{IN}	Reference Input
48	NC	No Connection

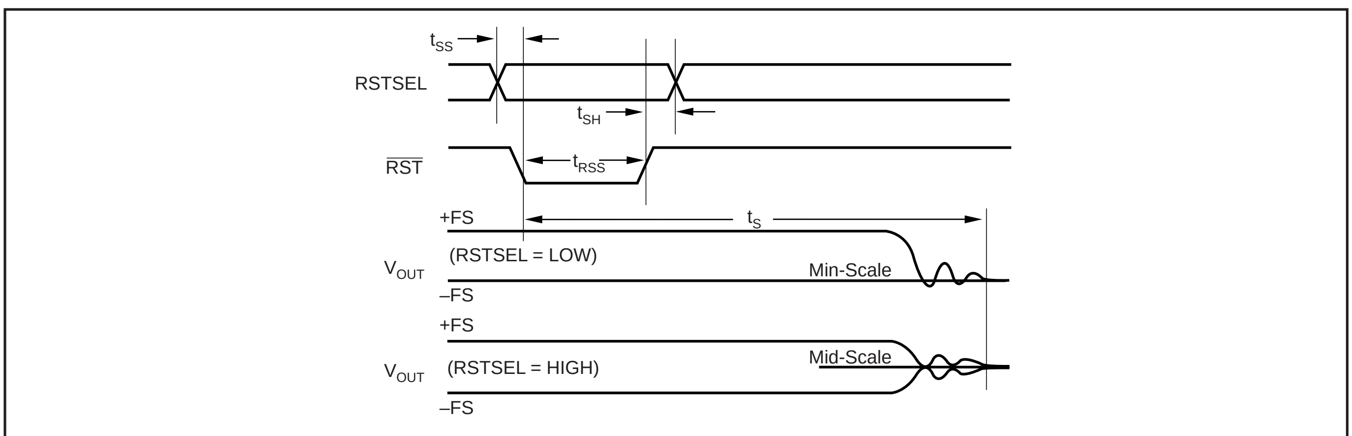
TIMING CHARACTERISTICS

PARAMETER	DESCRIPTION	DAC7741Y MIN	DAC7741Y TYP	DAC7741Y MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	100			ns
t_{RDS}	R/$\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	R/$\overline{W}$ HIGH after $\overline{CS}$ HIGH	10			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus High Impedance	10		70	ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		85	100	ns
t_{WCS}	$\overline{CS}$ LOW for Write	30			ns
t_{WS}	R/$\overline{W}$ LOW to $\overline{CS}$ LOW	10			ns
t_{WH}	R/$\overline{W}$ LOW after $\overline{CS}$ HIGH	10			ns
t_{LS}	$\overline{CS}$ LOW to LDAC HIGH	40			ns
t_{LH}	$\overline{CS}$ LOW after LDAC HIGH	0			ns
t_{LX}	LDAC HIGH	30			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	20			ns
t_{LWD}	LDAC LOW	40			ns
t_{SS}	RSTSEL Valid Before $\overline{RST}$ LOW	0			ns
t_{SH}	RSTSEL Valid After $\overline{RST}$ HIGH	10			ns
t_{RSS}	$\overline{RST}$ LOW	30			ns
t_S	Voltage Output Settling Time			5	µs

TIMING DIAGRAMS

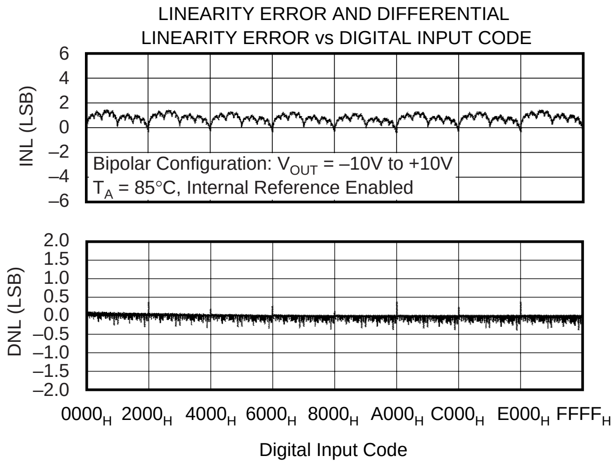


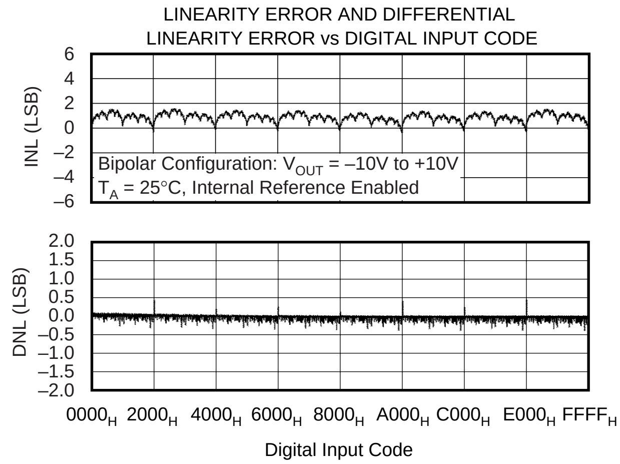
RESET TIMING

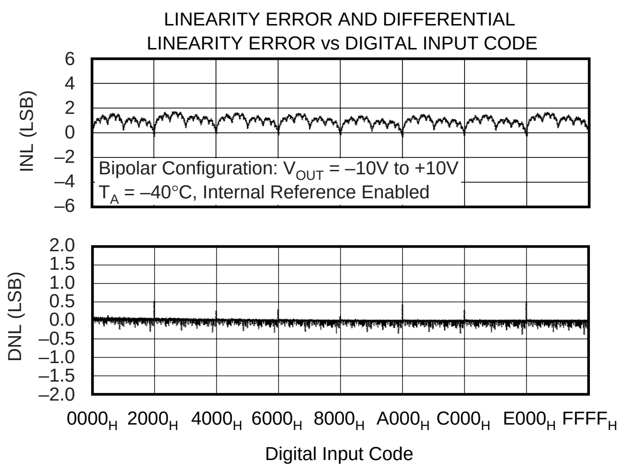


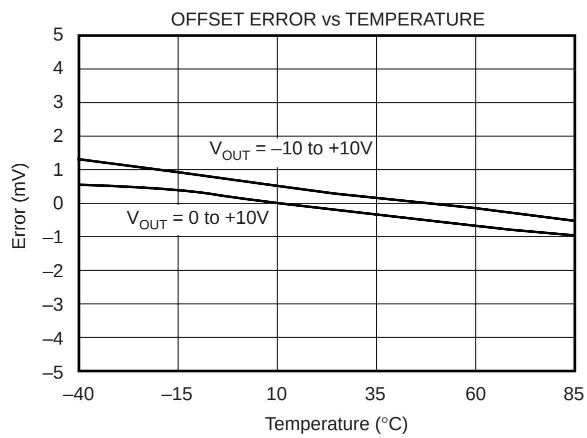
TYPICAL CHARACTERISTICS

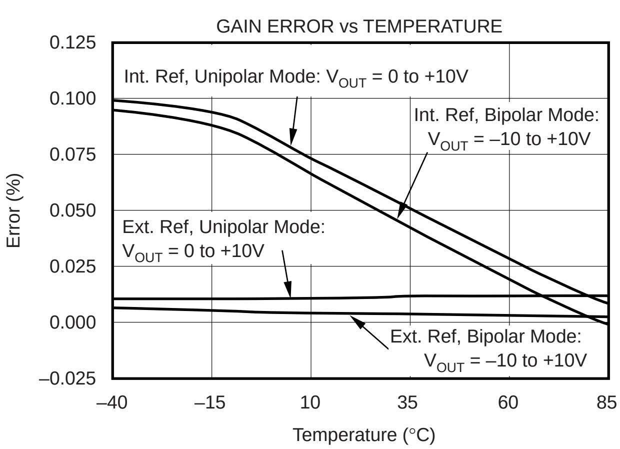
T_A = +25°C (unless otherwise noted)

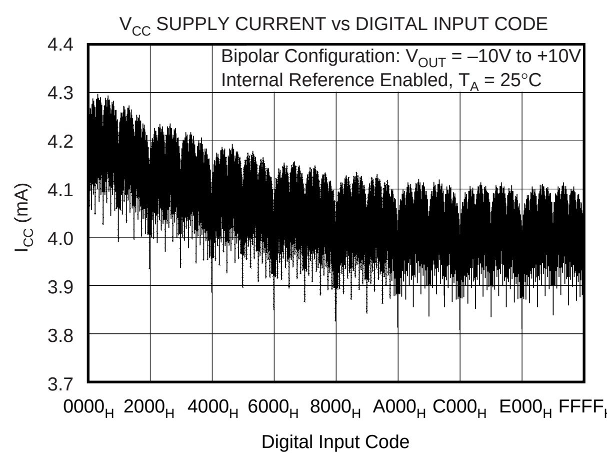






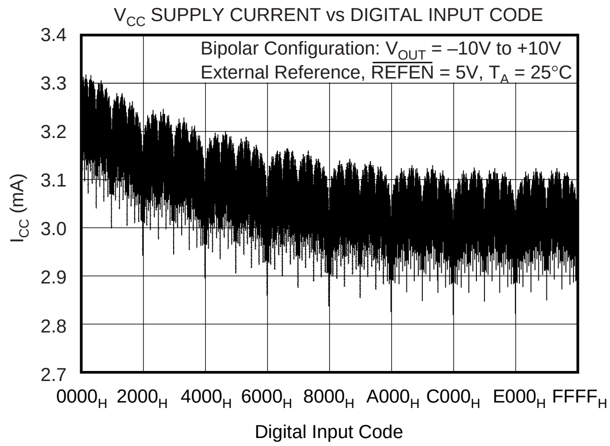


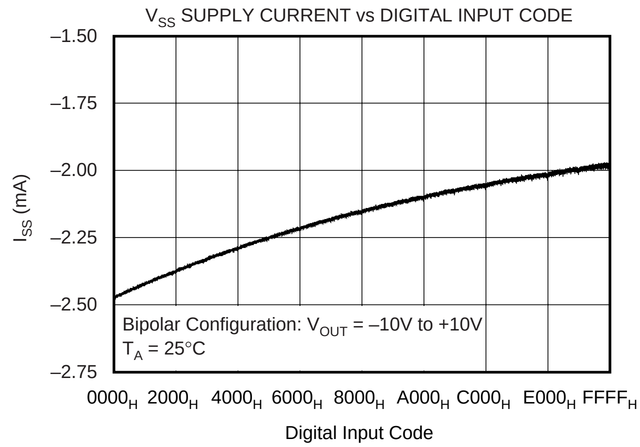


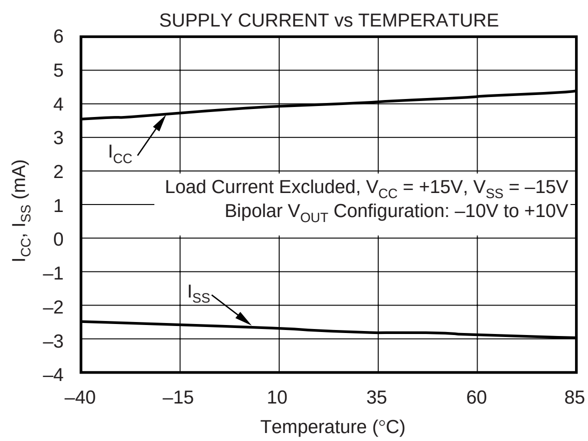


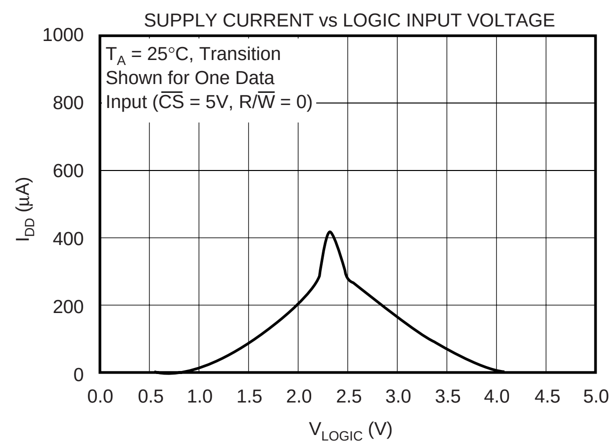
TYPICAL CHARACTERISTICS (Cont.)

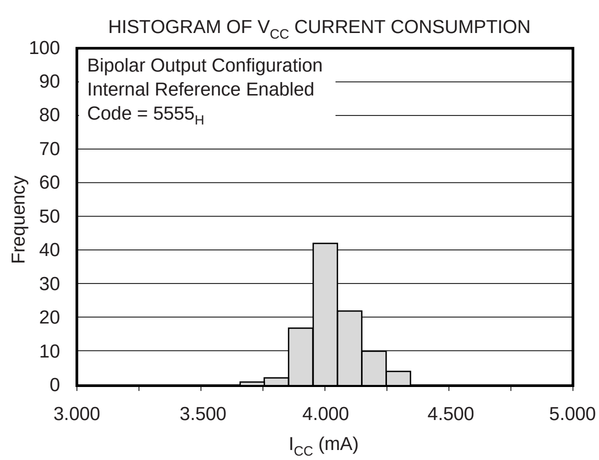
T_A = +25°C (unless otherwise noted)

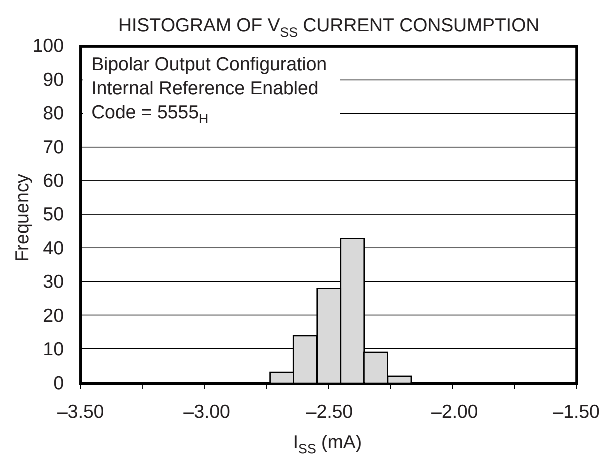




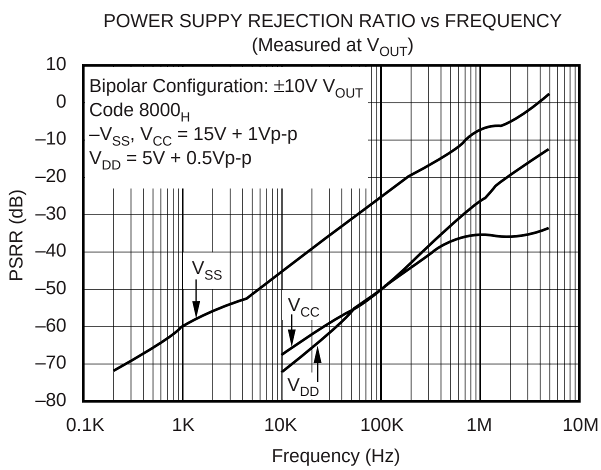


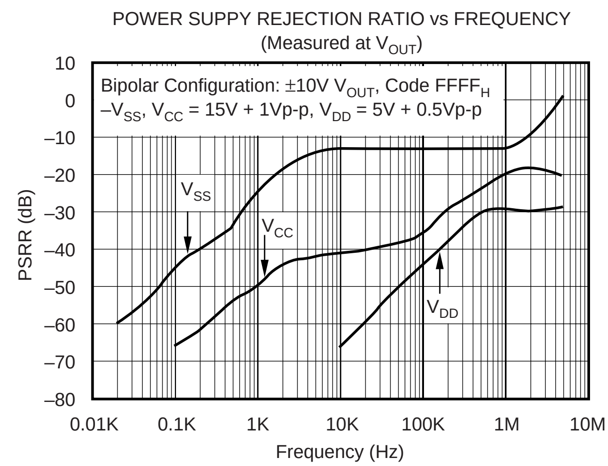


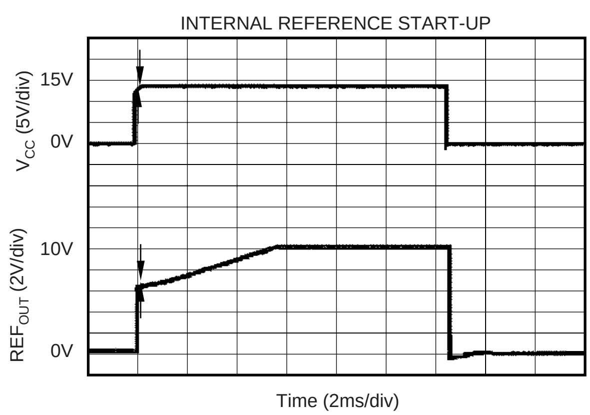


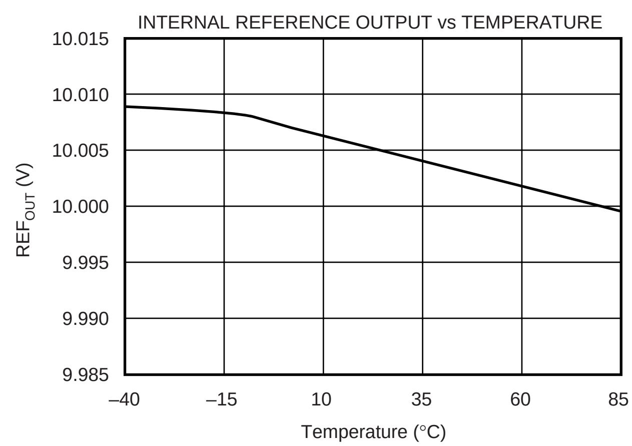


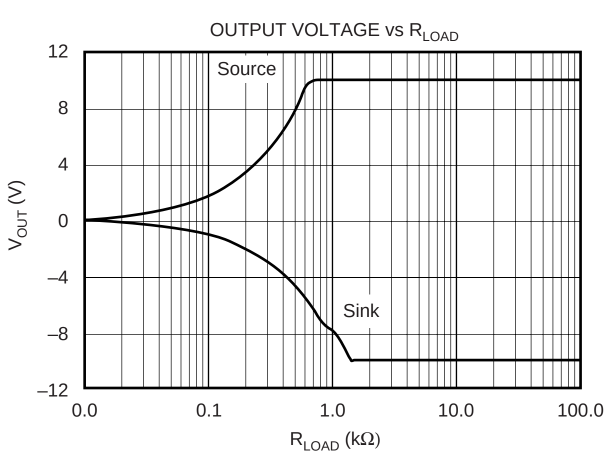
T_A = +25°C (unless otherwise noted)

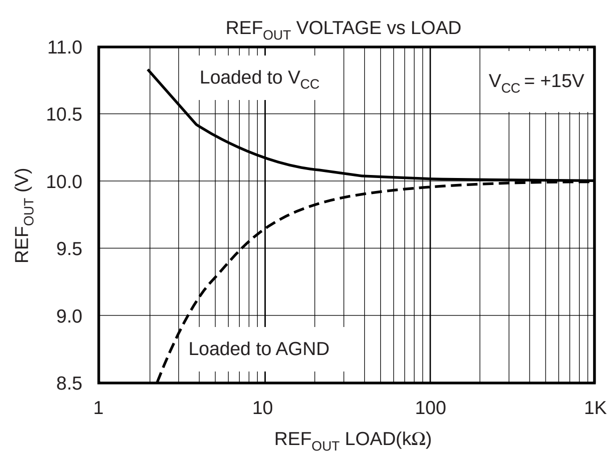






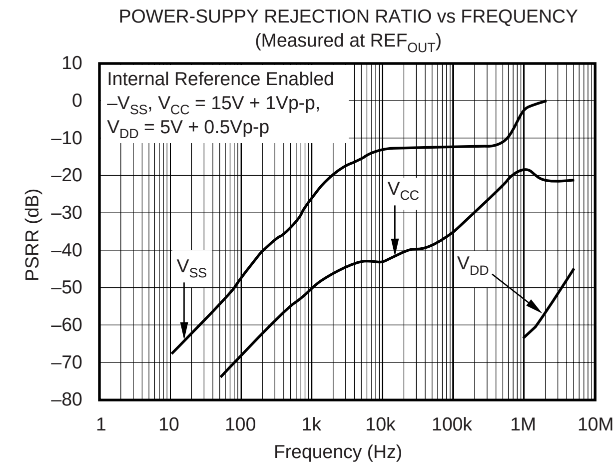


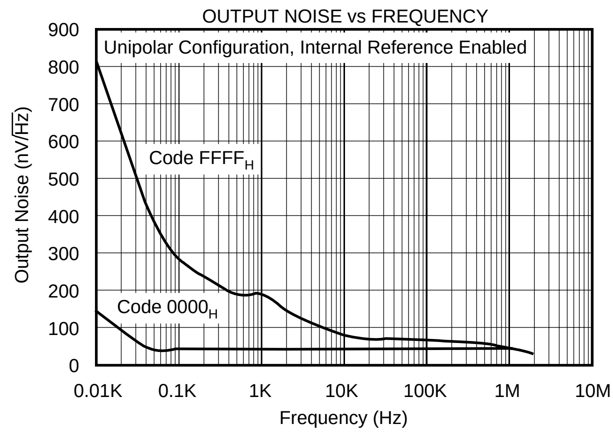


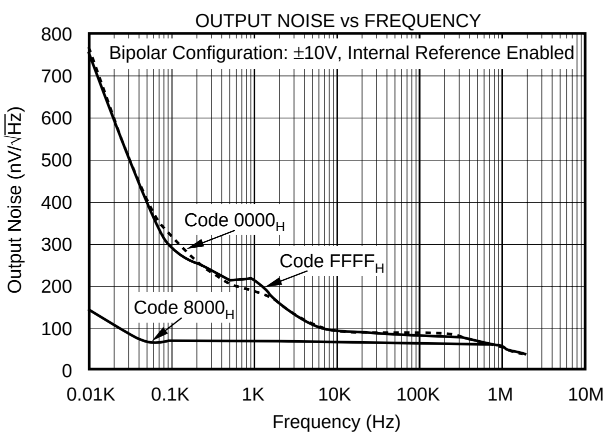


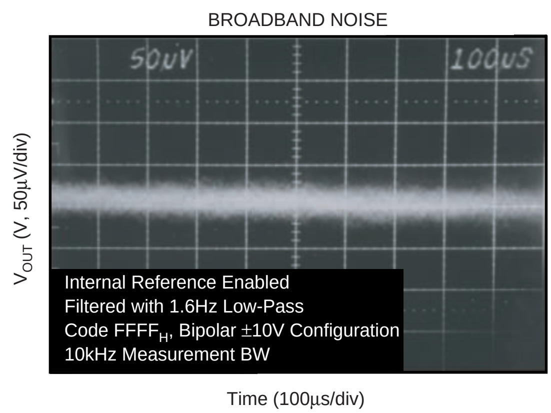
TYPICAL CHARACTERISTICS (Cont.)

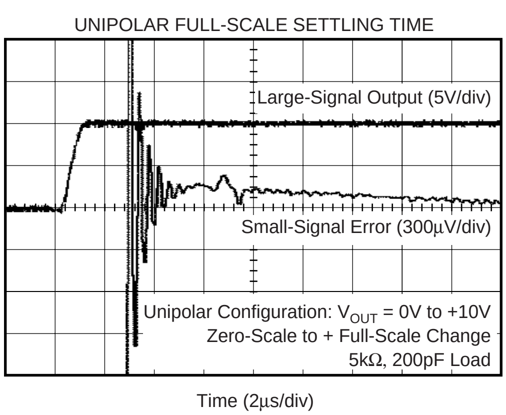
T_A = +25°C (unless otherwise noted)

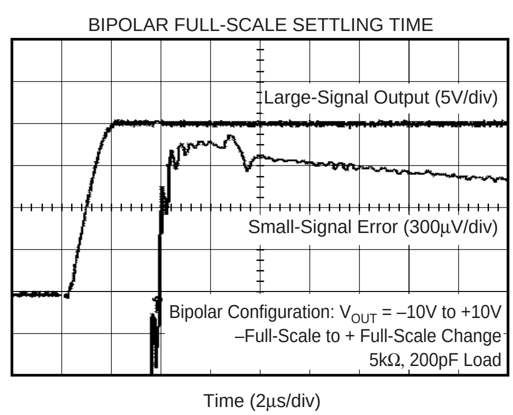






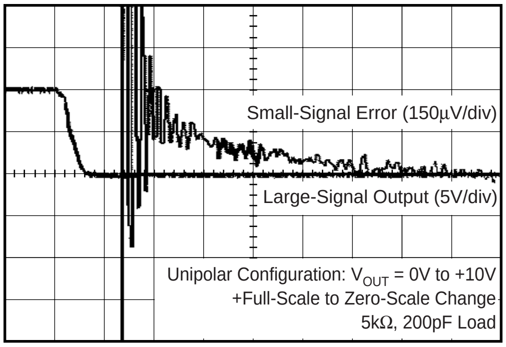






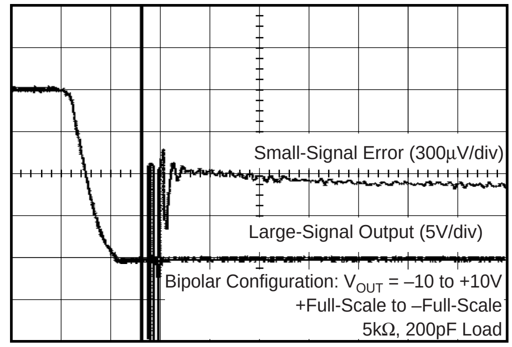
T_A = +25°C (unless otherwise noted)

UNIPOLAR FULL-SCALE SETTLING TIME



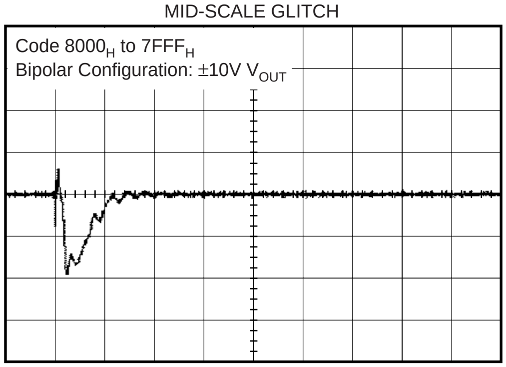
Time (2µs/div)

BIPOLAR FULL-SCALE SETTLING TIME



Time (2µs/div)

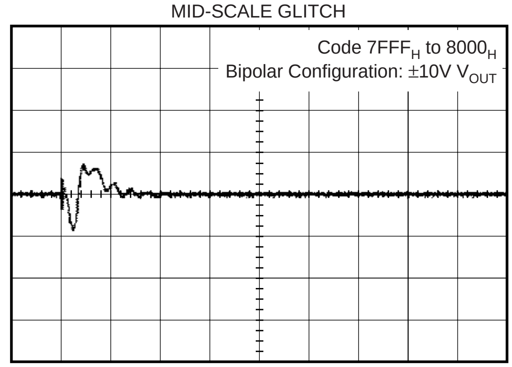
MID-SCALE GLITCH



V_{OUT} (V, 200mV/div)

Time (1µs/div)

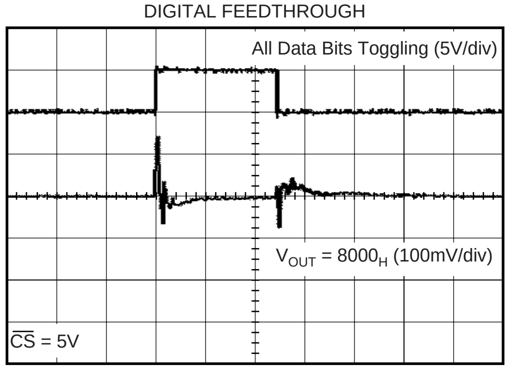
MID-SCALE GLITCH



V_{OUT} (V, 200mV/div)

Time (1µs/div)

DIGITAL FEEDTHROUGH



Time (200ns/div)

THEORY OF OPERATION

The DAC7741 is a voltage output, 16-bit DAC with a +10V built-in internal reference. The architecture is an R-2R ladder configuration with the three MSBs segmented, followed by an operational amplifier that serves as a buffer. The output buffer is designed to allow user-configurable output adjustments, giving the DAC7741 output voltage ranges of 0V to +10V, –5V to +5V, or –10V to +10V. Please refer to Figures 2, 3, and 4 for pin configuration information.

The digital input is a parallel word made up of the 16-bit DAC code, which is then loaded into the DAC register using the LDAC input pin. The converter can be powered from ±12V to ±15V dual analog supplies and a +5V logic supply. The device offers a reset function, which immediately sets the DAC output voltage and DAC register to min-scale (code 0000_H) or mid-scale (code 8000_H). The data I/O and reset functions are discussed in more detail in the following sections.

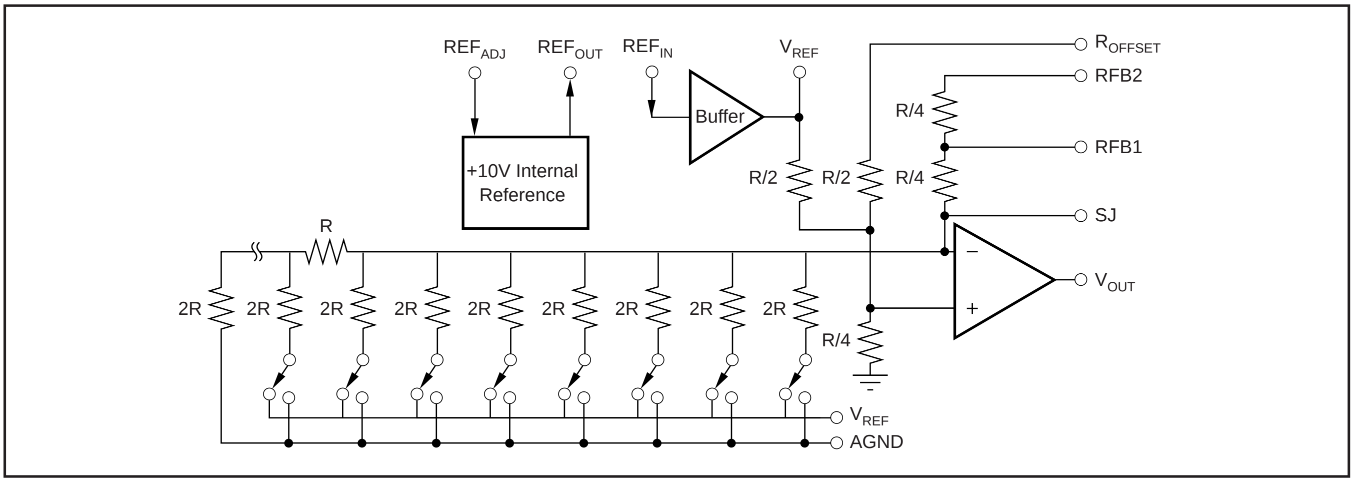


FIGURE 1. DAC7741 Architecture.

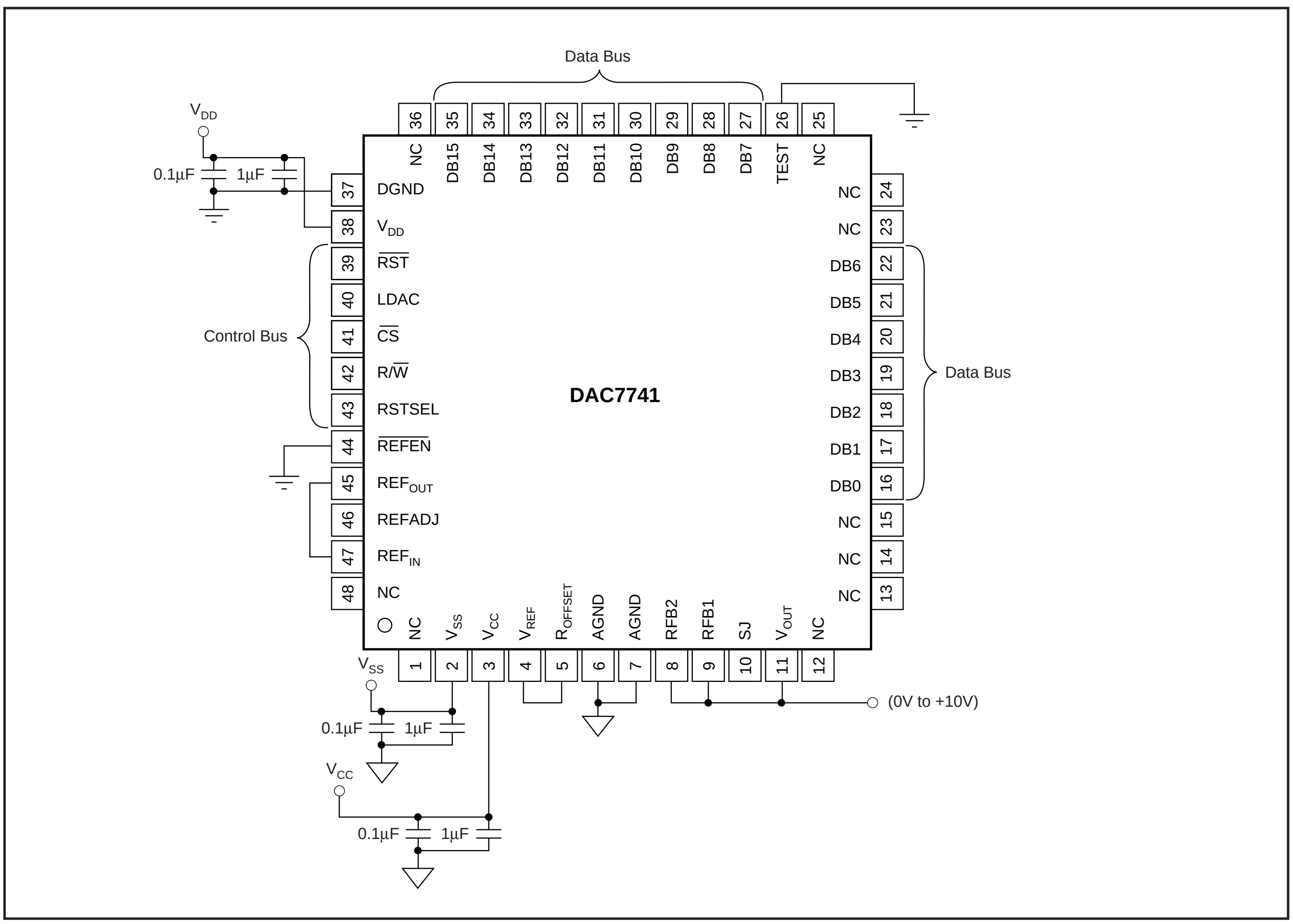


FIGURE 2. Basic Operation: V_{OUT} = 0 to +10V.

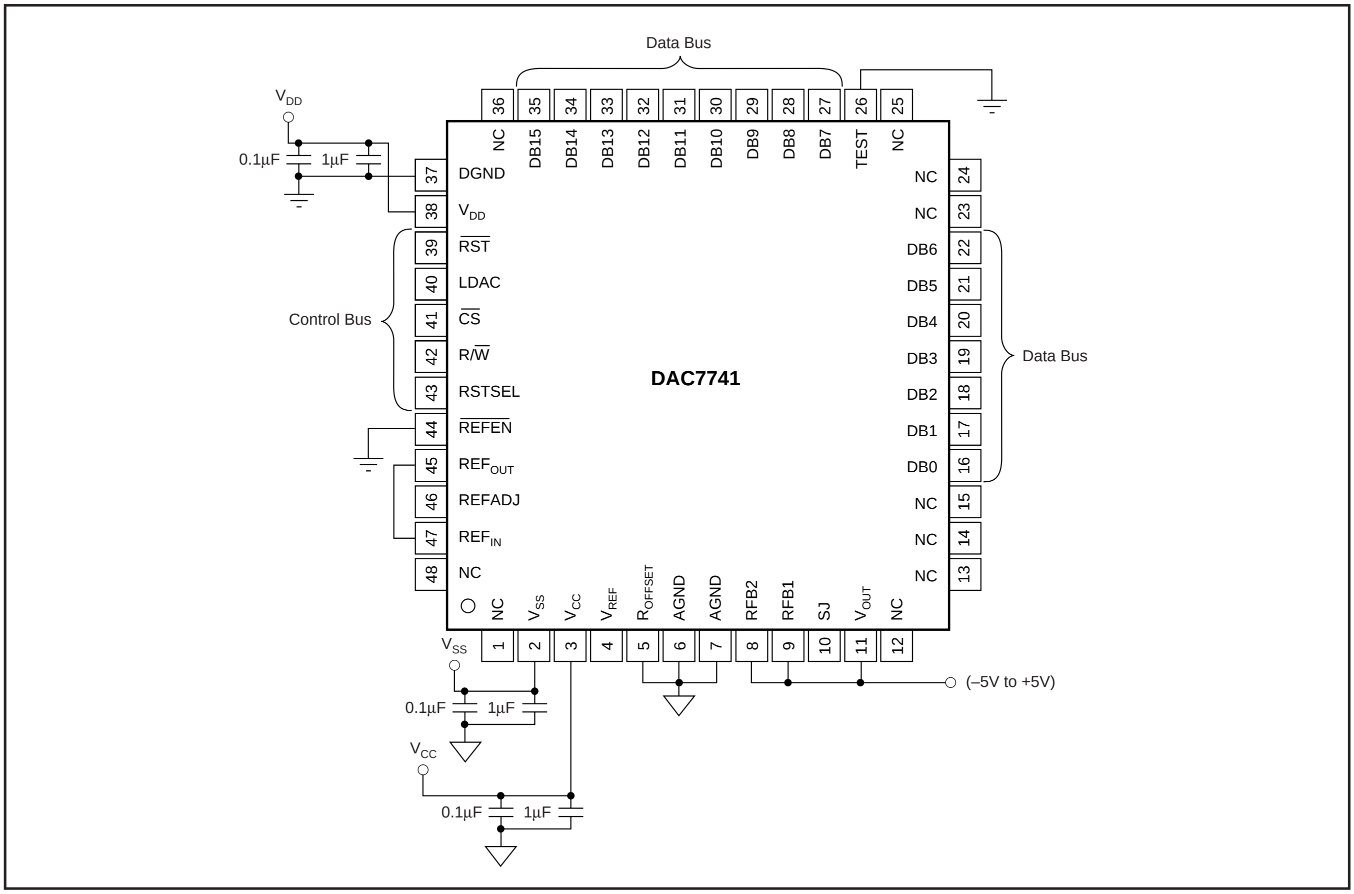


FIGURE 3. Basic Operation: V_{OUT} = –5V to +5V.

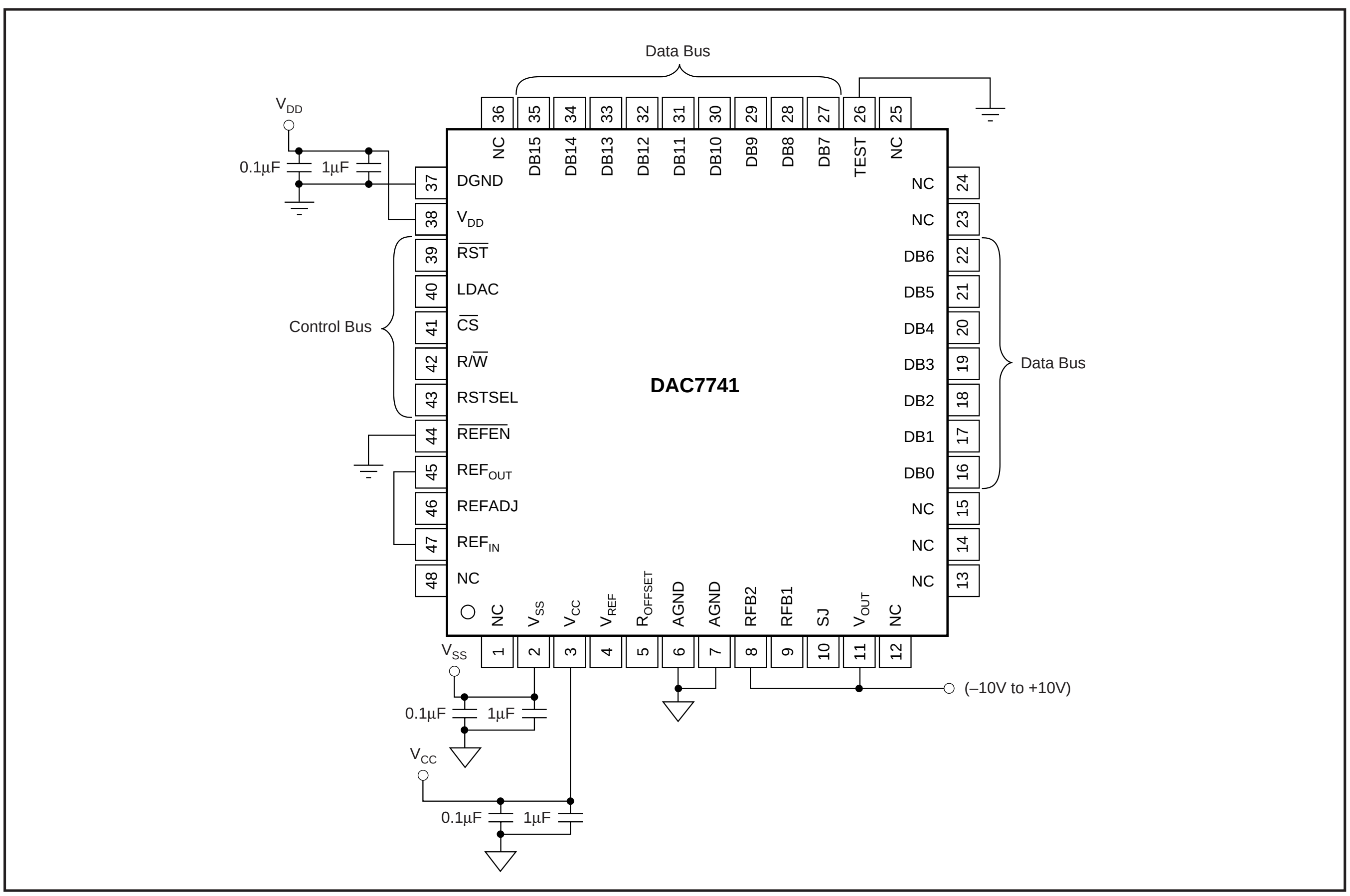


FIGURE 4. Basic Operation: V_{OUT} = –10V to +10V.

ANALOG OUTPUTS

The output amplifier can swing to within 1.4V of the supply rails, specified over the –40°C to +85°C temperature range. This allows for a ±10V DAC voltage output operation from ±12V supplies with a typical 5% tolerance.

When the DAC7741 is configured for a unipolar, 0V to 10V output, a negative voltage supply is required. This is due to internal biasing of the output stage. Please refer to the "Electrical Characteristics" table for more information.

The minimum and maximum voltage output values are dependent upon the output configuration implemented and reference voltage applied to the DAC7741. Please note that V_{SS} (the negative power supply) must be in the range of –4.75V to –15.75V for unipolar operation. The voltage on V_{SS} sets several bias points within the converter and is required in all modes of operation. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not ensured.

Supply sequence is important in establishing the correct startup of the DAC. The digital supply (V_{DD}) needs to establish correct bias conditions before the analog supplies (V_{CC}, V_{SS}) are brought up. If the digital supply cannot be brought up first, it must come up before either analog supply (V_{CC} or V_{SS}), with the preferred sequence of: V_{SS} (device substrate), V_{DD} then V_{CC}.

REFERENCE INPUTS

The DAC7741 provides a built-in +10V voltage reference and on-chip buffer to allow external component reference drive. To use the internal reference, $\overline{\text{REFEN}}$ must be LOW, enabling the reference circuitry of the DAC7741 (see Table I) and the REF_{OUT} pin must be connected to REF_{IN}. This is the input to the on-chip reference buffer. The buffers output is provided at the V_{REF} pin. In this configuration, V_{REF} is used to setup the DAC7741 output amplifier into one of three voltage output modes as discussed earlier. V_{REF} can also be used to drive other system components requiring an external reference.

The internal reference of the DAC7741 can be disabled when use of an external reference is desired. When using an external reference, the reference input, REF_{IN} , can be any voltage between 4.75V (or V_{SS} + 14V, whichever is greater) and V_{CC} – 1.4V.

$\overline{\text{REFEN}}$	ACTION
1	Internal Reference disabled; REF_{OUT} = HIGH Impedance
0	Internal Reference enabled; REF_{OUT} = +10V

TABLE I. $\overline{\text{REFEN}}$ Action.

DIGITAL INTERFACE

Table III shows the data format for the DAC7741 and Table II illustrates the basic control logic of the device. The interface consists of a chip select input ($\overline{\text{CS}}$), read/write control input (R/$\overline{\text{W}}$), data inputs (DB0-DB15) and a load DAC input (LDAC). An asynchronous reset input ($\overline{\text{RST}}$) which is active low, is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select (RSTSEL) signal. The DAC code is provided via a 16-bit parallel interface, as shown in Table II. The input word makes up the DAC code to be loaded into the data input register of the device. The data is latched into the input register on rising $\overline{\text{CS}}$ and is loaded into the DAC register upon reception of a rising edge on the LDAC input. This action updates the analog output, V_{OUT}, to the desired value. LDAC inputs of multiple DAC7741 devices can be connected when a synchronized update of numerous DAC outputs is desired. Please refer to the timing section for more detailed data I/O information.

DIGITAL INPUT	ANALOG OUTPUT	
	Unipolar Configuration	Bipolar Configuration
	Unipolar Straight Binary	Bipolar Offset Binary
0x0000	Zero (0V)	–Full-Scale (–V_{REF} or –V_{REF}/2)
0x0001	Zero + 1LSB	–Full-Scale + 1LSB
:	:	:
0x8000	1/2 Full-Scale	Bipolar Zero
0x8001	1/2 Full-Scale + 1LSB	Bipolar Zero + 1LSB
:	:	:
0xFFFF	Full-Scale (V_{REF} – 1LSB)	+Full-Scale (+V_{REF} – 1LSB or +V_{REF}/2 – 1LSB)

TABLE III. DAC7741 Data Format.

CONTROL STATUS					COMMAND		
R/$\overline{\text{W}}$	$\overline{\text{CS}}$	$\overline{\text{RST}}$	RSTSEL	LDAC	Input Register	DAC Register	Mode
L	L	H	X	H, L, ↓	Write	Hold	Write Data to Input Register
X	H	H	X	↑	Hold	Write	Update DAC register with data from input register.
L	L	H	X	↑	Transparent	Write	Write DAC register directly from data bus
H	L	H	X	H, L, ↓	Read	Hold	Read data in input register.
X	H	H	X	H, L, ↓	Hold	Hold	No Change
X	X	L	L	X	Reset to Min-Scale	Reset to Min-Scale	Reset to Input and DAC Register (0000_H) Min-Scale
X	X	L	H	X	Reset to Mid-Scale	Reset to Mid-Scale	Reset to Input and DAC Register (8000_H) Mid-Scale

TABLE II. DAC7741 Logic Truth Table.

DAC RESET

The $\overline{RST}$ and RSTSEL inputs control the reset of the analog output. The reset command is level triggered by a low signal on $\overline{RST}$. Once $\overline{RST}$ is LOW, the DAC output will begin settling to the mid-scale or min-scale code depending on the state of the RSTSEL input. A HIGH value on RSTSEL will cause V_{OUT} to reset to the mid-scale code (8000H) and a LOW value will reset V_{OUT} to min-scale (0000_H). A change in the state of the RSTSEL input while $\overline{RST}$ is LOW will cause a corresponding change in the reset command selected internally and consequently change the output value of V_{OUT} of the DAC. Note that a valid reset signal also resets the input register of the DAC to the value specified by the state of RSTSEL.

GAIN AND OFFSET CALIBRATION

The architecture of the DAC7741 is designed in such a way as to allow for easily configurable offset and gain calibration using a minimum of external components. The DAC7741 has built-in feedback resistors and output amplifier summing points brought out of the package in order to make the absolute calibration possible. Figures 5 and 6 illustrate the relationship of offset and gain adjustments for the DAC7741 in a unipolar configuration and in a bipolar configuration, respectively.

When calibrating the DAC output, offset should be adjusted first to avoid first order interaction of adjustments. In unipolar mode, the DAC7741 offset is adjusted from code 0000_H and for either bipolar mode, offset adjustments are made at code 8000_H. Gain adjustment can then be made at code $FFFF_H$ for each configuration, where the output of the DAC should be at +10V for the 0V to +10V – 1LSB or ±10V output range and +5V – 1LSB for the ±5V output range. Figure 7 shows the generalized external offset and gain adjustment circuitry using potentiometers.

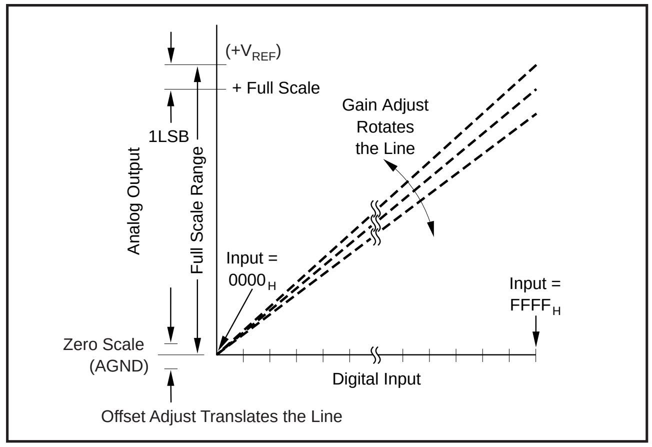


FIGURE 5. Relationship of Offset and Gain Adjustments for V_{OUT} = 0V to +10V Output Configuration.

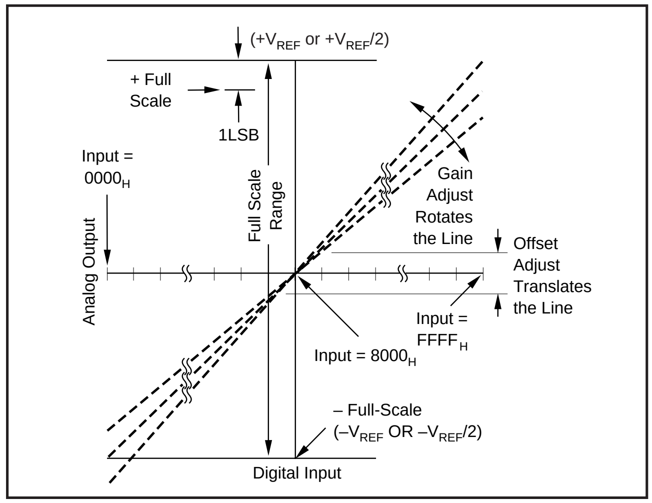


FIGURE 6. Relationship of Offset and Gain Adjustments for V_{OUT} = –10V to +10V Output Configuration. (Same theory applies for V_{OUT} = –5V to +5V).

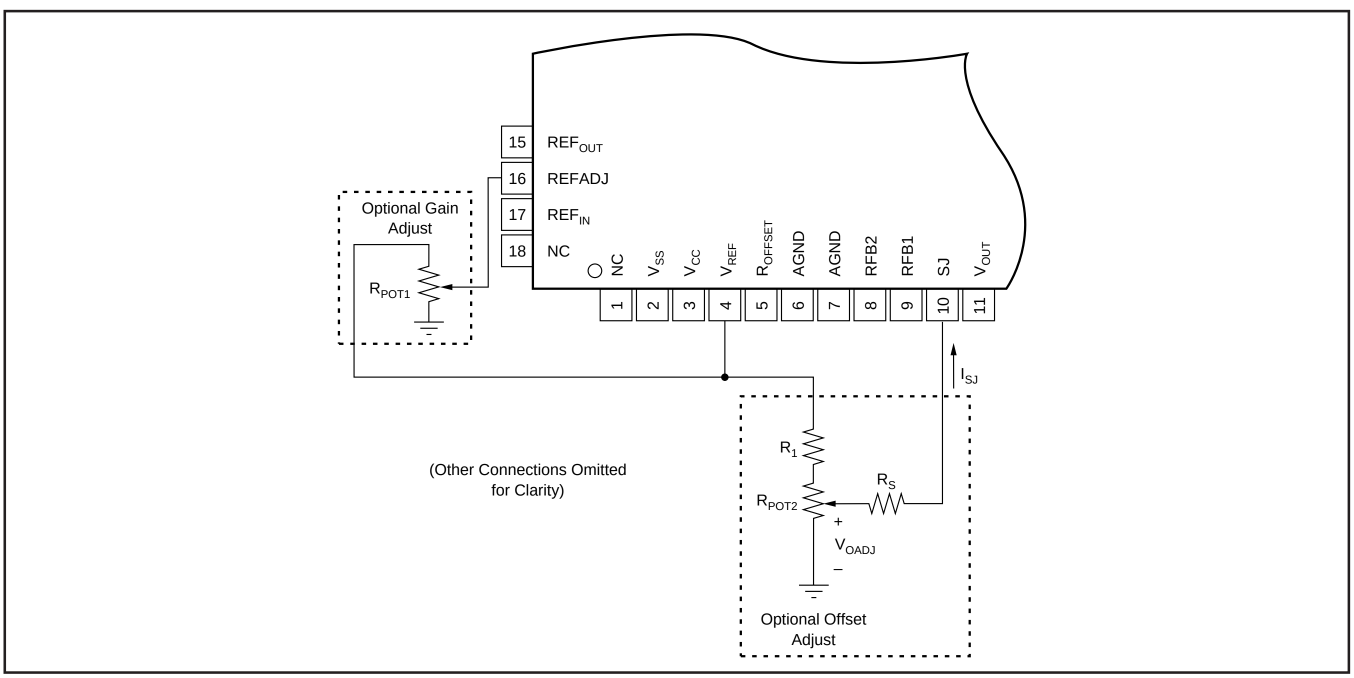


FIGURE 7. Generalized External Calibration Circuitry for Gain and Symmetrical Offset Adjustment.

OFFSET ADJUSTMENT

Offset adjustment is accomplished by introducing a small current into the summing junction (SJ) of the DAC7741. The voltage at SJ, or V_{SJ}, is dependent on the output configuration of the DAC7741. See Table IV for the required pin strapping for a given configuration and the nominal values of V_{SJ} for each output range.

REFERENCE CONFIGURATION	OUTPUT CONFIGURATION	PIN STRAPPING			V_{SJ}(1)
		R_{OFFSET}	RFB1	RFB2	
Internal Reference	0V to +10V –10V to +10V –5V to +5V	to V_{REF} NC to AGND	to V_{OUT} NC to V_{OUT}	to V_{OUT} to V_{OUT} to V_{OUT}	+5V +3.333V +1.666V
External Reference	0V to V_{REF} $-V_{REF}$ to V_{REF} $-V_{REF}/2$ to $V_{REF}/2$	to V_{REF} NC to AGND	to V_{OUT} NC to V_{OUT}	to V_{OUT} to V_{OUT} to V_{OUT}	$V_{REF}/2$ $V_{REF}/3$ $V_{REF}/6$
NOTE: (1) Voltage measured at V_{SJ} for a given configuration.					

TABLE IV. Nominal V_{SJ} vs. V_{OUT} and Reference Configuration.

The current level required to adjust the DAC7741 offset can be created by using a potentiometer divider as shown in Figure 7. Another alternative is to use a unipolar DAC in order to apply a voltage, V_{OADJ}, to the resistor R_S. A ±2uA current range applied to SJ will ensure offset adjustment coverage of the ±0.1% maximum offset specification of the DAC7741.

When in a unipolar configuration (V_{SJ} = 5V), only a single resistor, R_S, is needed for symmetrical offset adjustment with a 0V to 10V V_{OADJ} range. When in one of the two bipolar configurations, V_{SJ} is either +3.333v (±10V range) or +1.666V (±5V range), and circuit values chosen to match those given in Table V will provide symmetrical offset adjust. Please refer to Figure 7 for component configuration.

OUTPUT CONFIGURATION	R_{POT2}	R_1	R_S	I_{SJ} RANGE	NOMINAL OFFSET ADJUSTMENT
0V to +10V	10K	0	2.5M	±2µA	±25mV
–10V to +10V	10K	5K	1.5M	±2.2µA	±55mV
–5V to +5V	10K	20K	1M	±1.7µA	±21mV

TABLE V. Recommended External Component Values for Symmetrical Offset Adjustment (V_{REF} = 10V).

Figure 8 illustrates the typical and minimum offset adjustment ranges provided by forcing a current at SJ for a given output voltage configuration.

GAIN ADJUSTMENT

When using the internal reference of the DAC7741, gain adjustment is performed by adjusting the internal reference voltage via the reference adjust pin, REFADJ. The effect of a reference voltage change on the gain of the DAC output can be seen in the generic equation (for unipolar configuration):

$$V_{OUT} = V_{REFIN} \bullet (N/65536)$$

where N is represented in decimal format and ranges from 0 to 65535.

REFADJ can be driven by a low impedance voltage source such as a unipolar, 0V to +10V DAC or a potentiometer (less than 100kΩ) as shown in Figure 7. Since the input impedance of REFADJ is typically 50kΩ, the smaller the resistance of the potentiometer, the more linear the adjustment will be. A 10kΩ potentiometer is suggested if linearity of the reference adjustment is of concern.

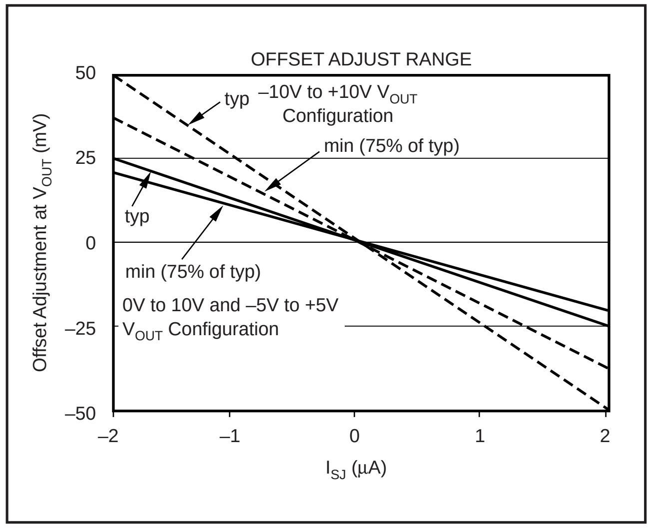


FIGURE 8. Offset Adjustment Transfer Characteristic.

When the DAC7741 internal reference is not used, gain adjustments can be made via trimming the external reference applied to the DAC at REF_{IN}. This can be accomplished through using a potentiometer, unipolar DAC, or other means of precision voltage adjustment to control the voltage presented to the DAC7741 by the external reference. Figure 9 and Table VI summarize the range of adjustment of the internal reference via REFADJ.

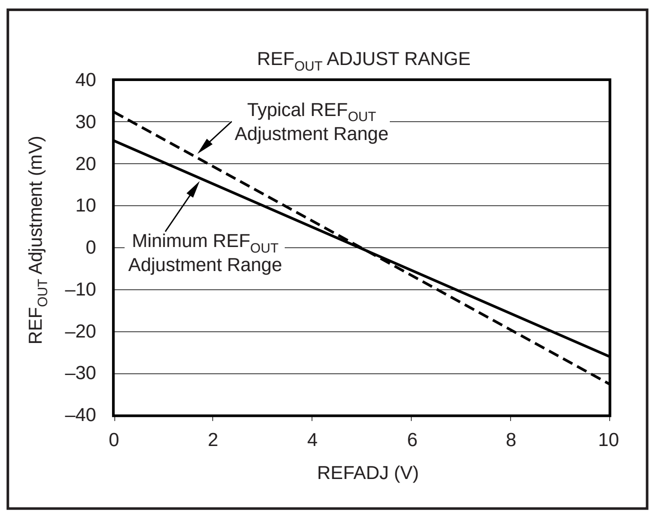


FIGURE 9. Internal Reference Adjustment Transfer Characteristic.

VOLTAGE AT REFADJ	REF_{OUT} VOLTAGE
REFADJ = 0V REFADJ = 5V or NC(1) REFADJ = 10V	10V + 25mV (min) 10V 10V – 25mV (max)
NOTE: "NC" is "Not Connected"	

TABLE VI. Minimum Internal Reference Adjustment Range.

NOISE PERFORMANCE

Increased noise performance of the DAC output can be achieved by filtering the voltage reference input to the DAC7741. Figure 10 shows a typical internal reference filter schematic. A low-pass filter applied between the REF_{OUT} and REF_{IN} pins can increase noise immunity at the DAC and output amplifier. The REF_{OUT} pin can source a maximum of 50µA so care should be taken in order to avoid overloading the internal reference output.

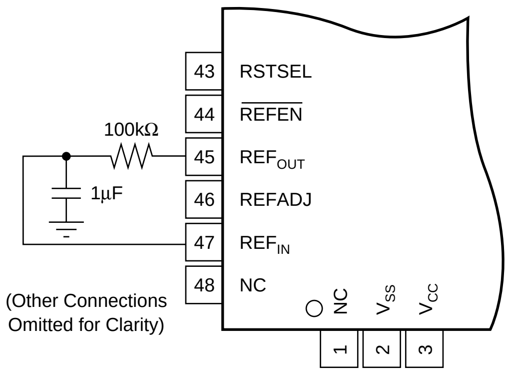


FIGURE 10. Internal Reference Filter.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC7741 offers separate digital and analog supplies, as it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more important it will become to separate the analog and digital ground and supply planes at the device.

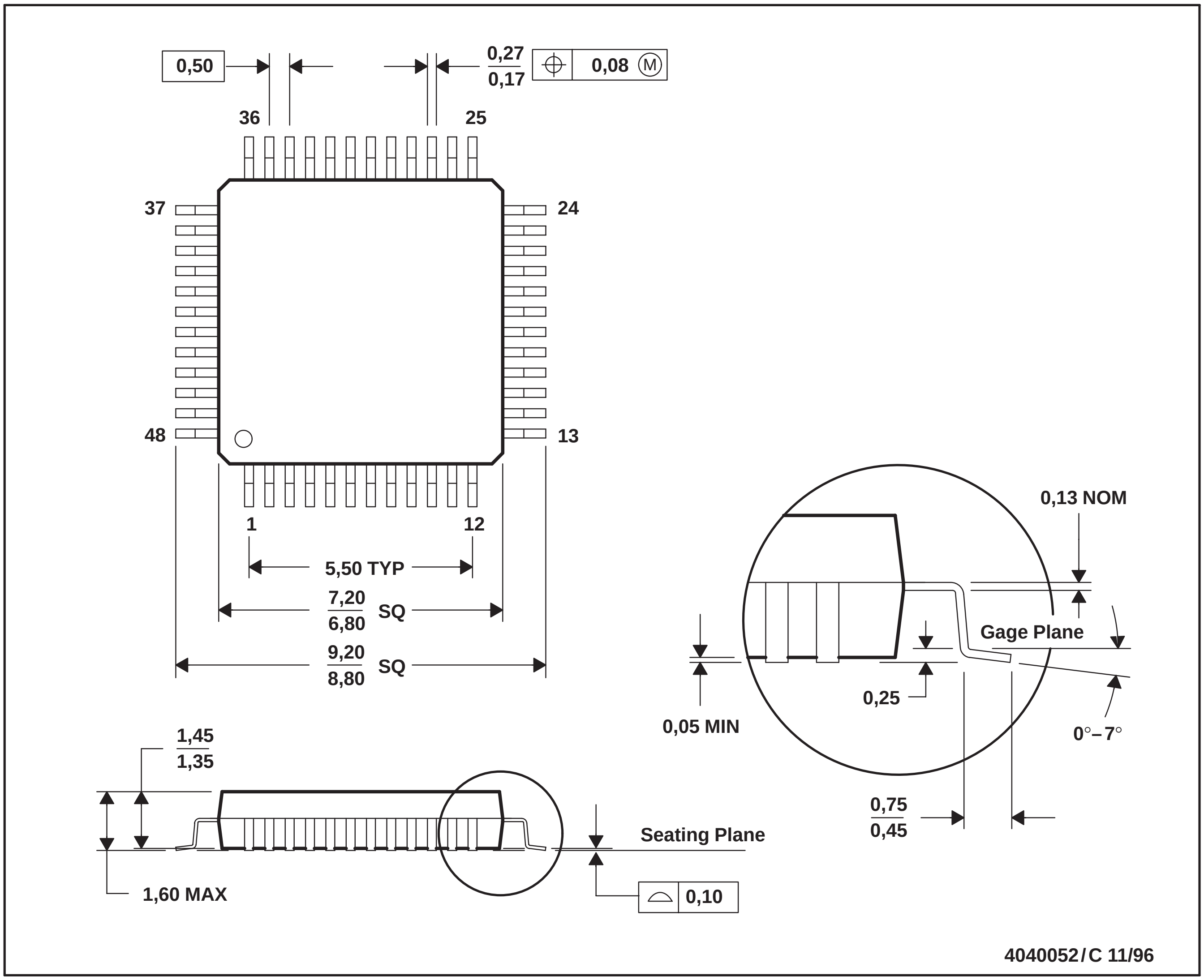
Since the DAC7741 has both analog and digital ground pins, return currents can be better controlled and have less effect on the DAC output error. Ideally, AGND would be connected directly to an analog ground plane and DGND to the digital ground plane. The analog ground plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The voltages applied to V_{CC} and V_{SS} should be well regulated and low noise. Switching power supplies and dc/dc converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

In addition, a 1µF to 10µF bypass capacitor in parallel with a 0.1µF bypass capacitor is strongly recommended for each supply input. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a "Pi" filter made up of inductors and capacitors–all designed to essentially low-pass filter the analog supplies, removing any high frequency noise components.

MTQF003A – OCTOBER 1994 – REVISED DECEMBER 1996

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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