M5M5V4R01J-12,-15

1997.11.20 Rev.F

4194304-BIT (4194304-WORD BY 1-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V4R01J is a family of 4194304-word by 1-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high speed application.

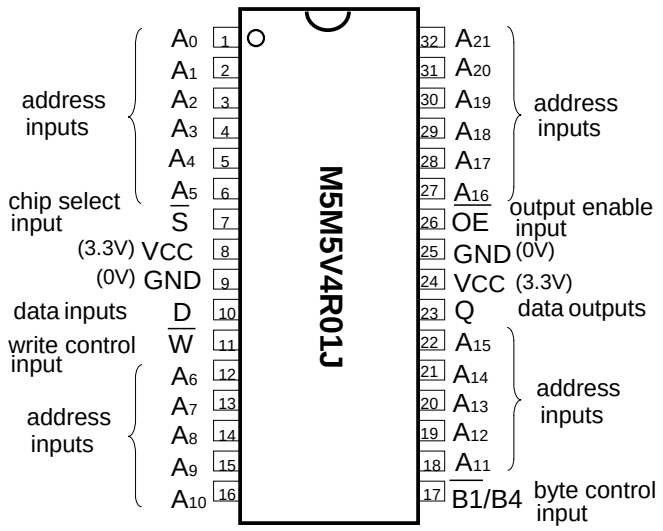
The M5M5V4R01J is offered in a 32-pin plastic small outline J-lead package(SOJ).

These device operate on a single 3.3V supply, and are directly TTL compatible. They include a power down feature as well.

FEATURES

- Fast access time M5M5V4R01J-12 •••• 12ns(max)
  M5M5V4R01J-15 •••• 15ns(max)
- Low power dissipation Active •••••••••• 297mW(typ)
  Stand by •••••••••• 3.3mW(typ)
- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Test mode is available
- Easy memory expansion by $\overline{S}$
- Three-state outputs : OR-tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Directly TTL compatible : All inputs and outputs

PIN CONFIGURATION (TOP VIEW)



Outline 32P0K

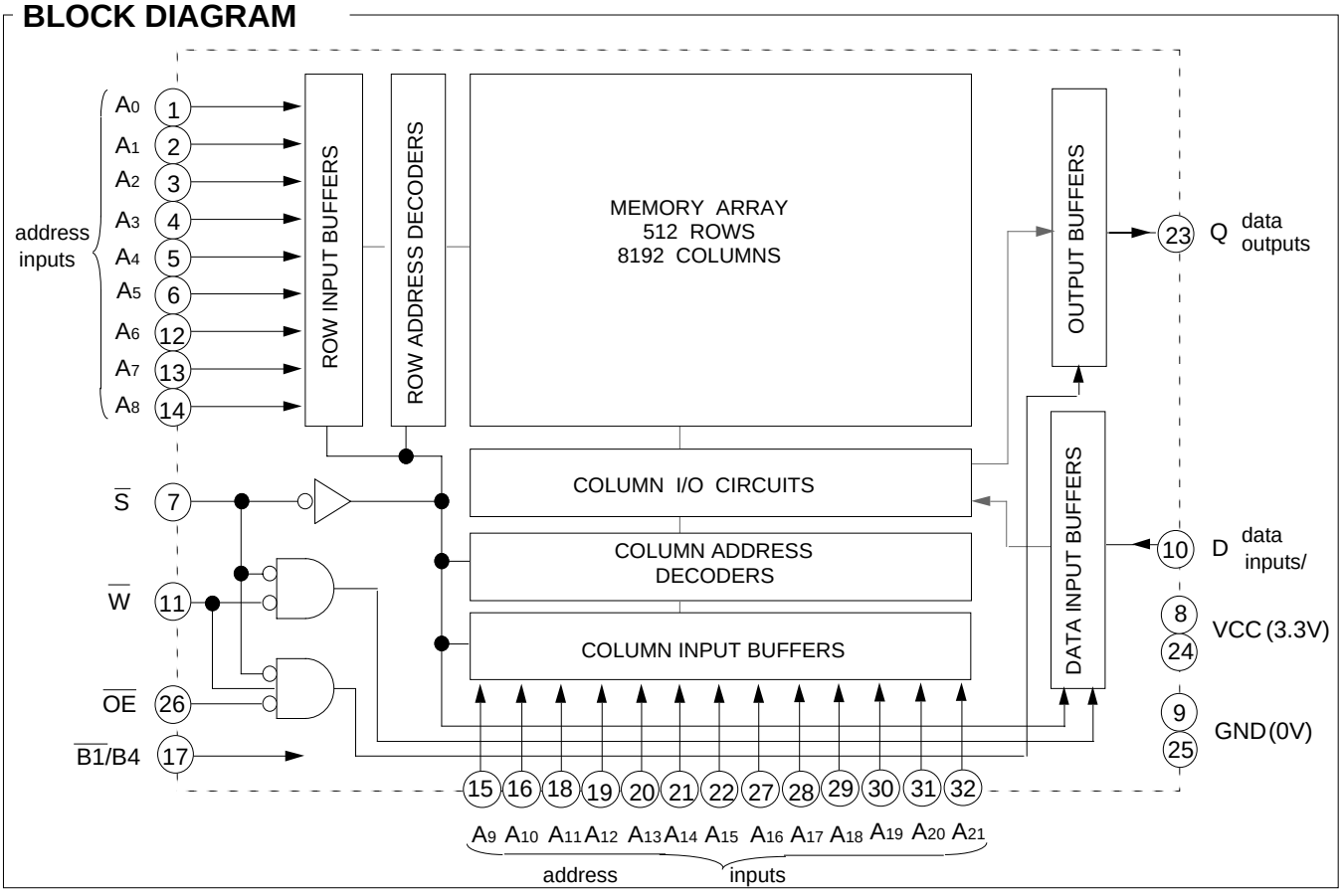
APPLICATION

High-speed memory units

PACKAGE

32pin 400mil SOJ

BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M5V4R01J is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of $\overline{W}$ or $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high impedance state, and the data bus
contention problem in the write cycle is eliminated.

A read cycle is excuted by setting W at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state ($\overline{S}$=L).

When setting $\overline{S}$ at high level, the chip is in a non-selectable mode in which both reading and writing are disable. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$.

Signal-$\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissapation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

The RAM works with an organization of 4194304-word by 1 bit,when $\overline{B1}$/B4 is low of floating. And an organization of 10485 76-word by 4bit is also obtained for reducing the test time, when $\overline{B1}$/B4 is high.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	D	Q	Icc
H	X	X	Non selection	High-impedance	High-impedance	Stand by
L	L	X	Write	Din	High-impedance	Active
L	H	L	Read	High-impedance	Dout	Active
L	H	H		High-impedance	High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-2.0* ~ 4.6	V
V_I	Input voltage		-2.0* ~ VCC+0.5	V
V_O	Output voltage		-2.0* ~ VCC+0.5	V
Pd	Power dissipation	Ta=25℃	1000	mW
Topr	Operating temperature		0 ~ 70	℃
Tstg(bias)	Storage temperature (bias)		-10 ~ 85	℃
T_{stg}	Storage temperature		-65 ~ 150	℃

*Pulse width ≤ 20ns, In case of DC:-0.5V

DC ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70℃, Vcc=3.3V $^{+10\%}_{-5\%}$ unless otherwise noted)

Symbol	Parameter	Condition			Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage				2.2		Vcc+0.3	V
V_{IL}	Low-level input voltage				-0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} =-4mA			2.0			V
V_{OL}	Low-level output voltage	I_{OL}= 8mA					0.4	V
I_I	Input current	V_I = 0~Vcc					2	μA
$\lvert I_{OZ} \rvert$	Output current in off-state	$V_{I(\overline{S})}$= V_{IH} V_O= 0~Vcc					10	μA
I_{CC1}	Active supply current (TTL level)	$V_{I(\overline{S})}$= V_{IL} other inputs V_{IH} or V_{IL} Output-open(duty 100%)	AC	12ns cycle			160	mA
				15ns cycle			150	
			DC			90	100	
I_{CC2}	Stand by current (TTL level)	$V_{I(\overline{S})}$= V_{IH}	AC	12ns cycle			75	mA
				15ns cycle			70	
			DC				50	
I_{CC3}	Stand by current	$V_{I(\overline{S})}$= Vcc≥0.2V other inputs V_I≤0.2V or V_I≥Vcc-0.2V				1	10	mA

CAPACITANCE (Ta=0 ~ 70℃, Vcc=3.3V $^{+10\%}_{-5\%}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Limit			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms,f=1MHz			8	pF
C_O	Output capacitance	V_O=GND, V_O=25mVrms,f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc=5V,Ta=25℃
3: C_I,C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70℃, Vcc=3.3V $^{+10\%}_{-5\%}$ unless otherwise noted)

(1)MEASUREMENT CONDITION

Input pulse levels ••••••••••••••••••••••••• V_{IH}=3.0V, V_{IL}=0.0V
Input rise and fall time ••••••••••••••••••••••••••••••••••••• 3ns
Input timing reference levels •••••••••••• V_{IH}=1.5V, V_{IL}=1.5V
Output timing reference levels •••••••••• V_{OH}=1.5V, V_{OL}=1.5V
Output loads ••• Fig1 ,Fig2

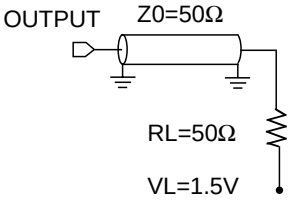


Fig.1 Output load

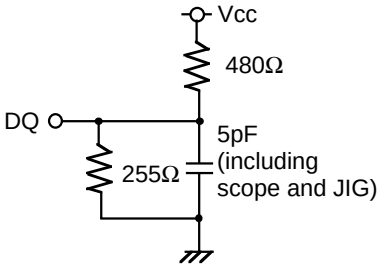


Fig.2 Output load for t_{en}, t_{dis}

(2)READ CYCLE

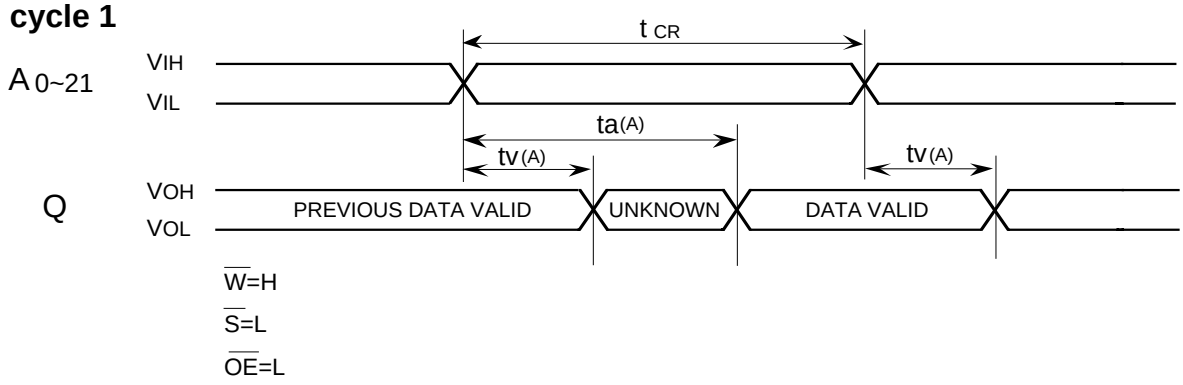
Symbol	Parameter	Limits				Unit
		M5M5V4R01J -12		M5M5V4R01J -15		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	12		15		ns
$ta_{(A)}$	Address access time		12		15	ns
$ta_{(S)}$	Chip select access time		12		15	ns
$ta_{(OE)}$	Output enable access time		6		8	ns
$tdis_{(S)}$	Output disable time after $\overline{S}$ high	0	6	0	7	ns
$tdis_{(OE)}$	Output disable time after $\overline{OE}$ high	0	6	0	7	ns
$ten_{(S)}$	Output enable time after $\overline{S}$ low	0		0		ns
$ten_{(OE)}$	Output enable time after $\overline{OE}$ low	0		0		ns
$tv_{(A)}$	Data valid time after address change	3		3		ns
tPU	Power-up time after chip selection	0		0		ns
tPD	Power-down time after chip selection		12		15	ns

(3)WRITE CYCLE

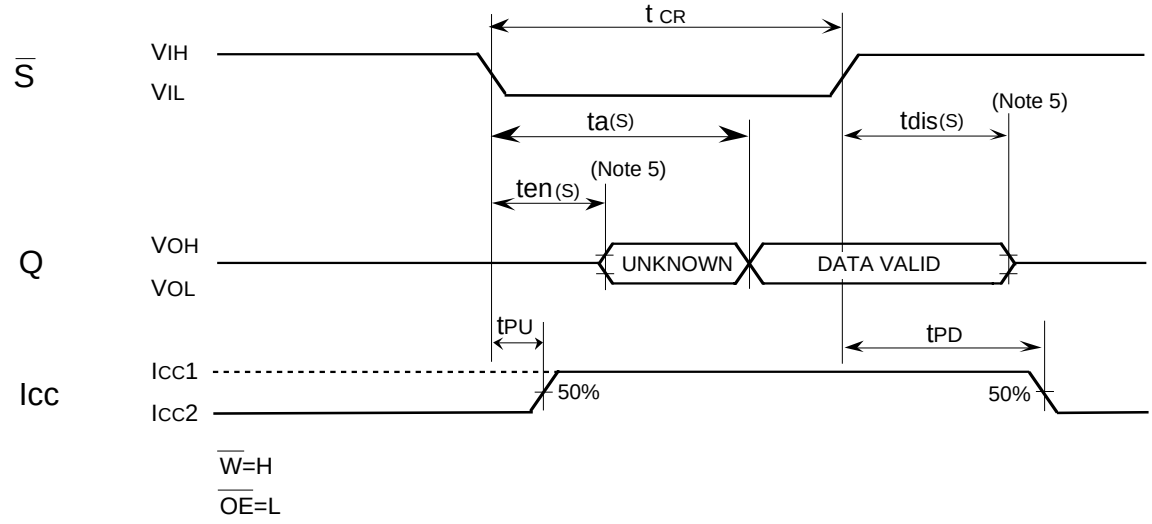
Symbol	Parameter	Limits				Unit
		M5M5V4R01J -12		M5M5V4R01J -15		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	12		15		ns
$tw_{(W)}$	Write pulse width	10		12		ns
$tsu_{(A)1}$	Address setup time($\overline{W}$)	0		0		ns
$tsu_{(A)2}$	Address setup time($\overline{S}$)	0		0		ns
$tsu_{(S)}$	Chip select setup time	10		12		ns
$tsu_{(D)}$	Data setup time	6		7		ns
$th_{(D)}$	Data hold time	0		0		ns
$trec_{(W)}$	Write recovery time	1		1		ns
$tdis_{(W)}$	Output disable time after $\overline{W}$ low	0	6	0	7	ns
$tdis_{(OE)}$	Output disable time after $\overline{OE}$ high	0	6	0	7	ns
$ten_{(W)}$	Output enable time after $\overline{W}$ high	0		0		ns
$ten_{(OE)}$	Output enable time after $\overline{OE}$ low	0		0		ns
$tsu_{(A-WH)}$	Address to $\overline{W}$ High	10		12		ns

(4)TIMING DIAGRAMS

Read cycle 1

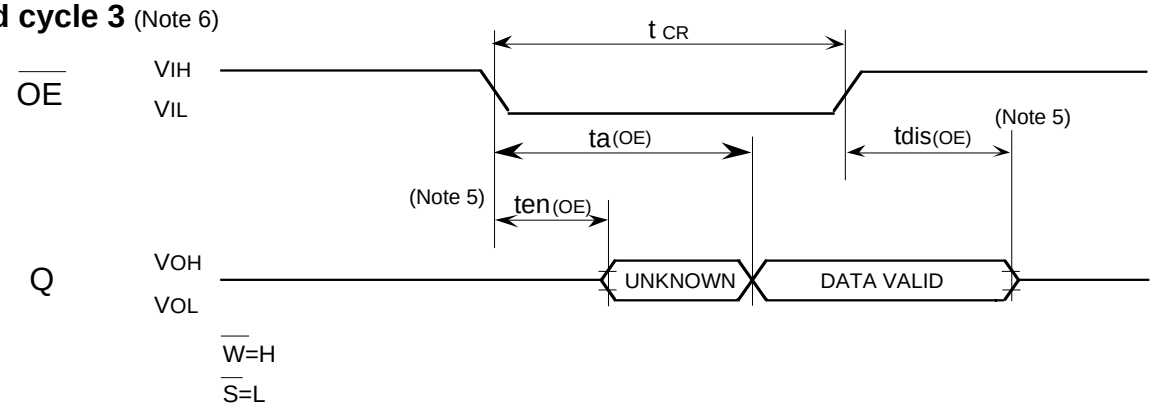


Read cycle 2 (Note 4)



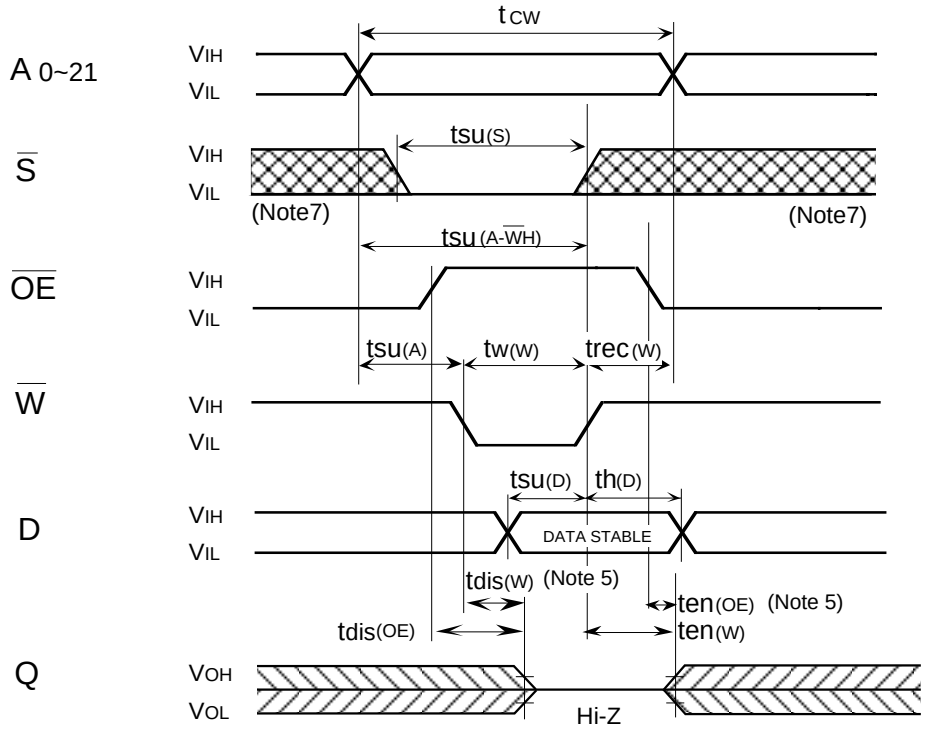
Note 4. Addresses valid prior to or coincident with S transition low.
5. Transition is measured ±500mv from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 6)

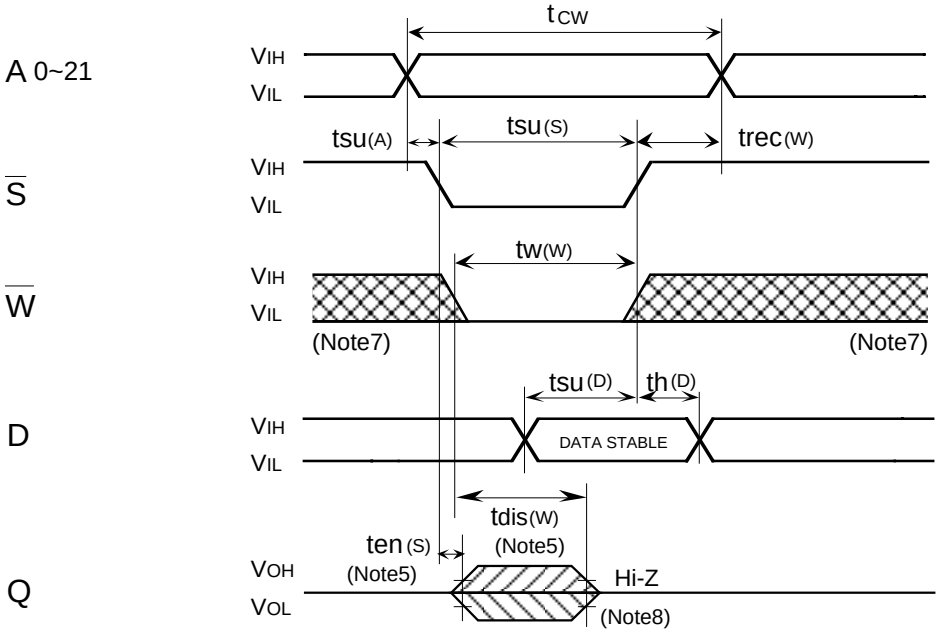


Note 6. Addresses and S valid prior to OE transition low by (ta(A)-ta(OE)), (ta(S)-ta(OE))

Write cycle ($\overline{W}$ control mode)



Write cycle ($\overline{S}$ control mode)



Note 7: Hatching indicates the state is don't care.

8: When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

9: ten,tdis are periodically sampled and are not 100% tested.