General Purpose USB Device

GENERAL DESCRIPTION

CS8810 is a single chip general-purpose USB controller, which integrates USB 1.1 compliant transceiver. Together with product dependent firmware and software driver, this chip is able to fulfill diverse demand of end products.

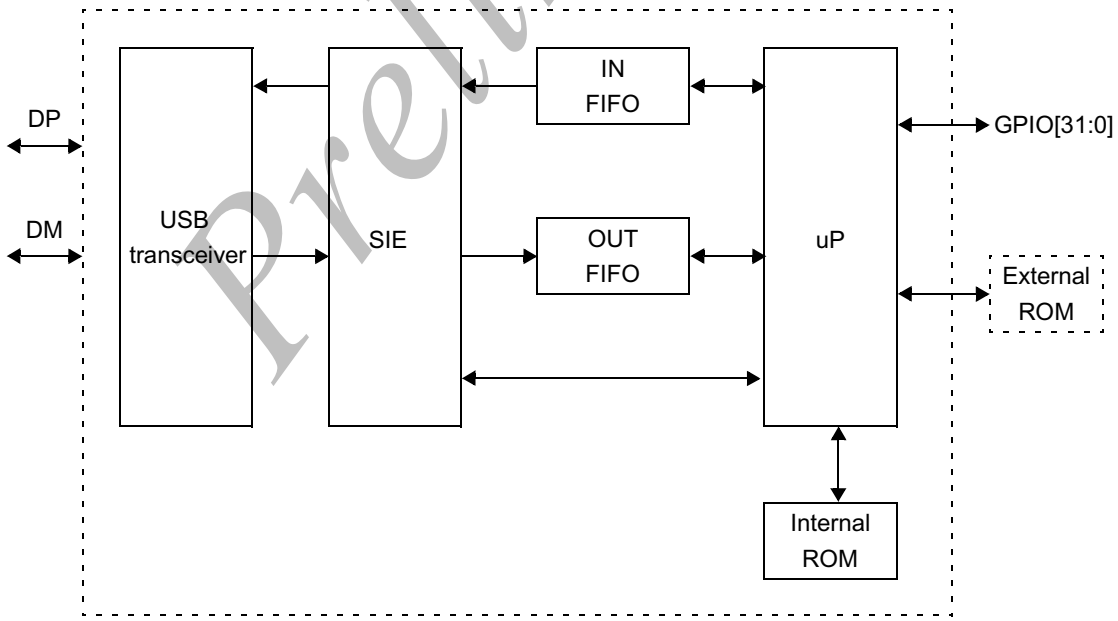
FEATURES

- Combined with application specific firmware, this chip can be configured to support
  1. USB to IDE/ATAPI peripheral devices, including CDROM, CDR/RW, HDD, ZIP drivers, LS120, Compact Flash, Smart Media cards, Disk on chip, etc.
  2. USB to parallel port including SPP, EPP, ECP
  3. USB to serial port

FEATURES (continued)

- Four endpoints (CONTROL, INTERRUPT, BULK-IN and BULK-OUT) are implemented
- FIFO in each of IN and OUT endpoint is to support maximum bulk size (64 bytes)
- Embedded microcontroller is responsible for executing USB and device dependent commands
- Hardware driven interrupt improves latency and efficiency
- 16K x 14 internal metal programmable ROM to meet various application demand
- Accessible external memory provides viable development tool
- Built-in USB transceiver
- 4MHz crystal input with internal 12X multiplier
- Optional serial EEPROM to store customized data
- 3.3 Volt power with 5 Volt tolerant I/O
- Low power with 0.35 µm technology
- 100-pin LQFP package

BLOCK DIAGRAM



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PIN CONNECTION DIAGRAM

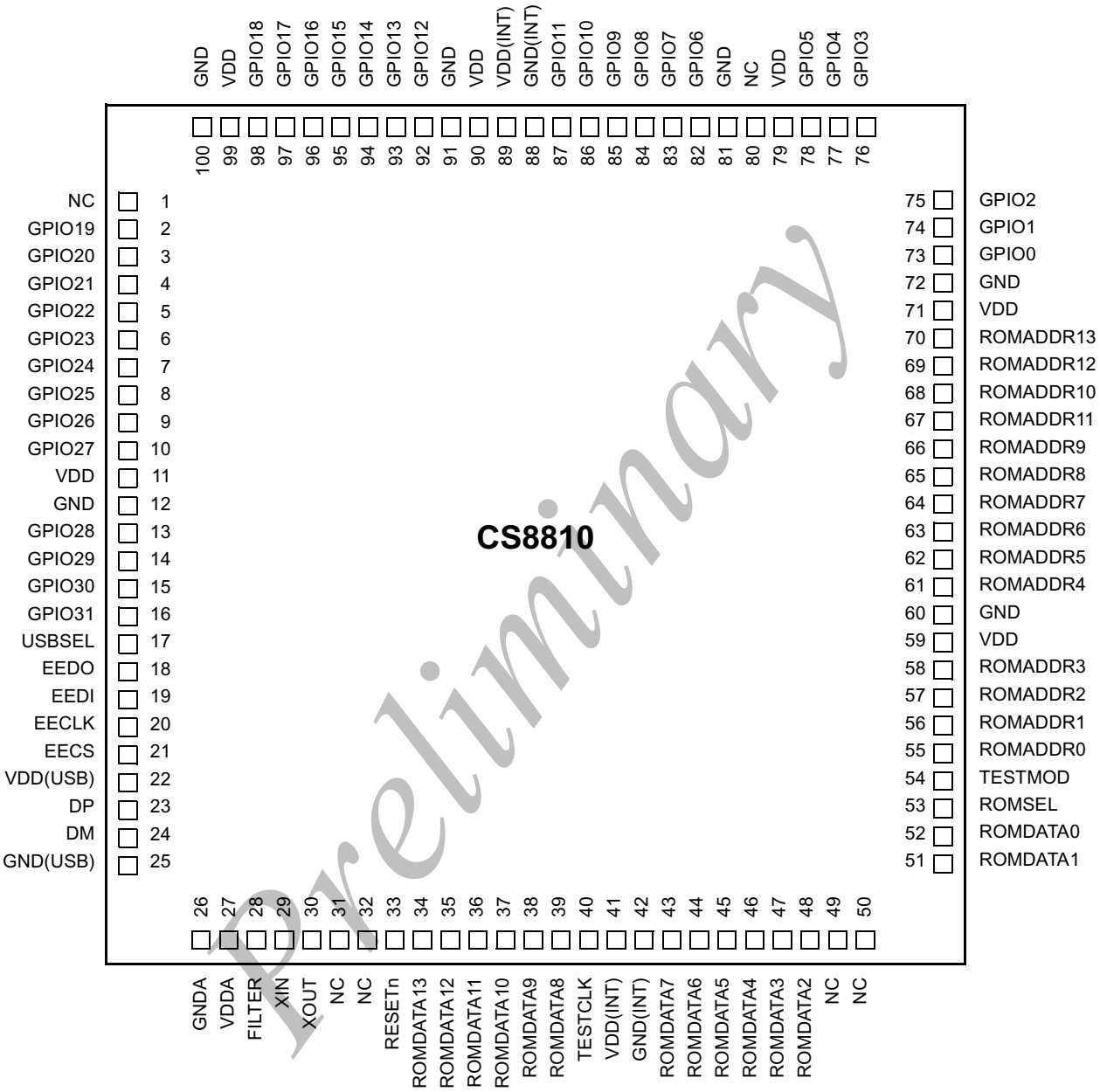


Figure-1 100-pin LQFP

PIN DESCRIPTION

Name	I/O	Pin	Description
USB	4 pins		
XIN	I	29	Crystal Input
XOUT	O	30	Crystal Output
DP	I/O	23	Data Plus of internal USB transceiver
DM	I/O	24	Data Minus of internal USB transceiver
OUSBDP	O	9	Output to DP to external USB transceiver
OUSBDM	O	10	Output to DM to external USB transceiver
OUSBEN	O	16	Output enable to external USB transceiver
IUSBDP	I	14	Input from DP of external USB transceiver
IUSBDM	I	13	Input from DM of external USB transceiver
IUSBDATA	I	15	Data from differential output of external USB transceiver
USBSEL	I	17	0: internal USB transceiver 1: external USB transceiver
EEPROM	4 pins		
EEDI	I	19	Data Input from EEPROM
EEDO	O	18	Data Output to EEPROM
EECLK	O	20	EEPROM Clock
EECS	O	21	EEPROM Chip Select
ROM	29 pins		
ROMADDR[13:0]	0	70-69, 67, 68, 66-61, 58-55	External ROM Address
ROMDATA[13:0]	I	34-39, 43-48, 51-52	External ROM Data
ROMSEL	I	53	0: internal ROM 1: external ROM
MISC.	4 pins		
TESTMOD	I	54	0: normal 1: internal ROM testing
RESETn	I	33	Power-on reset, active low
FILTER		28	Low pass filter for PLL
TESTCLK	I/O	40	Test mode clock Output only if internal PLL is used
DEVICE I/O	32 pins		
GPIO[31:0]	I/O	16-13, 10-2, 98-92, 87-82, 78-73	
POWER	10 pins		
VDD (USB)		22	
VDD (ANALOG)		27	
VDD (INT)		41, 89	
VDD (OB)		11, 59, 71, 79, 90, 99	
GROUND	10 pins		

Name	I/O	Pin	Description
GND (USB)		25	
GND (ANALOG)		26	
GND (INT)		42, 88	
GND (OB)		12,60, 72, 81, 91, 100	

Recommended pin mapping

PIN	Port	IDE Interface	CF Interface	SPP	EPP	ECP	Serial
0	A0	IORDn	IORDn	STROBEn	WRITEn	HOSTCLK	TD
	A1	IOWRn	IOWRn	AUTOLFn	DATASTRn	HOSTACK	RTS
	A2	CS0n	CS0n				
	A3	CS1n	CS1n				
	A4	A0	A0	ACKn	INTR	PRPHCLK	DTR
	A5	A1	A1	BUSYn	WAIT	PRPHACK	
	A6	A2	A2				
	A7	IDERSTn	IDERSTn				
	B0	DATA[0]	DATA[0]	DATA[0]	DATA[0]	DATA[0]	RD
	B1	DATA[1]	DATA[1]	DATA[1]	DATA[1]	DATA[1]	CTS
	B2	DATA[2]	DATA[2]	DATA[2]	DATA[2]	DATA[2]	DSR
	B3	DATA[3]	DATA[3]	DATA[3]	DATA[3]	DATA[3]	DCD
	B4	DATA[4]	DATA[4]	DATA[4]	DATA[4]	DATA[4]	RI
	B5	DATA[5]	DATA[5]	DATA[5]	DATA[5]	DATA[5]	
	B6	DATA[6]	DATA[6]	DATA[6]	DATA[6]	DATA[6]	
	B7	DATA[7]	DATA[7]	DATA[7]	DATA[7]	DATA[7]	
	C0	DATA[8]	DATA[8]	PAPEREND		XFLAG	
	C1	DATA[9]	DATA[9]	SELECT		ACKRVn	
	C2	DATA[10]	DATA[10]	ERRORn		PRPHREQ	
	C3	DATA[11]	DATA[11]				
	C4	DATA[12]	DATA[12]				
	C5	DATA[13]	DATA[13]	INITn	ADDSTRn	RVREQn	
	C6	DATA[14]	DATA[14]	SELPTRn	RESETn	ACT1284	
	C7	DATA[15]	DATA[15]	BUFDIR	BUFDIR	BUFDIR	
	D0	INTQ	INTQ				
	D1	IORDY	IORDY				
	D2	IO16n	IO16n				
	D3		CD1n				
	D4		CD2n				
	D5	VDD	VDD				
	D6	GND	GND				
	D7	INTQ	INTQ				

Italic: Bidirectional

Shaded: Input only

Others: Output only

FUNCTIONAL DESCRIPTION

USB transceiver

It converts between digital and analog domain of USB signals. Either internal or external USB transceiver can be selected. Internal USB transceiver only supports full speed mode.

SIE

USB Serial Interface Engine takes charge of all digital functions and interfaces with transceiver. Its main tasks include serializing and de-serializing bit string. To ensure data integrity, bit stuffing and de-stuffing is handled inside of SIE. After receiving interrupt and checking status flag, microcontroller executes appropriated instructions accordingly.

IN FIFO

It is a 16-byte deep FIFO, in which data are moved by microcontroller. SIE serializes byte data then sends to USB transceiver.

OUT FIFO

It is a 16-byte deep FIFO, in which data are de-serialized from USB SIE. Microcontroller moves data out from OUT FIFO.

Microcontroller

An embedded microcontroller plays a critical role in the chip. Its tasks includes:

1. interprets USB command and interrupt of SIE
2. moves data between FIFO and device
3. moves data of control and interrupt packet
4. interfaces with EEPROM

If any CRC error occurs during data transfer from device to USB, microcontroller has to send the data of original bulk again.

ROM

ROM mainly contains instruction sets of microcontroller. Either internal or external ROM can be selected through ROMSEL pin. In the stage of application specific firmware development, external ROM provides a very useful environment.

USB Device Endpoint Operation

Endpoint 0

Endpoint 0 is a control endpoint which responses USB standard and vendor specific commands. It is configured as a maximum eight bytes access.

Endpoint 2

Endpoint 2 is an interrupt IN endpoint, which returns status every programmable polling interval. It is configured as an eight bytes access.

Endpoint 3

Endpoint 3 is a bulk OUT endpoint, in which data is from USB host to device. After data are stored from EP3 FIFO, microcontroller moves them into internal SRAM until whole USB packet (64 bytes) is done. However, data will not be sent to device until handshake stage (CRC checking) passes.

Endpoint 4

Endpoint 4 is a bulk IN endpoint, which is responsible for data from device to USB host. The length of bulk can be programmed as 8, 16, 32 or 64 bytes. Microcontroller takes responsibility of transferring data from device to EP4 FIFO.

USB Generic Commands:

1. Get Device Status

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
80h	00	00	00	00	00	02h	00

data stage:

D[7:0]	D[15:8]
D:[7:2]: 6'b00_0000D D:[1]:1'b1: remote wakeup enable D:[0]:1'b1, self powered	00

2. Get Interface Status

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
81h	00	00	00	00	00	02h	00

data stage:

D[7:0]	D[15:0]
00	00

3. Get EP0 Status

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
82h	00	00	00	80h or 00	00	02h	00

data stage:

D[7:0]	D[15:8]
D:[7:6]: 7'b000_0000 1: EP0 Stalled	00

4. Get EP2 Status

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
82h	00	00	00	82h	00	02h	00

data stage:

D[7:0]	D[15:8]
D:[7:6]: 7'b000_0000 1: EP2 Stalled	00

5. Get EP3 Status

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
82h	00	00	00	03h	00	02h	00

data stage:

D[7:0]	D[15:0]
D:[7:6]: 7'b000_0000 1:EP3 Stalled	00

6. Get EP4 Status

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
82h	00	00	00	84h	00	02h	00

data stage:

D[7:0]	D[15:0]
D:[7:6]: 7'b000_0000 1: EP4 Stalled	00

7. Get Device Descriptor (Total 18 bytes)

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
80h	06h	00	01h	00	00	12h	00

data stage:

Offset0 (Length)	Offset1 (Type)	Offset2 (USB Minor Rel. No)	Offset3 (USB Major Rel. No)	Offset4 (Class)	Offset5 (Subclass)	Offset6 (protocol)	Offset7 (EP0 MaxSize)
12h	01h	10h	01h	00h	00	00	08h

Offset8 (Vendor ID low)	Offset9 (Vendor ID high)	Offset10 (Product ID low)	Offset11 (Product ID high)	Offset12 (Release ID low)	Offset13 (Release ID high)	Offset14 (Index of Manufacturer String)	Offset15 (Index of Product String)
22h	0ah	14h	60h	02h	01h	01h	02h

Offset16 (Serial no.)	Offset17 (no. of configuration)
03h	01h

Note: Some of the data can be read from EEPROM where Serial EEPROM is optional for CS8810.

Note: The A1 version has Release ID 0102h and the B0 version has Release ID 0201h.

8. Get Configuration Descriptor (Total 39 bytes)

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
80h	06h	00	02h	00	00	27h	00

data stage:

configuration descriptor:

Offset0 (Length)	Offset1 (Type)	Offset2 (Total length low)	Offset3 (Total length high)	Offset4 (NumInterface)	Offset5 (ConfigNo)	Offset6 (StringIndex)	Offset7 (Attribute)
09h	02h	27h	00	01h	01h	00	A0h

Offset8 (MaxPower)
30h

interface 0 descriptor:

Offset0 (Length)	Offset1 (Type)	Offset2 (InterfaceNum)	Offset3 (AltInterface)	Offset4 (NumEP)	Offset5 (Interface Class)	Offset6 (Interface Subclass)	Offset7 (Interface Protocol)
09h	04h	00	00	03h	00h*	00h*	00

Offset8 (StringIndex)
00

Note: The numbers there are for CS6565.

EP2 descriptor:

Offset0 (Length)	Offset1 (Type)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPacket Size Lo)	Offset5 (MaxPacket Size High)	Offset6 (Interval)
07h	05h	82h	03h interrupt	08h	00	01h

EP3 descriptor:

Offset0 (Length)	Offset1 (Type)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPacket Size Lo)	Offset5 (MaxPacket Size High)	Offset6 (Interval)
07h	05h	03h	02h bulk	40h	00	00

EP4 descriptor:

Offset0 (Length)	Offset1 (Type)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPacket Size Lo)	Offset5 (MaxPacket Size High)	Offset6 (Interval)
07h	05h	84h	02h bulk	40h	00	00

Note: Some of the data can be read from EEPROM where Serial EEPROM is optional for CS8810.

9. Get Configuration

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
80h	08h	00	00	00	00	01h	00

data stage:

Offset0 (Configure Value)
00 or 01h

Note: If the returned configuration value is 00h, it means the device is in address state. If the returned value is 01h, it means the device had been configured.

10. Get Interface

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
81h	0Ah	00	00	00	00	01h	00

data stage:

Offset0 (AltInterface)
00

11. Set Address

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
00	05h	address	00	00	00	00	00

12. Set Configuration

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
00	09h	config	00	00	00	00	00

config=0x00h: address state
config=0x01h: configured state

13. Set Interface

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
01h	0Bh	00	00	00	00	00	00

CPU has to make sure the interface number and alternate interface are 0.

14. Set Endpoint Stall

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
02h	03h	00	00	EP*	00	00	00

Note: EP= 00h: Stall endpoint 0

Note: EP=82h: Stall endpoint 2

Note: EP=03h: Stall endpoint 3

Note: EP=84h: Stall endpoint 4

15. Clear Endpoint Stall

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
02h	01h	00	00	EP*	00	00	00

Note: EP= 00h: Clear endpoint 0 stall

Note: EP=82h: Clear endpoint 2 stall

Note: EP=03h: Clear endpoint 3 stall

Note: EP=84h: Clear endpoint 4 stall

16. Set Remote Wakeup Feature

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
00	03h	01h	00	00	00	00	00

17. Clear Remote Wakeup Feature

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
00	01h	01h	00	00	00	00	00

18. Get String Descriptor 0, Language ID Code

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
80h	06h	00	03h	00	00	04h	00

data stage:

Offset0 (Length)	Offset1 (Type)	Offset2 (LangID lo)	Offset3 (LangID hi)
04h	03h	09h	04h

19. Get String Descriptor 1, Manufacture String

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
80h	06h	01h	03h	09h	04h	TBD	00

data stage:

Offset0 (Length)	Offset1 (Type)	Offset2 (String)
TBA	03h	Copy from EEPROM or hard code

20. Get String Descriptor 2, Product String

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
80h	06h	02h	03h	09h	04h	TBD	00

data stage:

Offset0 (Length)	Offset1 (Type)	Offset2 (String)
TBA	03h	Copy form EEPROM or hard code

21. Get String Descriptor 3, Serial No.

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
80h	06h	03h	03h	09h	04h	TBD	00

data stage:

Offset0 (Length)	Offset1 (Type)	Offset2 (String)
TBA	03h	Copy from EEPROM or hard code

Vendor Specific Commands

1. Get USB Single Register Data

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
C0h	F0h	00	00	RegIdx	00	01h	00

data stage:

Offset0
Reg[Regidx]

Note: Fetch single byte of data from USB register. This command is intended for internal debugging use.

2. Get EEPROM Single Word Memory Data

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
C0h	F2h	00	00	RegIdx	00	02h	00

data stage:

Offset0	Offset1
Low Byte MEM[Regidx]	High Byte MEM[RegIdx]

3. Get EEPROM Programming Status

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
C0h	F4h	00	00	00	00	01h	00

data stage:

Offset0
Status

Fetch single byte of EEPROM programming status. If status=0, the programming is not finished yet.

4. Get EEPROM Validation Status

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
C0h	F6h	00	00	00	00	01h	00

data stage:

Offset0
Status

Fetch single byte of EEPROM validation status. If status=1, the content of EEPROM consists of correct signature and valid check sum.

5. Set USB Registers Single Write

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
40h	F1h	AndVal	OrVal	RegIdx	00	00	00

Note: NewValue= ((OldValue and AndVal) or OrVal) and This feature is provided to set or clear register value more easily.

Note: For B0 version, this vendor command can also be issued as 40_F0_AndVal_OrVal_RegIdx_00_00_00.

6. Set EEPROM Multiple Memory Data

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
40h	F3h	DataLow	DataHigh	RegIdx	00	00	00

Note: This vendor command can also be issued as 40_F2_DataLow_DataHigh_RegIdx_00_00_00 for B0 version.

7. Erase all EEPROM data

setup stage:

bmReq	bReq	wValue		wIndex		wLength	
40h	F5h	00	00	00	00	00	00

Note: All contents in EEPROM will be erased and filled with 0xff.

Note: For B0 version, this vendor command can also be issued as 40_F4_00_00_00_00_00_00.

List of Command and Status Registers.

Register Address	Register Names	Register Description
00h	IntEnReg1	Interrupt Enable Register 1
01h	IntEnReg2	Interrupt Enable Register 2
02h	IntStsReg1	Interrupt Status Register 1
03h	IntStsReg2	Interrupt Status Register 2
04h	EP0TxDataReg	EP0 Transmit FIFO Data Register
05h	EP0RxDataReg	EP0 Receive FIFO Data Register
06h	EP2DataReg	EP2 FIFO Data Register
07h	EP3DataReg	EP3 FIFO Data Register
08h	EP4DataReg	EP4 FIFO Data Register
09h	EP0RxCntReg	EP0 Receive FIFO Count Register
0Ah	EP3CntReg	EP3 FIFO Count Register
0Bh	EPStsReg	Endpoint Status Register
0Ch	EP3WtrMrkReg	EP3 FIFO Water Mark Register
0Dh	EP4WtrMrkReg	EP4 FIFO Water Mark Register
0Eh	EP3MaxPktSzReg	EP3 Maximum Packet Size Register
0Fh	HskStsReg	Handshake Status Register
10h	EP0StsReg	EP0 Status Register
11h	DevAddrReg	Device Address Value Register
12h	FrmNumReg1	Frame Number MSB Register
13h	FrmNumReg2	Frame Number LSB Register
14h	EP3ReqCntReg	EP3 Request Count Register
15h	EP4ReqCntReg	EP4 Request Count Register
16h	EP3NakCntReg	EP3 NAK Count Register
17h	EP4NakCntReg	EP4 NAK Count Register
18h	EP4CntReg	EP4 FIFO Count Register

Address 00h: Interrupt Enable Register 1 (IntEnReg1)

Bits	Description	Read	Write	Default
7	EP4 Interrupt Enable. When set, this bit enables a local interrupt to be set when EP4 bulk data packet has been sent by the device.	Yes	Yes	0
6	EP3 Interrupt Enable. When set, this bit enables a local interrupt to be set when EP3 bulk data packet has been received by the device.	Yes	Yes	0
5	EP2 Interrupt Enable. When set, this bit enables a local interrupt to be set when EP2 interrupt data packet has been sent by device to Host.	Yes	Yes	0
4	EP4 FIFO Water Mark Interrupt Enable. When set, this bit enables a local interrupt to be set when EP4 FIFO falls below the corresponding water mark.	Yes	Yes	0
3	EP3 FIFO Water Mark Interrupt Enable. When set, this bit enables a local interrupt to be set when EP3 FIFO crosses the corresponding water mark.	Yes	Yes	0
2	SETUP Interrupt Enable. When set, this bit enables a local interrupt to be set when Host transmits a setup packet.	Yes	Yes	0
1	EP0 Tx Interrupt Enable. When set, this bit enables a local interrupt to be set when EP0 data packet has been sent by the device to Host successfully.	Yes	Yes	0
0	EP0 Rx Interrupt Enable. When set, this bit enables a local interrupt to be set when EP0 data packet has been received by the device from Host successfully.	Yes	Yes	0

Address 01h: Interrupt Enable Register 2 (IntEnReg2)

Bits	Description	Read	Write	Default
7	EP0 Error. When set, this bit enables a local interrupt to be set when there is a likelihood of EP0 error condition.	Yes	Yes	0
6	USB Reset Interrupt Enable. When set, this bit enables a local interrupt to be set when Host transmits reset special signal to the device.	Yes	Yes	0
5	SOF Interrupt Enable. When set, this bit enables a local interrupt to be set when a Start Of Frame packet is received by the device.	Yes	Yes	0
4	USB Suspend Interrupt Enable. When set, this bit enables a local interrupt to be set when Host does not transmit any signals to the device for more than 5 ms.	Yes	Yes	0
3	Reserved			0
2	EP4 Data Toggle Mode. When set, this bit resets the Data Toggle bit to zero at the end of a USB transaction from EP4. When cleared the Data Toggle bit strictly toggles with every successful USB transaction.	Yes	Yes	0
1	EP3 Data Toggle Mode. When set, this bit resets the Data Toggle bit to zero at the end of a USB Transaction from EP3. When cleared the Data Toggle bit strictly toggles with every successful USB transaction.	Yes	Yes	0

Bits	Description	Read	Write	Default
0	EP2 Data Toggle Mode. When set, this bit resets the Data Toggle bit to zero at the end of a USB Transaction from EP2. When cleared the Data Toggle bit strictly toggles with every successful USB transaction.	Yes	Yes	0

Address 02h: Interrupt Enable Register 1(IntStsReg1)

Bits	Description	Read	Write	Default
7	EP4 Interrupt Status. This bit indicates when EP4 bulk data packet has been sent by device. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0
6	EP3 Interrupt Status. This bit indicates when a EP3 bulk data packet has been received by device. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0
5	EP2 Interrupt Status. This bit indicates when the EP2 interrupt data packet has been sent by device to Host successfully when EP2 Toggle Mode bit is 0 otherwise this bit will be set for every transaction on this EP irrespective of handshake from Host. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0
4	EP4 FIFO Water Mark Interrupt Status. This bit is set when the number of bytes in the EP4 FIFO is equal to the EP4 FIFO Water Mark, the another byte is sent to the Host from the FIFO. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0
3	EP3 FIFO Water Mark Interrupt Status. This bit is set when the number of bytes in the EP3 FIFO is equal to the EP3 FIFO Water Mark, and another byte is received from the Host into the FIFO. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0
2	SETUP Interrupt Status. This bit indicates when a setup transaction is received by device from Host. This status bit is cleared by writing 1. Note: It is recommended that the firmware should clear this bit and then read the EP0 receive FIFO data.	Yes	Yes/CLR	0
1	Misc Interrupt Enable. This bit indicates when other miscellaneous interrupts have been set. It is OR-ed signal from the bits in Interrupt Status Registers 2. CPU has to look into Interrupt Status Register 2 to see exactly which interrupt has been set.	Yes	No	0
0	Reserved			0

Address 03h: Interrupt Status Register 2 (IntStsReg2)

Bits	Description	Read	Write	Default
7	EP0 Transmit Interrupt Status. This bit indicates when a EP0 data packet has been sent by device to Host successfully. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0
6	EP0 Receive Interrupt Status. This bit indicates when a EP0 data packet has been received by device from Host successfully. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0

Bits	Description	Read	Write	Default
5	EP0 Error. This bit indicates when a EP0 error condition signal is detected by device. This status bit is cleared by writing 1. During a control transfer, when a direction change is detected by device and if CPU has not set the data stage complete bit, then the USB IP sets this bit. This bit is also set by the IP when the host requests for more than the pre-negotiated data in the control read transfer.	Yes	Yes/CLR	0
4	USB Reset Interrupt Status. This bit indicates when a reset signal has been received by device from Host. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0
3	USB Suspend Interrupt Status. This bit indicates when a suspend signal has been received by device from Host. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0
2	SOF Interrupt Status. This bit indicates when a Start of Frame packet has been received by device. This status bit is cleared by writing a 1.	Yes	Yes/CLR	0
1-0	Reserved			0

Address 04h: EP0TxDataReg

Bits	Description	Read	Write	Default
7-0	EP0 Transmit FIFO Data Register. This port is used for writing data to the EP0 Transmit Data FIFO. The FIFO is read by Host using control transfer.	No	Yes	0

Address 05h: EP0RxDataReg

Bits	Description	Read	Write	Default
7-0	EP0 Receive FIFO Data Register. This port is used for reading data to the EP0 Transmit Data FIFO. The FIFO is written by Host using control transfer.	Yes	No	0

Address 06h: EP2DataReg

Bits	Description	Read	Write	Default
7-0	EP2 FIFO Data Register. This port is used for writing data to the EP2 FIFO. The FIFO is read by Host using interrupt transfer.	No	Yes	0

Address 07h: EP3DataReg

Bits	Description	Read	Write	Default
7-0	EP3 FIFO Data Register. This port is used for reading data from the EP3 FIFO. The FIFO is written by Host using bulk transfer.	Yes	No	0

Address 08h: EP4DataReg

Bits	Description	Read	Write	Default
7-0	EP4 FIFO Data Register. This port is used for writing data to the EP4 FIFO. The FIFO is read by Host using bulk transfer.	No	Yes	0

Address 09h: EP0RxCntReg

Bits	Description	Read	Write	Default
7-0	EP0 Receive FIFO Count. This register returns the count of number of bytes in EP0 receive FIFO containing valid entries at the end of the current valid data packet transaction. Values range from 0 (empty) to 8 (full).	Yes	No	0

Address 0Ah: EP3CntReg

Bits	Description	Read	Write	Default
7-0	EP3 FIFO Count. This register returns the count of number of bytes in EP3 FIFO containing valid entries at the end of the current valid data packet transaction. Values range from 0 (empty) to 16 (full)	Yes	No	0

Address 0Bh: Endpoint Status Register (EPStsReg)

Bits	Description	Read	Write	Default
7	EP2 FIFO Data Valid. If set, this bit allows data in EP2 FIFO to be read by the next read from the Host. This bit is automatically cleared by Host read.	Yes	Yes	0
6	EP2 Stall. If this bit is set, Host bulk reads from the EP2 FIFO will result in a STALL acknowledge by the USB IP. No data will be returned to the Host.	Yes	Yes	0
5	EP3 Maximum packet Size Error. This bit is set by USB IP when it detects a packet whose length is more than the maximum packet size for bulk transfer.	Yes	No	0
4	EP3 Stall. If this bit is set, Host bulk writes to the EP3 FIFO will result in a STALL acknowledge by the USB IP. No data will be returned to the Host.	Yes	Yes	0
3	EP4 FIFO Data Transfer Complete. CPU sets this bit after completing the total packet transfer from its memory to the EP4 FIFO, for the cases where the packet size is greater than the FIFO size, For cases where the packet size is less than or equal to the FIFO size it is set high by CPU along with data transfer to EP4 FIFO. USB IP resets this bit after completion of the current data transaction to the Host.	No	Yes	0
2	EP4 FIFO Data Valid. If set, this bit allows the data in the EP4 FIFO to be read by the next read from the Host. This bit is automatically cleared by a Host read.	Yes	Yes	0
1	EP4 Stall. If this bit is set, Host bulk reads from the EP4 FIFO will result in a STALL acknowledge by the USB IP. No data will be returned to the Host.	Yes	Yes	0
0	reserved			0

Address 0Ch: EP3WtrMrkReg

Bits	Description	Read	Write	Default
7-0	EP3 FIFO Water Mark Register. This register determines the threshold value at which the EP3 FIFO Water Mark Interrupt Status is set. The value is set by CPU depending on the configuration selected.	Yes	Yes	08h

Address 0Dh: EP4WtrMrkReg

Bits	Description	Read	Write	Default
7-0	EP4 FIFO Water Mark Register. This register determines the threshold value at which the EP4 FIFO Water Mark Interrupt Status is set. The value is set by CPU depending on the configuration selected.	Yes	Yes	08h

Address 0Eh: EP3MaxPktSzReg

Bits	Description	Read	Write	Default
7-0	EP3 Maximum Packet Size Register. This register contains the value of the maximum packet size EP3 can handle. The actual value is taken to be eight times the value stored in this register. A value of 0 represents a Maximum Packet Size of 8 bytes, a value of 1 represents 16 bytes and so on.	Yes	Yes	07h

Address 0Fh: Handshake Status Register (HskStsReg)

Bits	Description	Read	Write	Default
7	EP4 ACK. The last data packet transmitted by EP4 was successfully acknowledged with an ACK from the Host. Writing a 1 clears this bit. Writing a 0 has no effect.	Yes	Yes/CLR	0
6	EP3 ACK. The last data packet received by EP3 was successfully acknowledged with an ACK. Writing a 1 clears this bit. Writing a 0 has no effect.	Yes	Yes/CLR	0
5	EP4 FIFO Flush. Writing a 1 to this bit causes the EP4 FIFO to be flushed. Writing a 0 has no effect. Reading this bit always returns 0.	Yes	Yes/CLR	0
4	EP3 FIFO Flush. Writing a 1 to this bit causes the EP3 FIFO to be flushed. Reading this bit always returns 0. Writing a 0 has no effect.	Yes	Yes/CLR	0
3	EP2 FIFO Flush. Writing a 1 to this bit causes the EP2 FIFO to be flushed. Writing a 0 has no effect. Reading this bit always returns 0.	Yes	Yes/CLR	0
2	EP0 Tx FIFO Flush. Writing a 1 to this bit causes the EP0 transmit FIFO to be flushed. Reading this bit always returns 0. Writing a 0 has no effect.	Yes	Yes/CLR	0
1	Status Stage. This bit is set by the USB IP, when the host changes the direction in the data stage of a control transfer before CPU sets the control transfer complete bit, i.e. when host initiates the status stage prematurely. This bit is cleared by CPU by writing a 1 in this location.	Yes	Yes/CLR	0
0	Suspend Control. If set, this bit indicates that there is a pending Suspend request from the Host. Writing a 1 clears this bit and causes the USB IP to enter suspended mode.	Yes	Yes/CLR	0

Address 10h: EP0 Status Register (EP0StsReg)

Bits	Description	Read	Write	Default
7	EP0 Maximum Packet Size Error. This bit is set by the USB IP when it detects a packet for EP0 whose length is more than the maximum packet size.	Yes	No	0

Bits	Description	Read	Write	Default
6	EP0 Tx FIFO Data Valid. If set, this bit allows data in the EP0 TX FIFO to be read by the next read from the Host. This bit is automatically cleared by Host read.	Yes	Yes	0
5	EP0 Stall. If this bit is set, the control transfer data phase writes or reads to the EP0 FIFO will result in a STALL acknowledge by the USB IP.	Yes	Yes	0
4	Control Transfer Complete. CPU set this bit after successful completion of data phase of a control transfer. USB IP resets this bit after completing the status phase of transfer.	No	Yes	0
3	Control Transfer In Progress. USB IP sets this bit when a valid SETUP token is received. USB IP resets the bit after completion of the control transfer.	Yes	No	0
2	Reserved			
1	USB Enable. CPU sets this bit after completing the power on reset or USB IP reset initialization, when all the default values of registers are written by CPU. Device listens to USB traffic only after this bit is set.	Yes	Yes	0
0	Device configured. CPU sets this bit after initial configuration of the device is completed by the Host and the Device moves to USB defined CONFIGURED state. Before setting the bit, CPU writes the Host assigned Device address value, EP data transfer types, maximum data packet sizes into the respective registers. Only after CPU sets this bit, the device responds to USB transactions to EPs other than EP0. When this bit is reset the USB IP responds to USB transactions to EP0. This bit is reset on power-on, USB IP reset and USB reset.	Yes	Yes	0

Address 11h: Device Address Register (DevAddrReg)

Bits	Description	Read	Write	Default
7-0	The Address value assigned by Host. This register holds the address for the USB function. During bus enumeration CPU writes in to this register a unique value assigned by Host via SET ADDRESS command. Only the least 7-bits are used.	Yes	Yes	0

Address 12h: Frame Number Register 1 (FrmNumReg1)

Bits	Description	Read	Write	Default
7-3	Reserved	Yes	No	0
2-0	Frame Counter MSB. This register contains the most significant bits of the frame number counter from the most recent SOF packet.	Yes	No	0

Address 13h: Frame Number Register 2 (FrmNumReg2)

Bits	Description	Read	Write	Default
7-0	Frame Counter LSB. This register contains the least significant bits of the frame number counter from the most recent SOF packet.	Yes	No	0

Address 14h: EP3 Request Count Register (EP3RegCntReg)

Bits	Description	Read	Write	Default
7-0	The register counts the number of EP3 request from host within each 1ms interval and is used for statistic purpose. This byte could be sent back as the 5th byte of interrupt transfer for performance tuning.	Yes	No	0

Address 15h: EP4 Request Count Register (EP4RegCntReg)

Bits	Description	Read	Write	Default
7-0	The register counts the number of EP4 request from host within each 1ms interval and is used for statistic purpose. This byte could be sent back as the 6th byte of interrupt transfer for performance tuning.	Yes	No	0

Address 16h: EP3 NAK Count Register (EP3NakCntReg)

Bits	Description	Read	Write	Default
7-0	The register counts the number of EP3 NAK response from host within each 1ms interval and is used for statistic purpose. This byte could be sent back as the 7th byte of interrupt transfer for performance tuning.	Yes	No	0

Address 17h: EP4 NAK Count Register (EP4NAKCntReg)

Bits	Description	Read	Write	Default
7-0	The register counts the number of EP4 request from host within each 1ms interval and is used for statistic purpose. This byte could be sent back as the 8th byte of interrupt transfer for performance tuning.	Yes	No	0

Address 18h: EP4CntReg

Bits	Description	Read	Write	Default
7-0	EP4 FIFO Count. This register returns the count of number of bytes in EP4 FIFO containing valid entries at the end of the current valid data packet transaction. Values range from 0 (empty) to 16 (full).	Yes	No	0

Data Storage Mapping at EEPROM

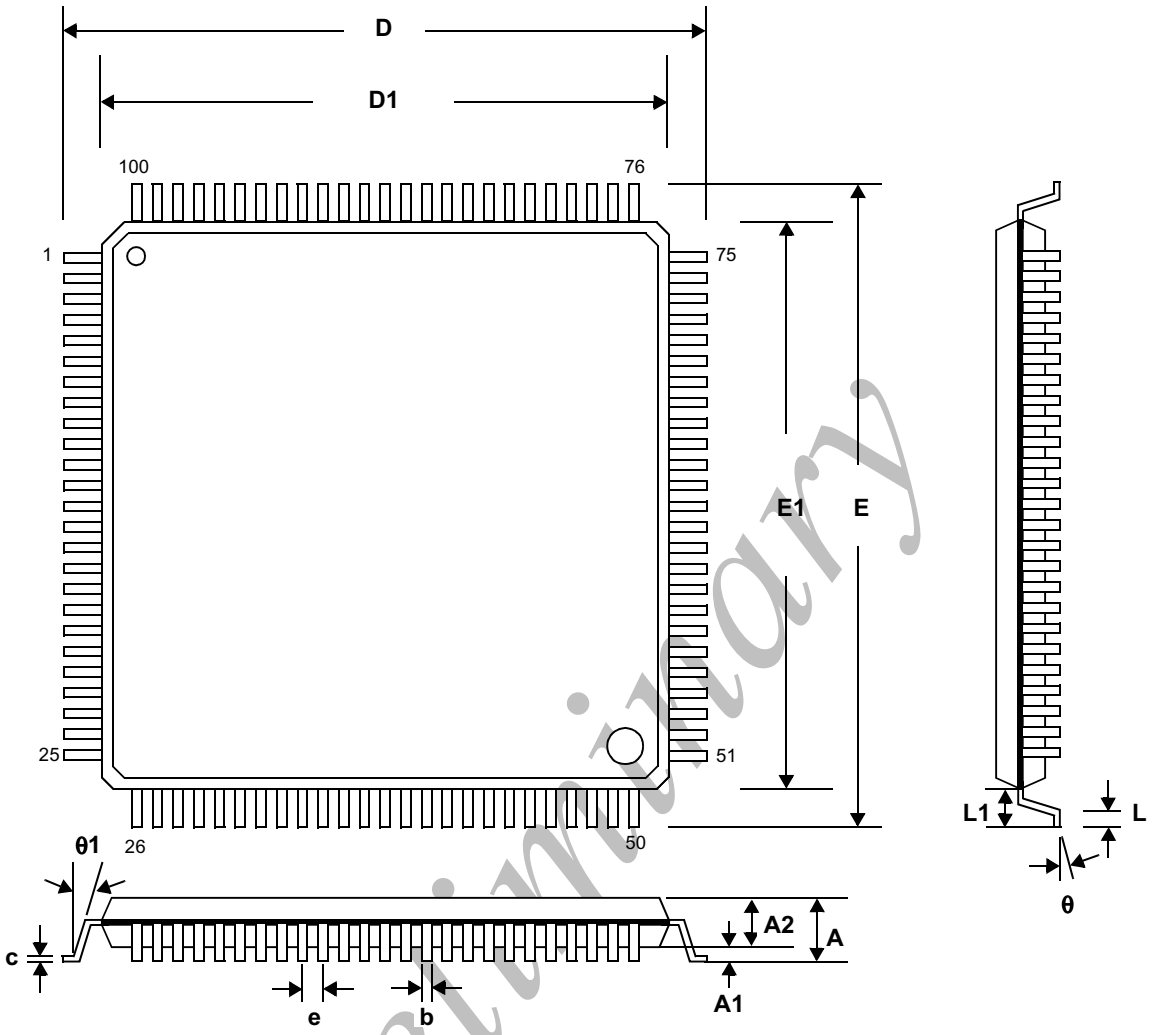
The serial EEPROM used will be Fairchild FM93C46-compatible type.

Individual developer can arbitrarily use the EEPROM contents from address 0x04. The first 4 words are reserved

	Low	High	Low	High	Low	High	Low	High
00h-03h	A5h	5Ah	C3h	3Ch	A5h	40h	ACh	F6h
04h-07h	10	01	00	00	00	08	22	0A
08h-0Bh	14	60	02	01	01	02	03	01
0Ch-0Fh	09	02	27	00	01	01	00	A0
10h-13h	30	09	04	00	00	03	00	00
14h-17h	00	00	07	05	82	03	08	00
18h-1Bh	01	07	05	03	02	40	00	00
1Ch-1Fh	07	05	84	02	40	00	00	00
20h-23h	00	00	00	00	00	00	00	00
24h-27h	00	00	00	00	00	00	00	6C
28h-2Bh	1c	03	43	65	6e	74	75	72
2Ch-2Fh	79	20	53	65	6d	69	2e	00
30h-33h	1e	03	55	53	42	20	43	6f
34h-37h	6e	74	72	6f	6c	6c	65	72
38h-3Bh	0e	03	30	30	30	30	30	30
3Ch-3Fh	00	00	00	00	00	00	00	00

by Century Semiconductor Inc. as signature words. The contents shown here is just an example.

PACKAGE OUTLINE (100-pin LQFP)



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	-	0.20	0.004	-	0.008
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	-	0.50	-	-	0.020	-
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-

APPLICATION CIRCUIT SCHEMATIC

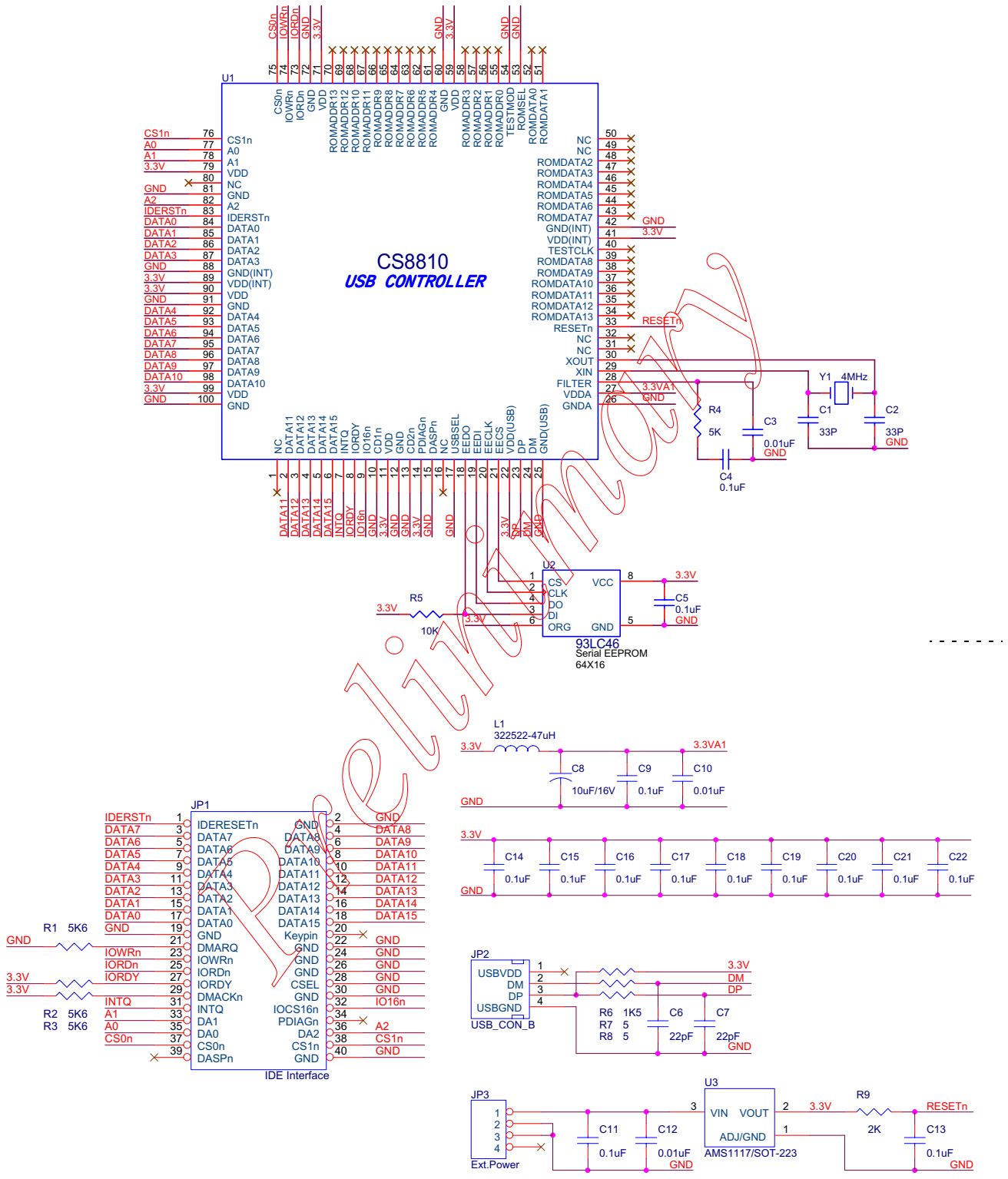


Figure-2 Using 100-pin LQFP package