100 MHz to 6 GHz TruPwr™ Detector

PRELIMINARY TECHNICAL DATA

ADL5500

FEATURES

Calibrated rms response
Excellent temperature stability
Up to 30 dB input range at 2.5 GHz
700 mV rms, 10 dBm, re 50 Ω maximum input
±0.25 dB linear response up to 2.5 GHz
Single-supply operation: 2.7 V to 5.5 V
Low power: 3.3 mW at 3 V supply

APPLICATIONS

Measurement of CDMA, W-CDMA, QAM, other complex modulation waveforms
RF transmitter or receiver power measurement

GENERAL DESCRIPTION

The ADL5500 is a mean-responding power detector for use in high frequency receiver and transmitter signal chains, from 100 MHz to 6 GHz. It is very easy to apply. It requires a single supply only between 2.7 V and 5.5 V and a power supply decoupling capacitor. The input is internally ac-coupled and has an input impedance of 50 Ω. The output is a linear-responding dc voltage with a conversion gain of 7.5 V/V rms. An external low-pass filter network can be added at the output to increase the averaging time constant.

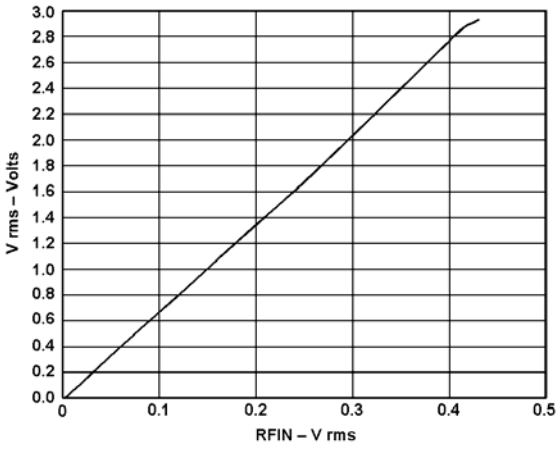

Figure 1. Output vs. Input Level, Supply 3 V, Frequency 1.9 GHz

The ADL5500 is intended for true power measurement of simple and complex waveforms. The device is particularly useful for measuring high crest-factor (high peak-to-rms ratio) signals, such as CDMA and W-CDMA.

The ADL5500 is specified for operation from −40°C to +85°C and is available in 4-lead wafer-level chip scale package, 1.0mm x 1.0 mm. It is fabricated on a proprietary high f_T silicon bipolar process.

FUNCTIONAL BLOCK DIAGRAM

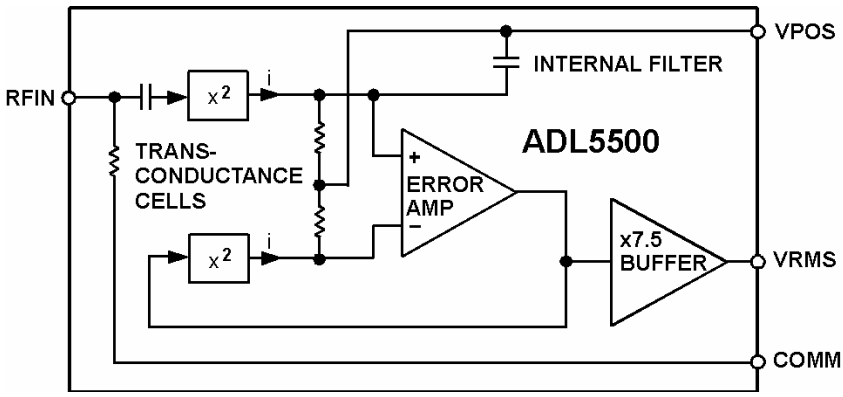

Figure 2.

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SPECIFICATIONS

T_A = 25°C, V_S = 3 V, f_{RF} = 900 MHz, unless otherwise noted.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	(Input RFIN)				
Frequency Range		100		6000	MHz
Linear Response Upper Limit	V_S = 3 V		390		mV rms
	Equivalent dBm, re 50 Ω		4.9		dBm
	V_S = 5 V		660		mV rms
	Equivalent dBm, re 50 Ω		9.4		dBm
Input Impedance			tbd		Ω||pF
RMS CONVERSION	(Input RFIN to Output VRMS)				
Conversion Gain			7.5		V/V rms
Output Intercept			0		V
Dynamic Range[1]	Error Referred to Best Fit Line				
±0.25 dB Error[2]	CW Input, −40°C < T_A < +85°C		14		dB
±1 dB Error	CW Input, −40°C < T_A < +85°C		23		dB
±2 dB Error	CW Input, −40°C < T_A < +85°C		26		dB
	CW Input, V_S = 5 V, −40°C < T_A < +85°C		30		dB
POWER SUPPLIES					
Operating Range	−40°C < T_A < +85°C	2.7		5.5	V
Quiescent Current	0 mV rms at RFIN[3]		1.1		mA

[1] Calculated using linear regression from best fit line.
[2] Compensated for output reference temperature drift.
[3] Supply current is input level dependant.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

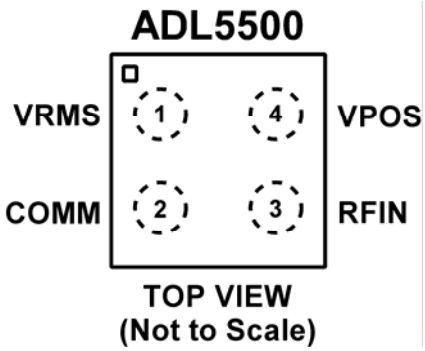

Figure 3. 4-Lead WLCSP

Table 2. Pin Function Descriptions

Pin	Mnemonic	Function
1	VRMS	Output Pin. Near rail-to-rail voltage output with limited current drive capabilities. Expected load >10 kΩ to ground.
2	COMM	Device Ground Pin.
3	RFIN	Signal Input Pin. Internally ac-coupled. Nominal 50 Ω input impedance.
4	VPOS	Supply Voltage Pin. Operational range 2.7 V to 5.5 V.

DEVICE HANDLING

The wafer-level chip scale package consists of solder bumps connected to the active side of the die. The part is lead-free with 95.5% tin, 4.0% silver, and 0.5% copper solder bump composition. The WLCSP package can be mounted on printed circuit boards using standard surface-mount assembly techniques; however, caution should be taken to avoid damaging the die. See the AN-617 application note for additional information. WLCSP devices are bumped die, and exposed die can be sensitive to light condition, which can influence specified limits.

EVALUATION BOARD

Figure 4 shows the schematic of the ADL5500 evaluation board. The layout and silkscreen of the evaluation board layers are shown in Figure 5 to Figure 8. The board is powered by a single supply in the 2.7 V to 5.5 V range. The power supply is decoupled by 100 pF and 0.01 µF capacitors. Table 3 details the various configuration options of the evaluation board.

Problems caused by impedance mismatch may arise using the evaluation board to examine the ADL5500 performance. One way to reduce these problems is to put a coaxial 3 dB attenuator on the RFIN SMA connector. Mismatches at the source, cable, and cable interconnection, as well as those occurring on the evaluation board, can cause these problems.

A simple (and common) example of such a problem is triple travel due to mismatch at both the source and the evaluation board. Here the signal from the source reaches the evaluation board and mismatch causes a reflection. When that reflection reaches the source mismatch, it causes a new reflection, which travels back to the evaluation board, adding to the original signal incident at the board. The resultant voltage varies with both cable length and frequency dependence on the relative phase of the initial and reflected signals. Placing the 3 dB pad at the input of the board improves the match at the board and thus reduces the sensitivity to mismatches at the source. When such precautions are taken, measurements are less sensitive to cable length and other fixture issues. In an actual application when the distance between ADL5500 and source is short and well defined, this 3 dB attenuator is not needed.

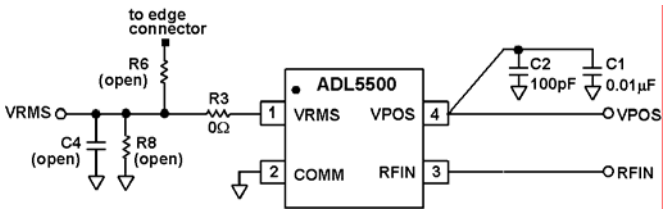

Figure 4. Evaluation Board Schematic

Table 3. Evaluation Board Configuration Options

Component	Function	Default Condition
VPOS, GND	Ground and Supply Vector Pins.	Not Applicable
C1, C2	Power Supply Decoupling. The nominal supply decoupling of 0.01 µF and 100 pF.	C1 = 0.01 µF (Size 0402) C2 = 100 pF (Size 0402)
R3, R8, C4	Output Filtering. The internal 1 kΩ output resistance with the C4 to produce a low pass filter to reduce output ripple. The output can also be scaled down using the resistor divider pads R3 and R8. Also, resistors and capacitors can be placed in C4 and R8 to load test VRMS.	R3 = 0 Ω (Size 0402) R8 = Open (Size 0402) C4 = 10 nF (Size 0402)
R6	Alternate Interface. R6 allows for VRMS to be accessible from the edge connector, which is only used for characterization.	R6 = Open (Size 0402)

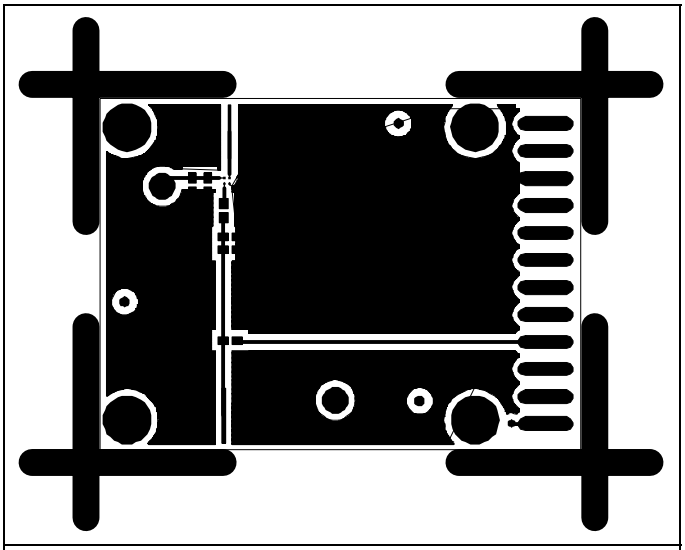

Figure 5. Layout of Component Side (WLCSP)

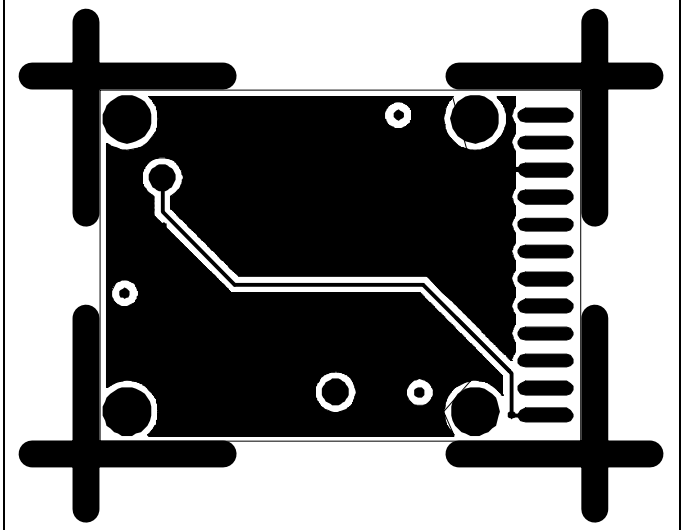

Figure 6. Layout of Circuit Side (WLCSP)

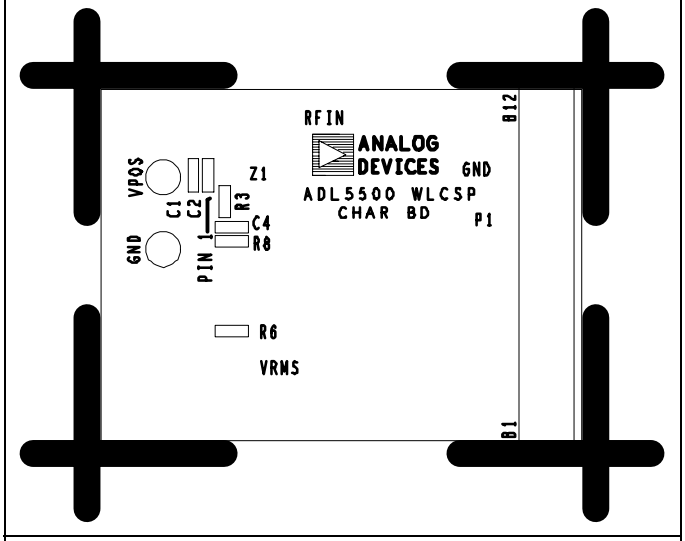

Figure 7. Silkscreen of Component Side (WLCSP)

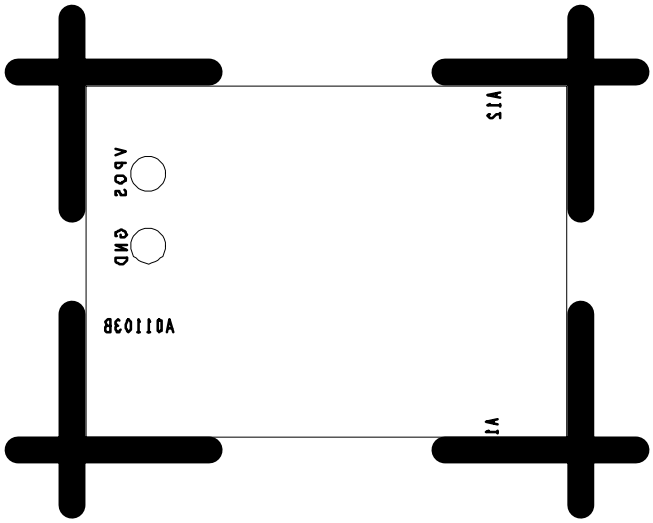

Figure 8. Silkscreen of Circuit Side (WLCSP)

OUTLINE DIMENSIONS

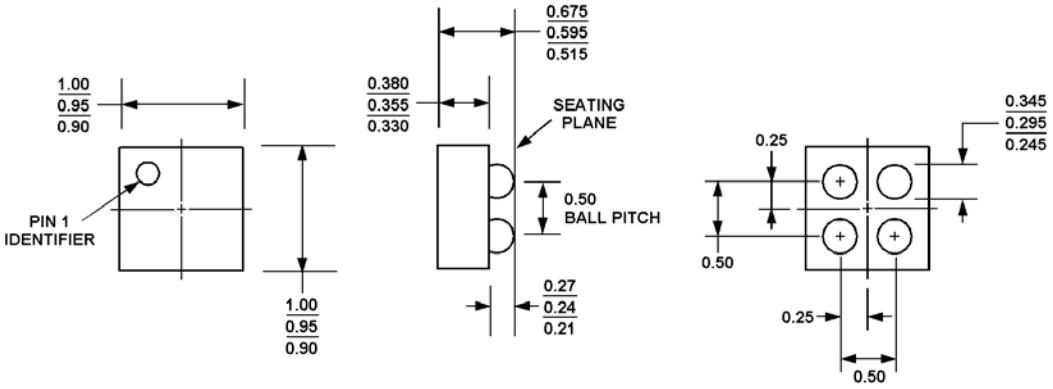

Figure 9. 4-Lead Wafer-level Chip Scale Package
Dimensions shown in mm

ORDERING GUIDE

ADL5500 Products	Temperature Package	Package Description	Package Outline	Branding Information	Ordering Quantity
ADL5500ACBZ-P7[1]	–40°C to +85°C	4-Lead Wafer-level Chip Scale Package, 7″ Pocket Tape and Reel	CB-4	Q06	3000
ADL5500-EVAL		Evaluation Board			

[1] Z = Pb-free part.

NOTES

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