Bookly Micro

8 Megabit (1M x 8) Flash Memory
AC39VF088

DEVICE FEATURES

- **Single Power Supply**
  - Full voltage range: 2.7 to 3.6 volt for both read and write operations
- **Sector-Erase Capability**
  - Uniform 4Kbyte sectors
- **Block-Erase Capability**
  - Uniform 64Kbyte blocks
- **Read Access Time**
  - Access time: 70 and 90 ns
- **Power Consumption**
  - Active current: 15 mA (Typical)
  - Standby current: 4 µA (Typical)
- **Erase Features**
  - Sector-Erase Time: 18 ms (Typical)
  - Block-Erase Time: 18 ms (Typical)
  - Chip-Erase Time: 45 ms (Typical)
  - Byte-Program Time: 14µs (Typical)
  - Chip Rewrite Time: 15 seconds (Typical)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Program or End-of-Erase Detection**
  - Data# Polling
  - Toggle Bit
- **CMOS I/O Compatibility**
- **JEDEC Standard**
  - Pin-out and software command sets compatible with single-power supply Flash memory
- **High Reliability:**
  - Endurance cycles: 100K (Typical)
  - Data retention: 10 years
- **Package Option**
  - 48-pin TSOP

PRODUCT DESCRIPTION

The AC39VF088 is a 1M x 8 CMOS Flash manufactured with Actrans' proprietary Split-Gate Flash memory technology. The AC39VF088 uses 2.7-3.6V power supply for Program and Erase. The AC39VF088 conforms to JEDEC standard pin outs for x8 memories.

Featuring high performance Byte-Program, the AC39VF088 devices provide a typical Byte-Program time of 14 µsec. The devices use Toggle Bit or Data# Polling to detect the completion of the Program or Erase operation. To protect against inadvertent write, they have on-chip hardware and software data protection schemes. Designed, manufactured and tested for a wide spectrum of applications, these devices are offered with a typically guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 10 years.

The AC39VF088 devices are suited for applications that require memories with convenient and economical updating of program, data or configuration. For all system applications, they improve significantly the performance and reliability while lowering power consumption. They consume less energy during Erase and Program operations as compared to alternative flash technologies. When programming or erasing a flash device, the total energy consumption is a function of the applied voltage, current, and time of operation. Since for any given voltage range, Actrans' technology uses less current to program and has a shorter erase time, the total energy consumption during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for applications of program, data and configuration storage.

The technology provides fixed Erase and Program times, which is independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies whose Erase and Program times increase with accumulated Erase and Program cycles.

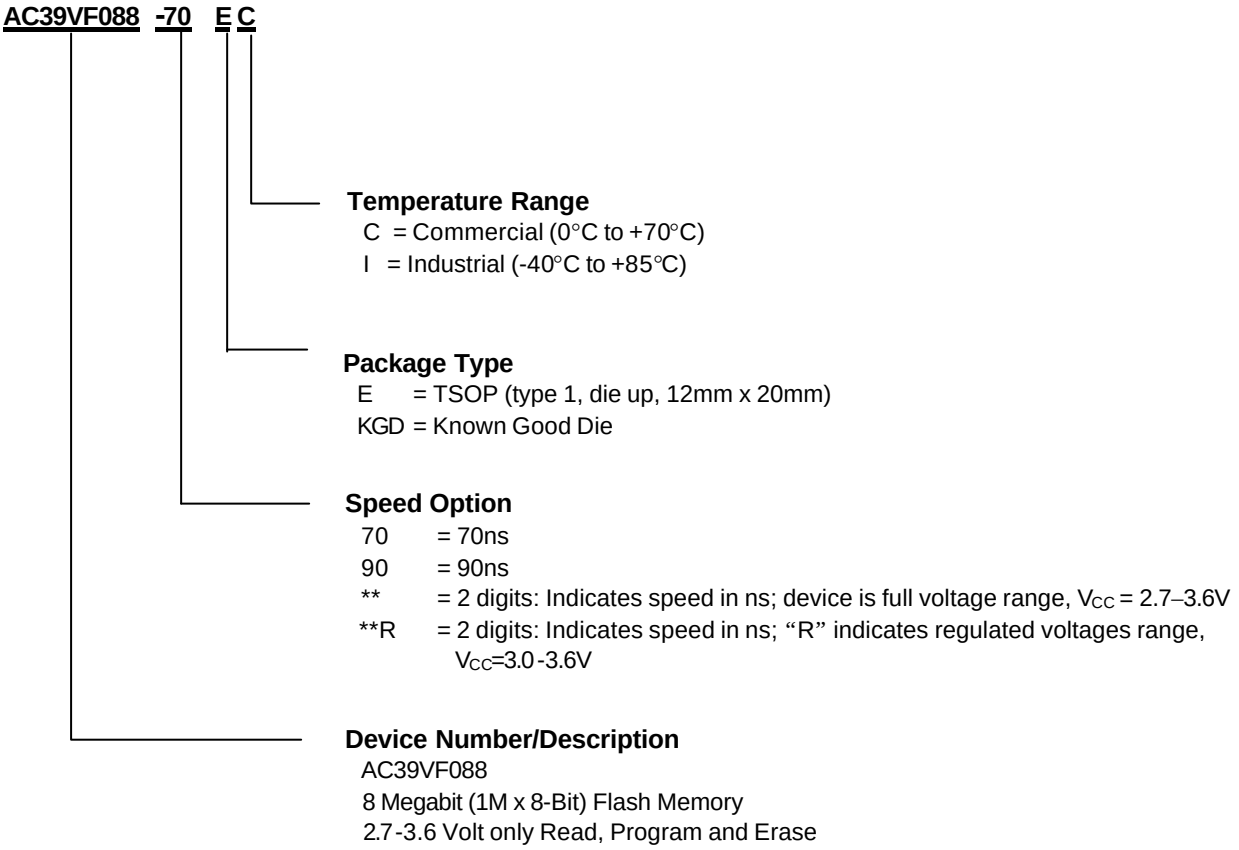
To meet surface mount requirements, the AC39VF088 is offered in package types of 48-pin TSOP, and known good die (KGD). For KGD, please contact Actrans System Inc. or its representatives for detailed information.

Table 1. PIN DESCRIPTION

Name of the Pin	Function
A0–A19	20 addresses
DQ7–DQ0	Data inputs/outputs
CE#	Chip enable
OE#	Output enable
WE#	Write enable
V_{DD}	2.7-3.6 volt single power supply
V_{SS}	Device ground
NC	Pin not connected internally

ORDERING INFORMATION
Standard Products

The order number is defined by a combination of the following elements.

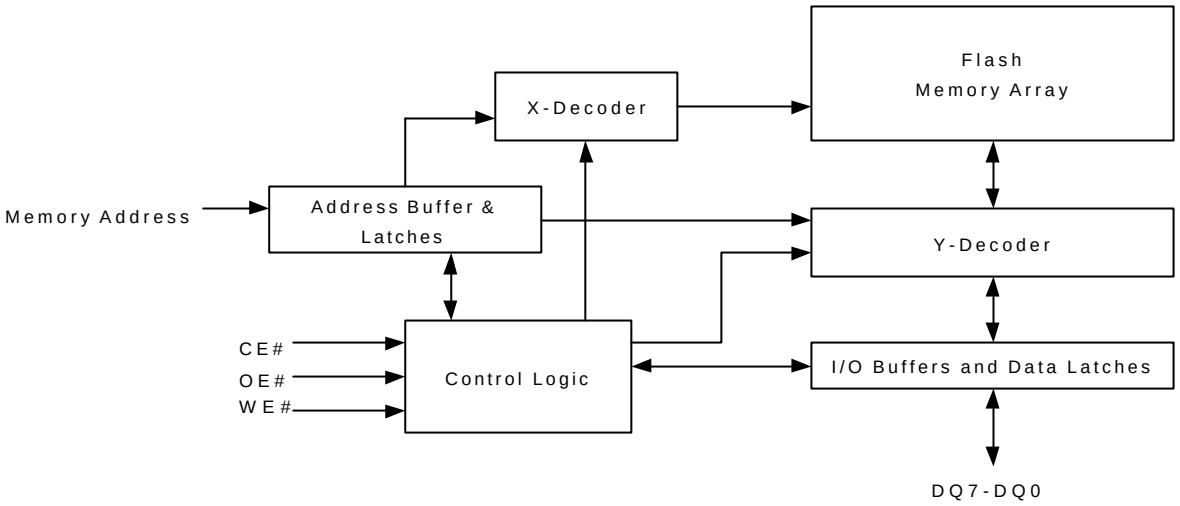


Valid Combinations for TSOP 48Pin Package	
AC39VF088-70	EC, EI
AC39VF088-70R	EC, EI
AC39VF088-90	EC, EI
AC39VF088-90R	EC, EI

Valid Combinations for FBGA 48 Ball Package			
Order Number		Package Marking	
AC39VF088-70	WAC, WAI	V088-70	C, I
AC39VF088-70R	WAC, WAI	V088-70R	C, I
AC39VF088-90	WAC, WAI	V088-90	C, I
AC39VF088-90R	WAC, WAI	V088-90R	C, I

Valid Combinations: Valid Combinations list the configurations that are supported in volume for this device.

Functional Block Diagram



Pin Assignments

DEVICE OPERATION

The AC39VF088 devices use Commands to initiate the memory operation functions. The Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Byte Program

The AC39VF088 devices are programmed on a byte-by-byte basis. Before programming, the sector where the byte locates must be fully erased. The Program operation is accomplished in three steps. The first step is a three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last; and the data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 20 µs. See Figures 2 and 3 for WE# and CE# controlled Program operation timing diagrams and Figure 14 for flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored.

Read

The Read operation of the AC39VF088 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram in Figure 1 for further details.

Table 2: AC39VF088 Device Operation

Operation	CE#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X[1]	Sector or Block address, XXH for Chip-Erase
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/D_{OUT}	X
Software Mode	V_{IL}	V_{IL}	V_{IH}		See Table 3
Product Identification					

1. X can be V_{IL} or V_{IH}, but no other value.

Write Command/Command Sequence

The AC39VF088 provides two software means to detect the completion of a write (Program or Erase) cycle in order to optimize the system write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation. The actual completion of the write operation is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Chip Erase

The AC39VF088 provides Chip-Erase feature, which allows the user to erase the entire memory array to the "1" state. This is useful and convenient when the entire device must be quickly erased. The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address AAAH in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid reads are Toggle Bit and Data# Polling. See Table 3 for the command sequence, Figure 6 for timing diagram, and Figure 17 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Sector/Block Erase

The AC39VF088 offers both Sector-Erase and Block-Erase modes. The Sector- (or Block-) Erase operation allows the system to erase the devices on a sector-by-sector (or block-by-block) basis. The sector architecture is based on uniform sector size of 4 KByte. The Block-Erase mode is based on uniform block size of 64 KByte. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit method. See Figures 7 and 8 for timing waveforms. Any commands issued during the Sector or Block Erase operation are ignored.

Data# Polling (DQ7)

When the AC39VF088 is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce the true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Program operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 4 for Data# Polling timing diagram and Figure 15 for a flowchart.

Toggle Bit (DQ6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 1s and 0s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ_6 bit will stop toggling. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 5 for Toggle Bit timing diagram and Figure 15 for a flowchart.

Data Protection

The AC39VF088 provides both hardware and software features to protect the nonvolatile data

from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The AC39VF088 provides the JEDEC approved Software Data Protection scheme for all data iteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. This group of devices is shipped with the Software Data Protection permanently enabled. See Table 3 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ15-DQ8 can be V_{IL} or V_{IH}, but no other value, during any SDP command sequence.

Product Identification

The product identification mode identifies the device as the AC39VF088. This mode may be assessed by software operations. Users may use the Software Product Identifiaction operation to identify the part(i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 3 for software operation, Figure 9 for the Software Entry and Read timing diagram and Figure 14 for the Software ID Entry command sequence flowchart.

Product Identification Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read operation. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., command is ignored during an internal Program or Erase operation. See Table 3 for software command and Figure 14 for a flowchart.

Table 3: Software Command Sequence

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Byte Program	AAAH	AAH	555H	55H	AAAH	A0H	WA[2]	Data				
Sector Erase	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	SA_X[4]	30H
Block Erase	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	BA_X[4]	50H
Chip Erase	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
Software ID Entry[5,6]	AAAH	AAH	555H	55H	AAAH	90H						
Manufacture ID	AAAH	AAH	555H	55H	AAAH	90H	000H	07FH				
Manufacture ID	AAAH	AAH	555H	55H	AAAH	90H	007H	07FH				
Manufacture ID	AAAH	AAH	555H	55H	AAAH	90H	080H	01FH				
Device ID	AAAH	AAH	555H	55H	AAAH	90H	001H	21H				
Software ID Exit[7]	XXH	F0H										

1. Address format A14-A0 (Hex), Addresses A19-A15 can be V_{IL} or V_{IH}, but no other value, for the Command sequence.
2. DQ7-DQ0 can be V_{IL} or V_{IH}, but no other value, for the Command sequence.
3. WA = Program Byte address.
4. SA_X for Sector-Erase; uses A19-A12 address lines.
   BA_X for Block-Erase; uses A19-A16 address lines.
5. The device does not remain in Software Product ID mode if powered down.
6. Both Software ID Exit operations are equivalent.
7. Please refer to figure 9 for more information.

ABSOLUTE MAXIMUM RATINGS (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... –55°C to 125°C
Storage Temperature ..... –65°C to 150°C
D.C. Voltage on Any Pin to Ground Potential ..... –0.5 V to V_{DD}+0.5V
Transient Voltage (<20ns) on Any Pin to Ground Potential..... –2.0V to V_{DD} +2.0V
Voltage on A9 Pin to Ground Potential..... –0.5 V to 13.2V
Package Power Dissipation Capability (Ta=25°C)..... 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds)..... 240°C
Output Short Circuit Current (Note 1)..... 50mA

Note 1: Output shorted for no more than one second. No more than one output shorted at a time.

Table 4: Operating Range

Model Name	Range	Ambient Temperature	V_{DD}
AC39VF088	Commercial	0°C to +70°C	2.7~3.6V
	Industrial	-40°C to +85°C	2.7~3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time..... 5ns
Output Load..... C_L=30pF for 55Rns
Output Load..... C_L=100pF for 70ns/90ns
See Figures 14 and 15

Table 5: DC CHARACTERISTICS

CMOS Compatible

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DD}	Power Supply Current	Address Input =V_{IL}/V_{IH}, at f=1/T_{RC} Min, V_{DD}=V_{DD} Max			
	Read	CE#=OE#=V_{IL}, WE#=V_{IH}, all I/Os open		30	mA
	Program and Erase	CE#=WE#=V_{IL}, OE#=V_{IH},		30	mA
I_{SB}	Standby V_{DD} Current	CE#=V_{IHC}, V_{DD}=V_{DD} Max		30	µA
I_{LI}	Input Leakage Current	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max		1	µA
I_{LO}	Output Leakage Current	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max		10	µA
V_{IL}	Input Low Voltage	V_{DD}=V_{DD} Min		0.8	V
V_{ILC}	Input Low Voltage (CMOS)	V_{DD}=V_{DD} Max		0.3	V
V_{IH}	Input High Voltage	V_{DD}=V_{DD} Max	0.7 V_{DD}		V
V_{IHC}	Input High Voltage (CMOS)	V_{DD}=V_{DD} Max	V_{DD}-0.3		V
V_{OL}	Output Low Voltage	I_{OL}=100µA, V_{DD}=V_{DD} Min		0.2	V
V_{OH}	Output High Voltage	I_{OH}=-100µA, V_{DD}=V_{DD} Min	V_{DD}-0.2		V

Table 6: Recommended System Power-up Timing

Parameter	Description	Min	Unit
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Program/Erase Operation	100	µs

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 7: Capacitance (Ta=25° C, f=1Mhz, other pins open)

Parameter	Description	Test Conditions	Max
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$=0V	12pF
C_{IN}[1]	Input Capacitance	V_{IN}=0V	6pF

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 8: Reliability Characteristics

Symbol	Parameter	Min Specification	Unit	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	10	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100+I_{DD}	mA	JEDEC Standard 78

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CCHARACTERISTICS

Table 9: Read Cycle Timing Parameters

Symbol	Parameter	70REC		90REC		Unit
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		90		ns
T_{CE}	Chip Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		20		30	ns
T_{OHZ}[1]	OE# High to High-Z Output		20		30	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

Symbol	Parameter	70EC		90EC		Unit
		Min	Max	Min	Max	
T_{RC}	Read Cycle Time	70		90		ns
T_{CE}	Chip Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
T_{CLZ}[1]	CE# Low to Active Output	0		0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		0		ns
T_{CHZ}[1]	CE# High to High-Z Output		20		30	ns
T_{OHZ}[1]	OE# High to High-Z Output		20		30	ns
T_{OH}[1]	Output Hold from Address Change	0		0		ns

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 10: Program/Erase Cycle Timing Parameter

Symbol	Parameter	Min	Max	Unit
T_{BP}	Byte-Program Time		24	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	45		ns
T_{WP}	WE# Pulse Width	45		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	45		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time		150	ns
T_{SE}	Sector Erase		30	ms
T_{BE}	Block Erase		30	ms
T_{SCE}	Chip Erase		60	ms

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

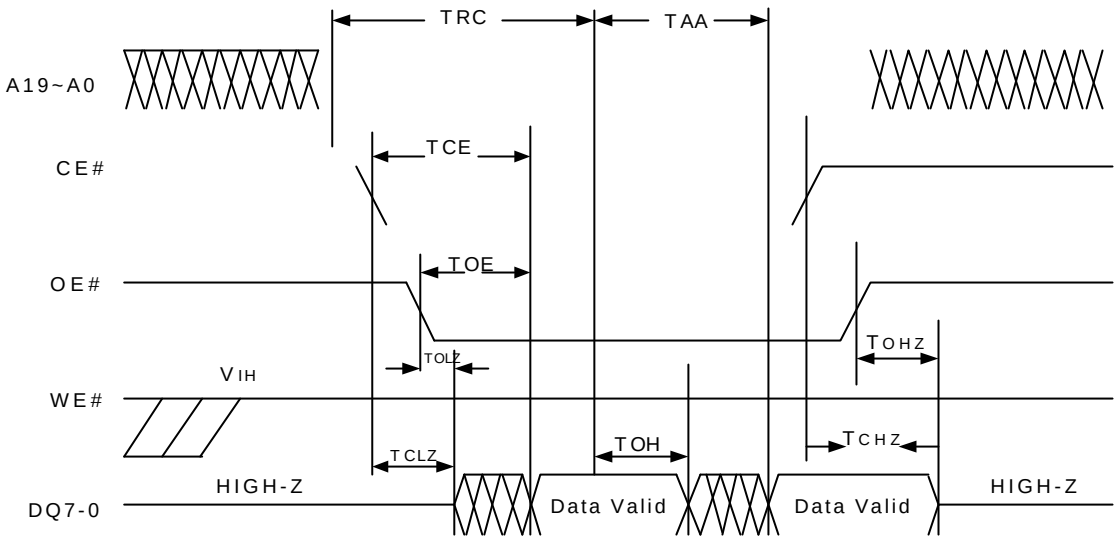
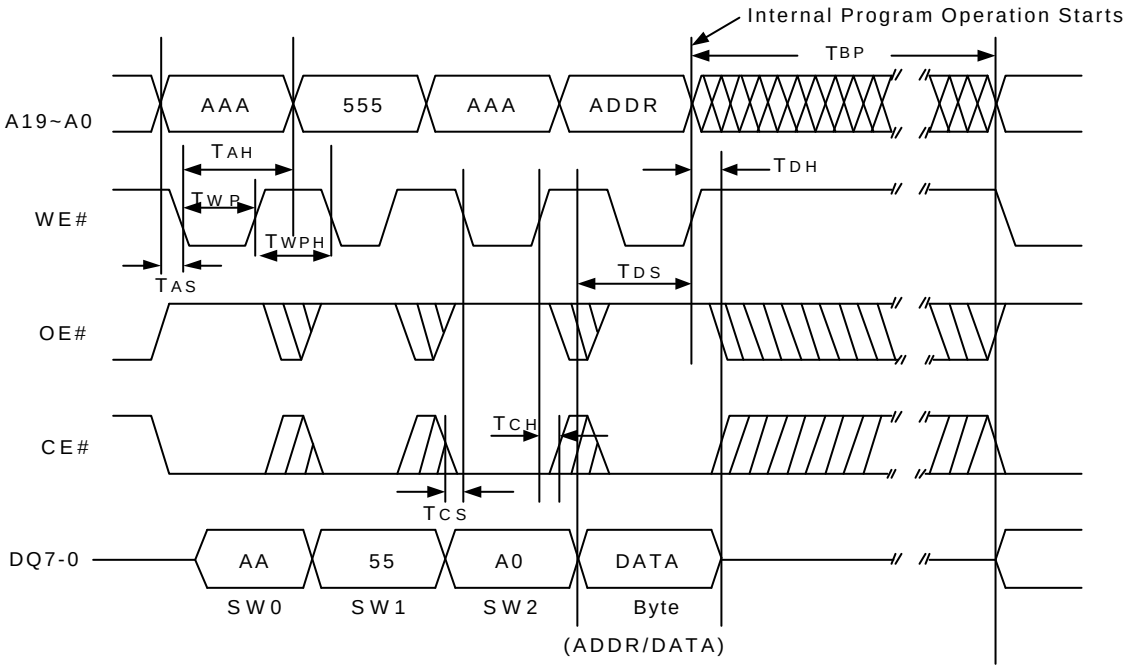
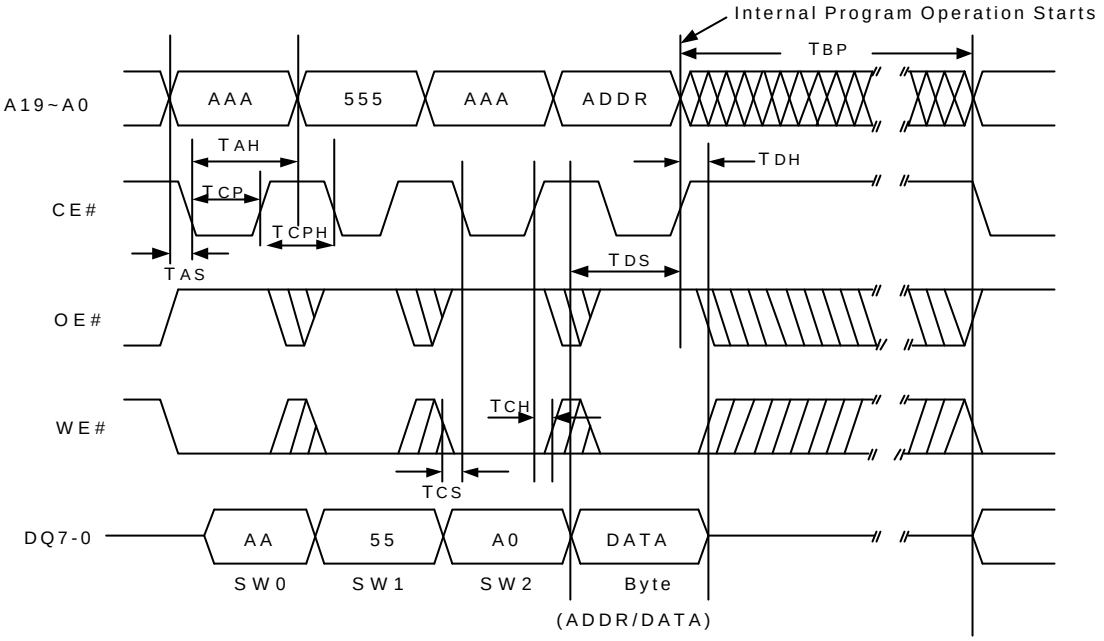


Figure 1. Read Cycle Timing Diagram



X can be VIL or VIH, but no other value.

Figure 2. WE# Controlled Program Cycle Timing Diagram



X can be VIL or VIH, but no other value.

Figure 3. CE# Controlled Program Cycle Timing Diagram

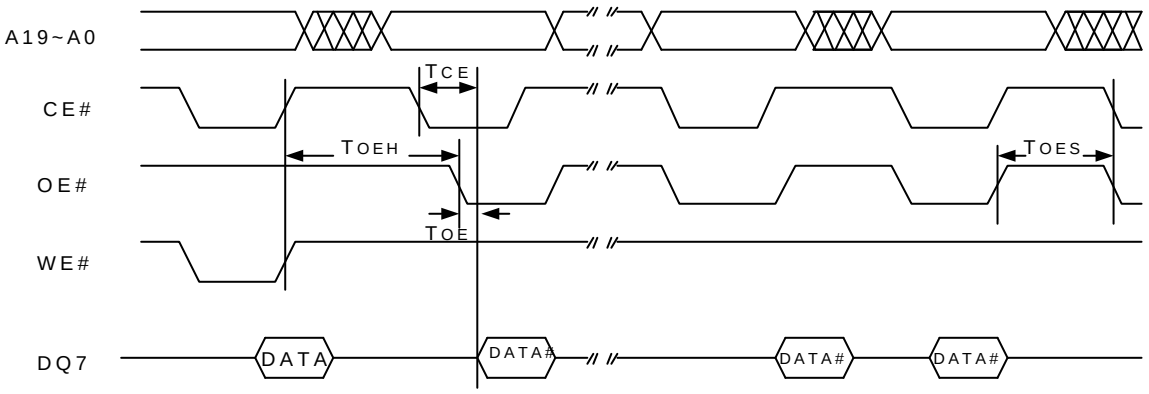


Figure 4. Data# Polling Timing Diagram

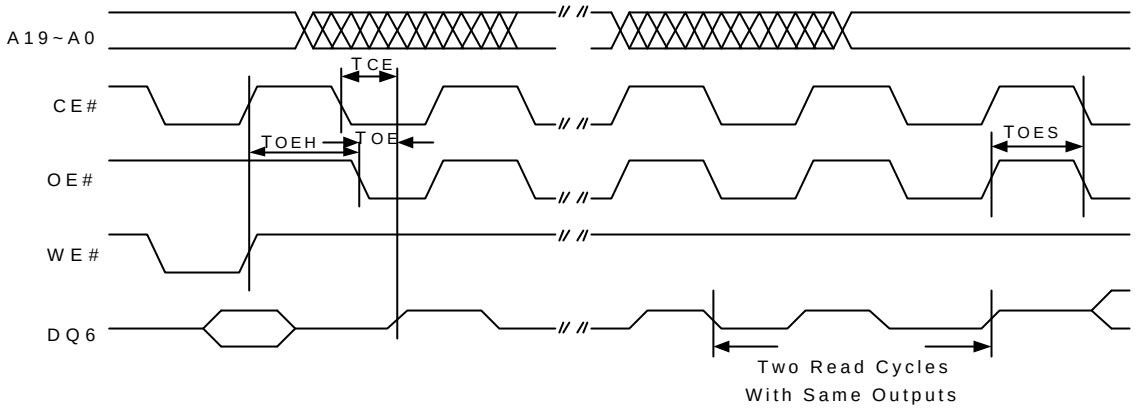
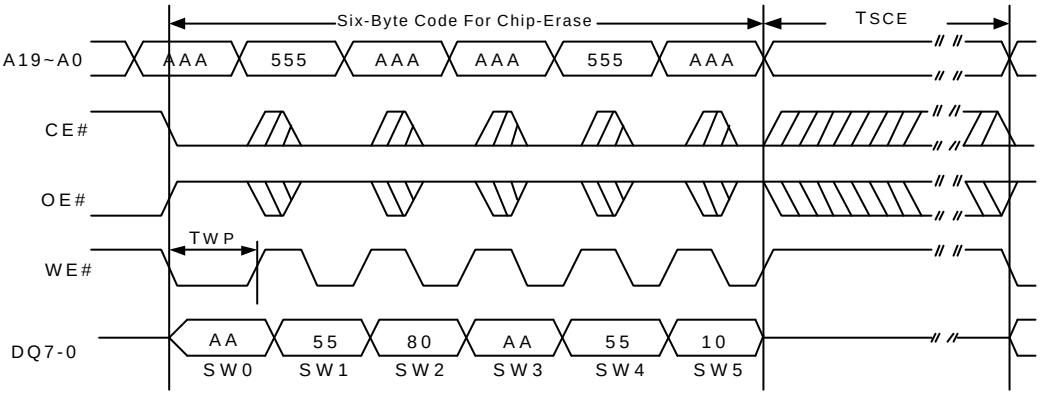


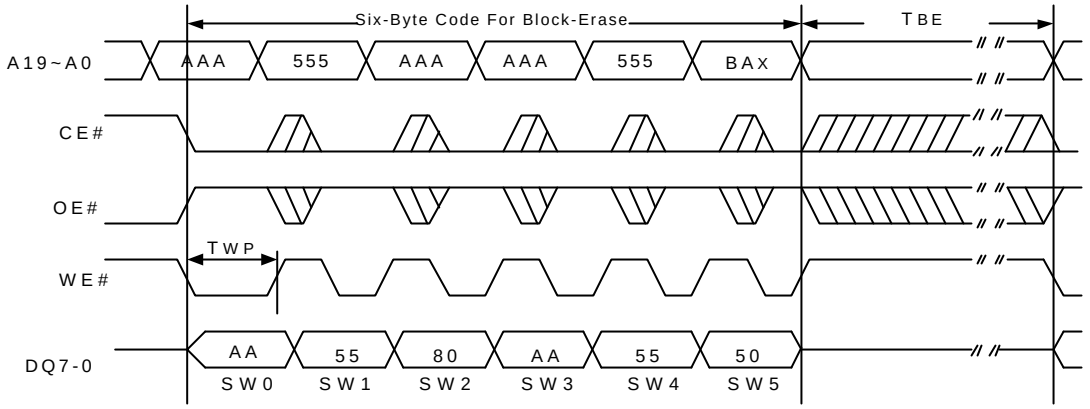
Figure 5. Toggle Bit Timing Diagram



Note: This device also supports CE# controlled Chip-Erase operation. The WE#and CE# signals are interchageable as long as minimum timings are met. (See Table 14)

X can be V_{IL} or V_{IH}, but no other value.

Figure 6. WE# Controlled Chip-Erase Timing Diagram

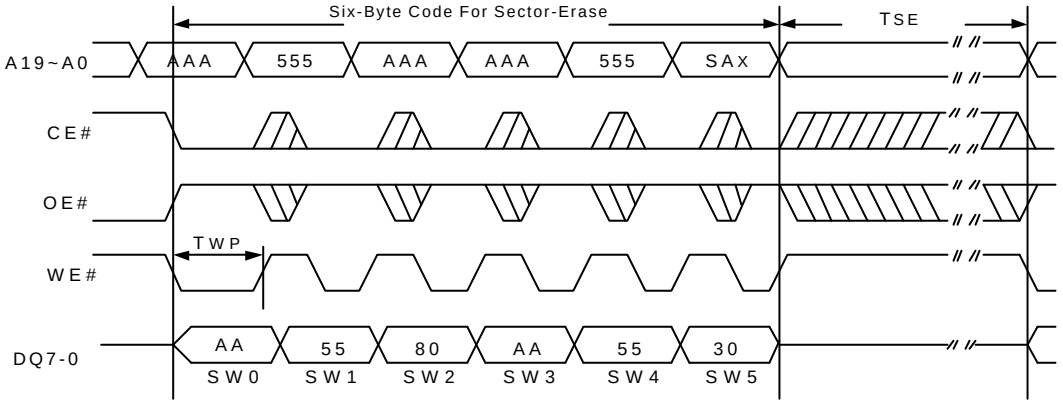


Note: This device also supports CE# controlled Block-Erase operation. The WE#and CE# signals are interchageable as long as minimum timings are met. (See Table 14)

BAX=Block Address

X can be VIL or VIH, but no other value.

Figure 7. WE# Controlled Block-Erase Timing Diagram



Note: This device also supports CE# controlled Sector-Erase operation. The WE#and CE# signals are interchageable as long as minimum timings are met. (See Table 14)

SAX=Sector Address

X can be VIL or VIH, but no other value.

Figure 8. WE# Controlled Sector-Erase Timing Diagram

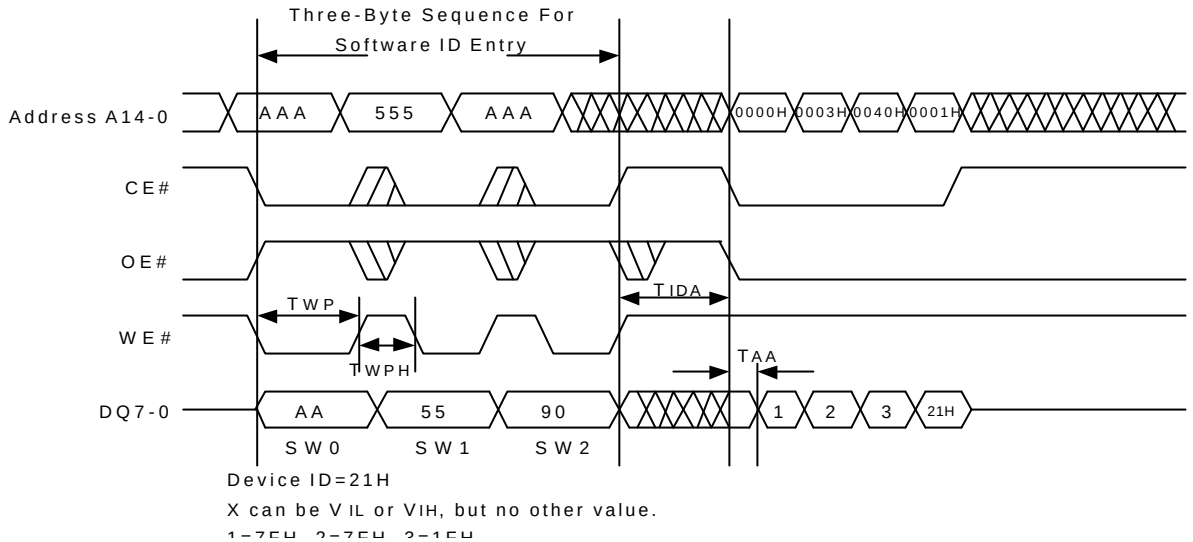
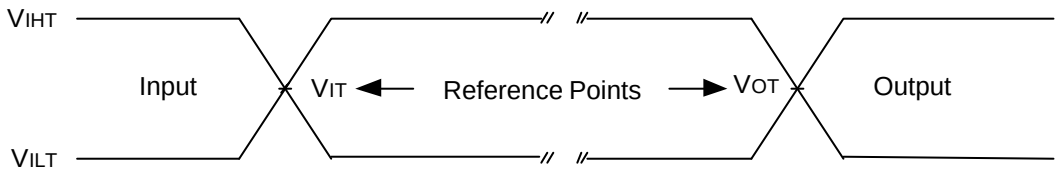


Figure 9. Software ID Entry and Read



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT}(0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outpputs are V_{IT}(0.5 V_{DD}) and V_{OT}(0.5 V_{DD}). Input rise and fall times(10% - 90%) are <5ns

Note: V_{IT} = Vinput Test
V_{OT} = Voutput Test
V_{IHT} = Vinput HIGH Test
V_{ILT} = Vinput LOW Test

Figure 10. AC Input/Output Reference Waveforms

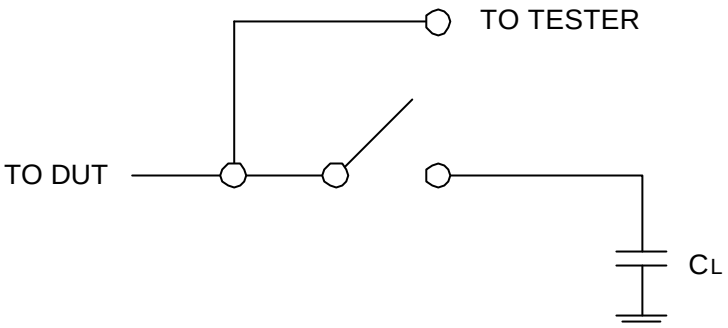


Figure 11. A Test Load Example

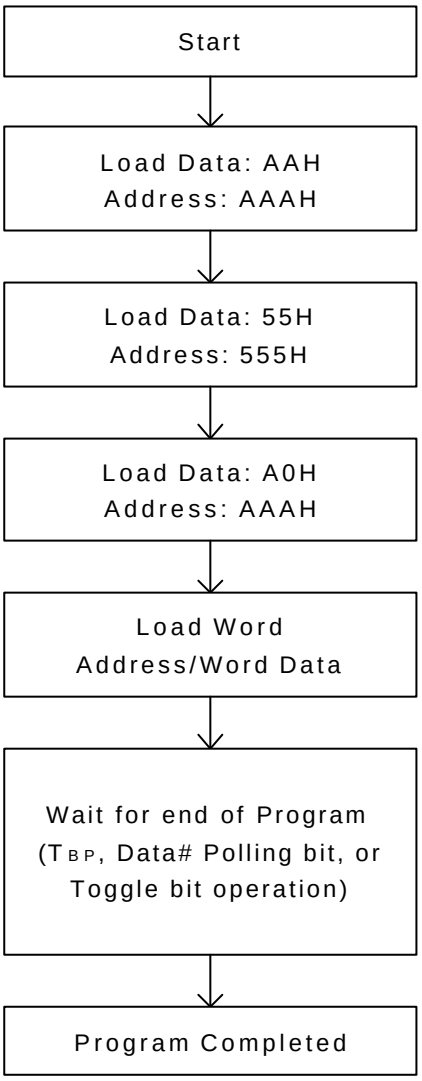


Figure 12. Byte-Program Algorithm

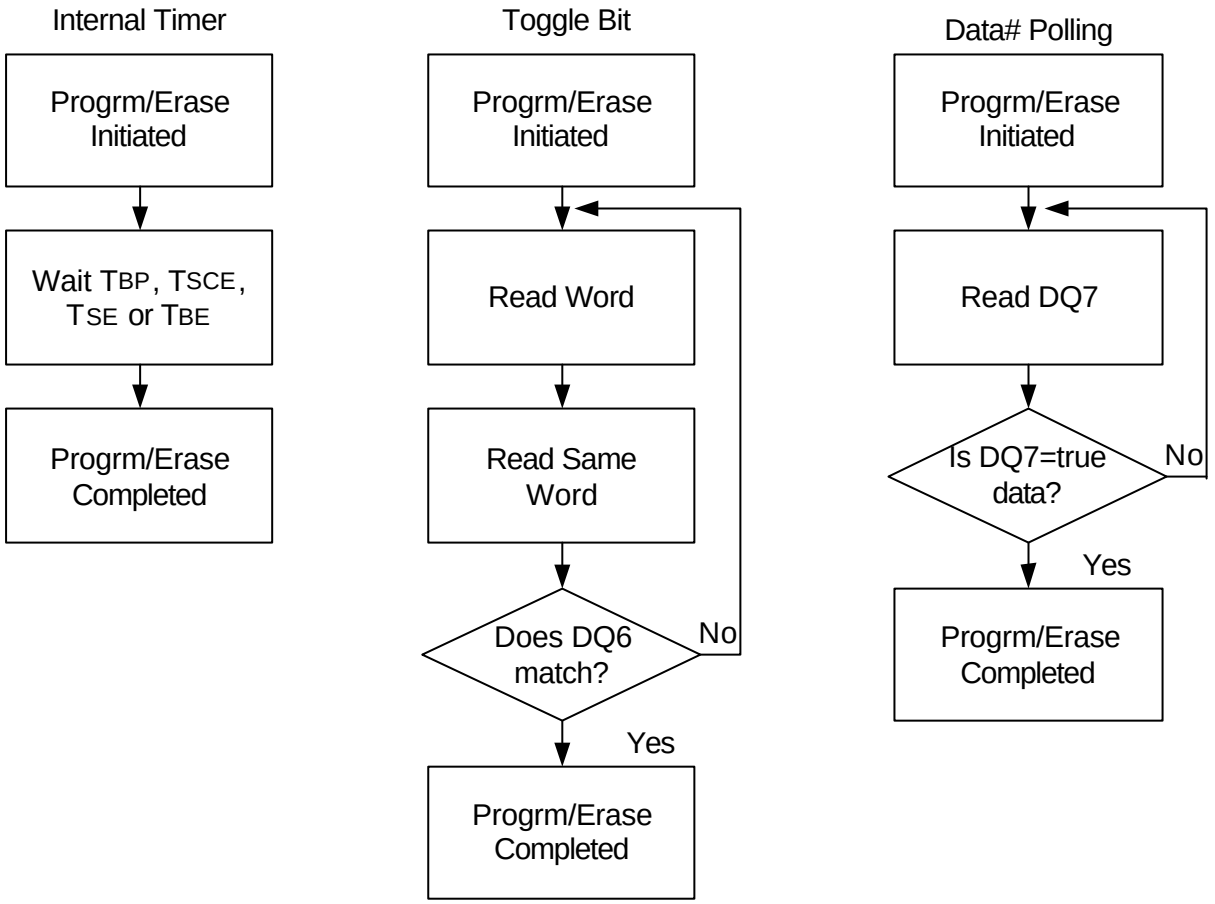


Figure 13. Wait Options

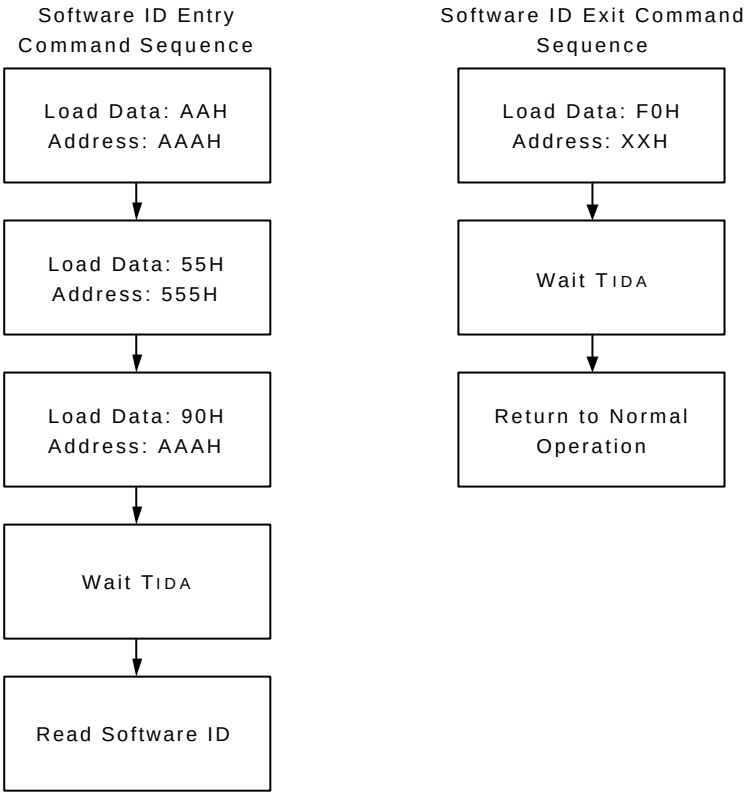


Figure 14. Software ID Command Flowcharts

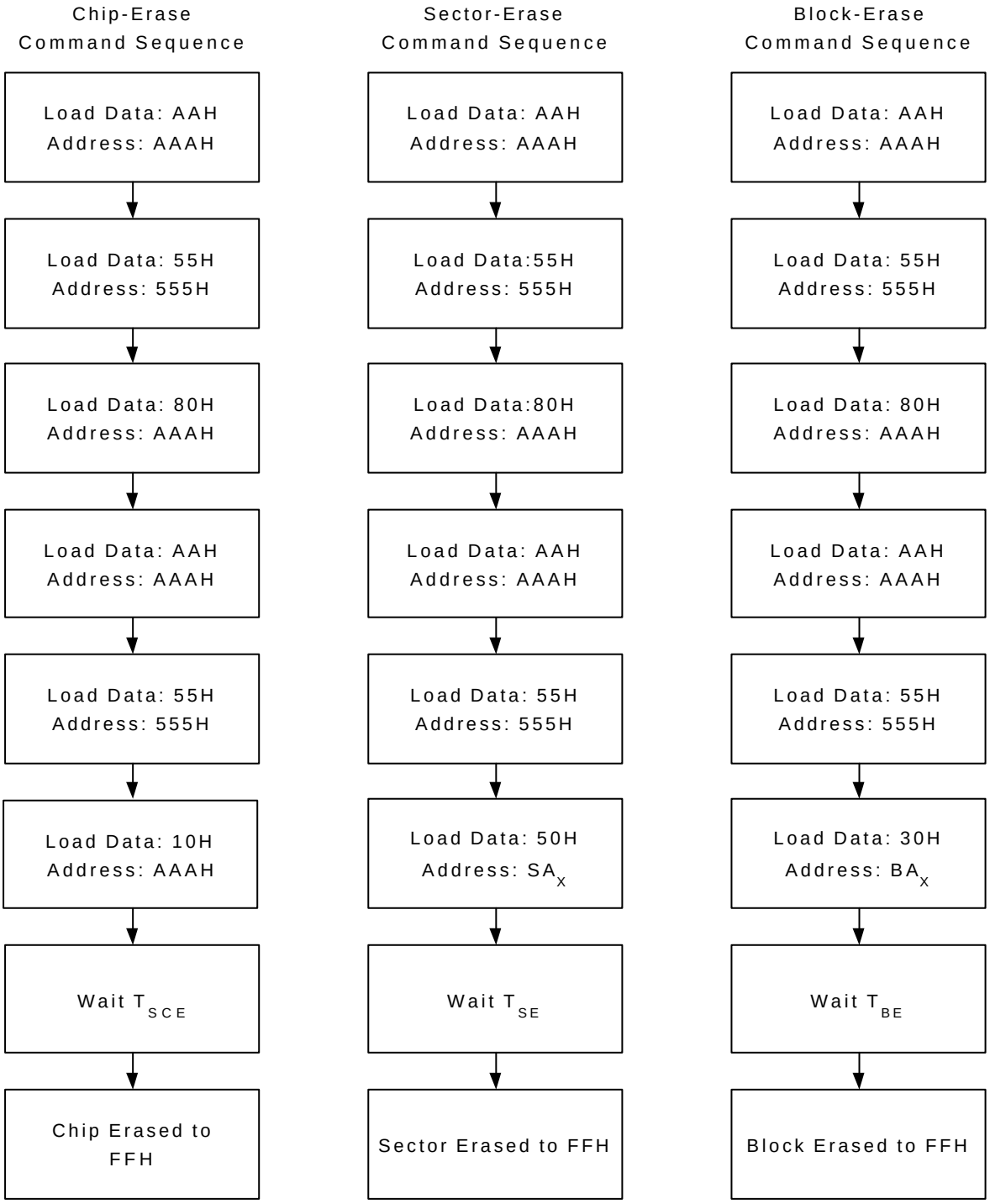


Figure 15. Erase Command Sequence