

General Description

The AAT4900 FastSwitch™ is a member of AnalogicTech™'s Application Specific Power MOSFET™ (ASPM™) product family. It is a Buffered Power Half-Bridge, consisting of low on-resistance Power MOSFETs with integrated control logic. This device operates with inputs ranging from 2.7V to 5.5V, making it ideal for both 3V and 5V systems. The device is protected from shoot-through current with its own control circuitry. The AAT4900 is capable of very fast switching times and is ideal for use in high frequency DC to DC Converters. The quiescent supply current is a low 4mA at 1MHz CLK frequency. In shutdown mode, the supply current decreases to less than 1µA max.

The AAT4900 is available in 5 pin SOT-23 or 8 pin SC70JW specified over -40 to 85°C.

Features

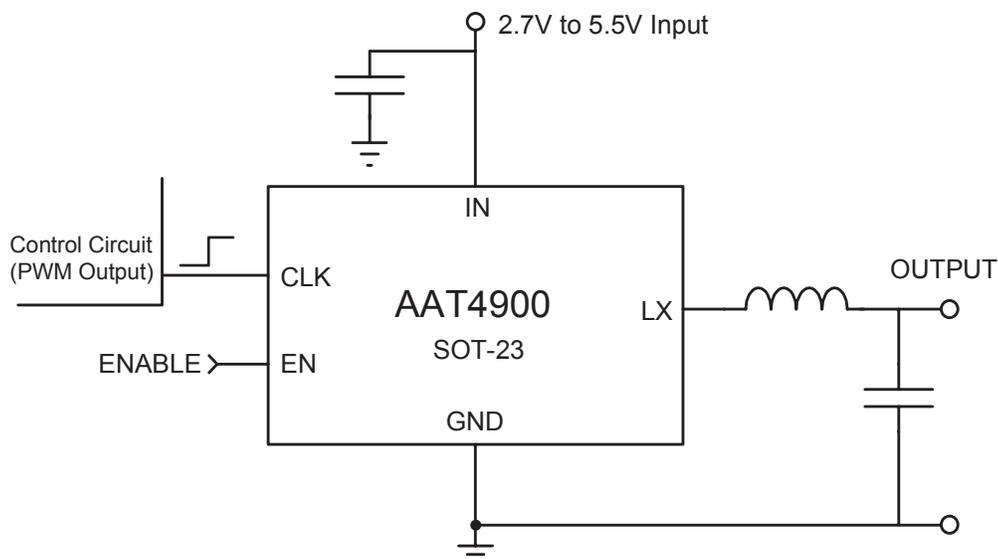
- 2.7V to 5.5V Input voltage range
- 105mΩ (typ) Low Side Switch $R_{DS(ON)}$
- 130mΩ (typ) High Side Switch $R_{DS(ON)}$
- Low quiescent current
 - 1µA (max) DC
 - 4mA at 1MHz
- Only 2.5V needed for Control Signal Input
- Break before make shoot-thru protection
- Temp range -40 to 85°C
- 5 pin SOT-23 or 8 pin SC70JW package

Applications

- High frequency DC/DC converters
- MOSFET Driver
- DC Motor Drive

Typical Applications

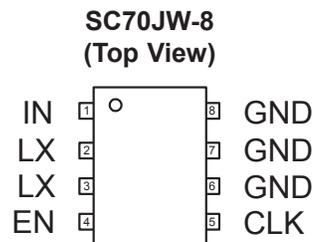
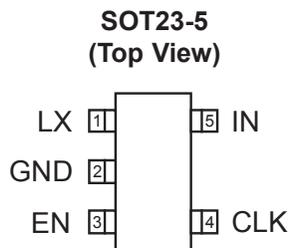
DC/DC Converter Output Stage



Pin Descriptions

Pin #		Symbol	Function
SOT23-5	SC70JW-8		
1	2, 3	LX	Inductor connection. LX output is controlled by CLK and EN(see Control Logic Table).
2	6, 7, 8	GND	Ground connection
3	4	EN	Active-high Enable input. A logic low signal puts the LX output pin in high impedance mode.
4	5	CLK	Logic input signal determines the state of LX output.
5	1	IN	Supply voltage input. Input voltage range from 2.7V to 5.5V.

Pin Configuration



Control Logic Table

Inputs		Output
CLK	EN	LX
0	0	High impedance
0	1	V_{IN}
1	0	High impedance
1	1	Ground

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Description	Value	Units
V_{IN}	IN to GND	-0.3 to 6	V
V_{EN}, V_{CLK}	EN, CLK to GND	-0.3 to $V_{IN}+0.3$	V
V_{OUT}	OUT to GND	-0.3 to $V_{IN}+0.3$	V
I_{MAX}	Maximum Continuous Switch Current	2	A
T_J	Operating Junction Temperature Range	-40 to 150	$^\circ\text{C}$
V_{ESD}	ESD Rating ¹ - HBM	4000	V
T_{LEAD}	Maximum Soldering Temperature (at Leads)	300	$^\circ\text{C}$

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Note 1: Human body model is a 100 pF capacitor discharged through a 1.5k Ω resistor into each pin.

Thermal Information

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance ² (SOT23-5, SC70JW-8)	190	$^\circ\text{C}/\text{W}$
P_D	Power Dissipation ² (SOT23-5, SC70JW-8)	526	mW

Note 2: Mounted on a demo board.

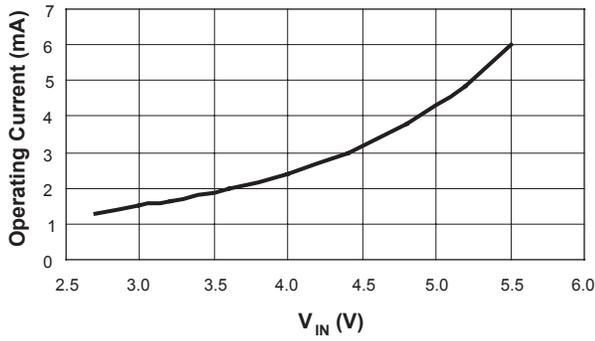
Electrical Characteristics ($V_{IN} = 5\text{V}$, $T_A = -40$ to 85°C unless otherwise noted. Typical values are at $T_A=25^\circ\text{C}$)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Operation Voltage		2.7		5.5	V
I_{QAC}	AC Quiescent Current	IN = 5V, EN = IN, CLK = 1MHz, $I_{LX} = 0$		4	9	mA
I_{QDC}	DC Quiescent Current	IN = 5V, EN = IN, CLK = GND, $I_{LX} = 0$			1	μA
$I_{Q(OFF)}$	Off-Supply Current	EN = CLK = GND IN = LX = 5.5V			1	μA
$I_{SD(OFF)}$	Off-Switch Current	EN = GND, IN = 5.5V, $V_{OUT}=0$, or LX = IN		0.03	1	μA
$R_{DS(ON)H}$	High Side MOSFET On Resistance	IN = 5.0V, $T_A = 25^\circ\text{C}$		130	165	m Ω
		IN = 3.0V, $T_A = 25^\circ\text{C}$		165	195	m Ω
$R_{DS(ON)L}$	Low Side MOSFET On Resistance	IN = 5.0V, $T_A = 25^\circ\text{C}$		105	145	m Ω
		IN = 3.0V, $T_A = 25^\circ\text{C}$		135	175	m Ω
V_{ONL}	CLK, EN Input low Voltage	IN = 2.7V to 5.5V			0.8	V
V_{ONH}	CLK, EN Input High Voltage	IN = 2.7V to $\leq 4.2\text{V}$ ³	2.0			V
		IN = $>4.2\text{V}$ to 5.0V ³	2.4			V
I_{SINK}	CLK, EN Input leakage	CLK, EN = 5.5v		0.01	1	μA
T_{BBM}	Break Before Make Time	CLK rising		5		ns
		CLK falling		5		ns
T_{ON-DLY}	CLK to LX delay	CLK rising		30		ns
		CLK falling		40		ns
T_{HIZ}	EN to OUT HiZ delay	CLK = GND		40		ns
		CLK = IN		40		ns

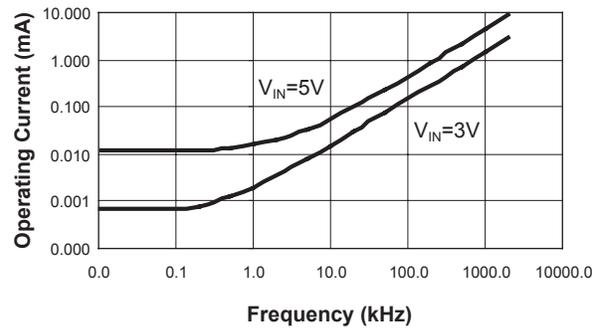
Note 3: For V_{IN} outside this range consult CLK/Enable Threshold vs. Input Voltage curve.

Typical Characteristics

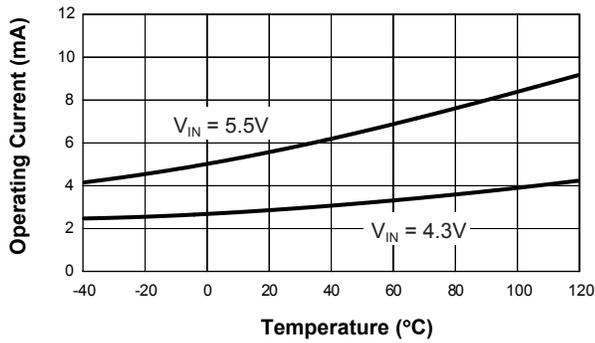
Operating Current vs. Input Voltage
Fs=1MHz



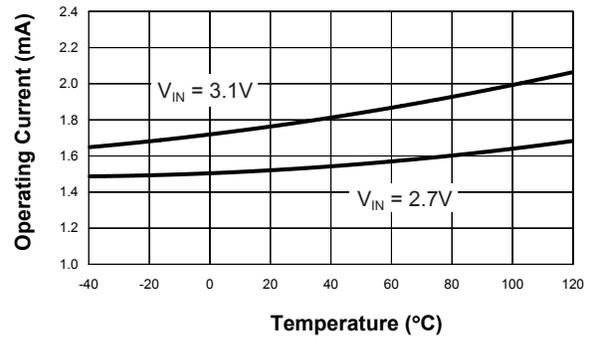
Operating Current vs. Switching Frequency



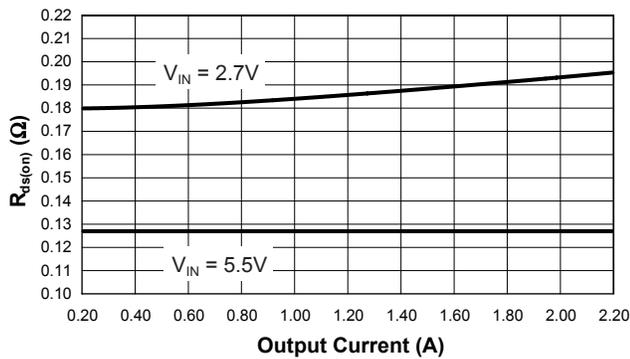
Operating Current vs. Temperature
Fs=1MHz



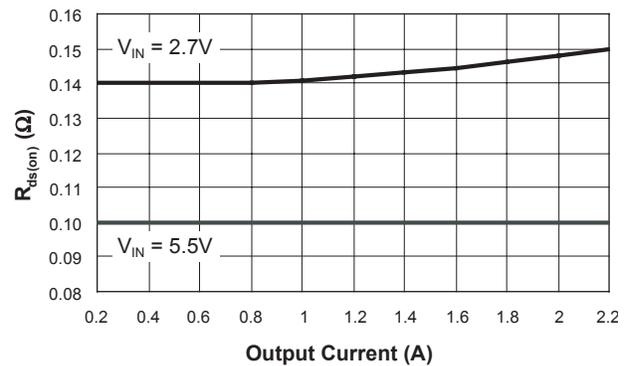
Operating Current vs. Temperature
Fs=1MHz



High Side R_{ds(on)} vs. Output Current

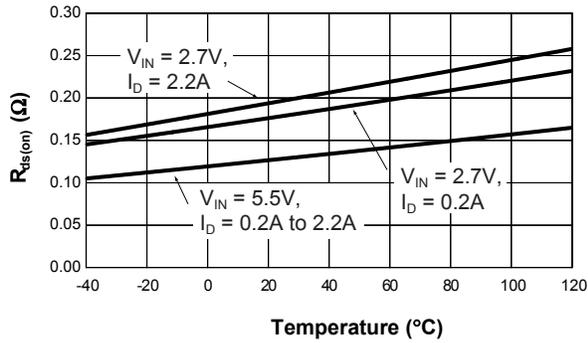


Low Side R_{ds(on)} vs. Output Current

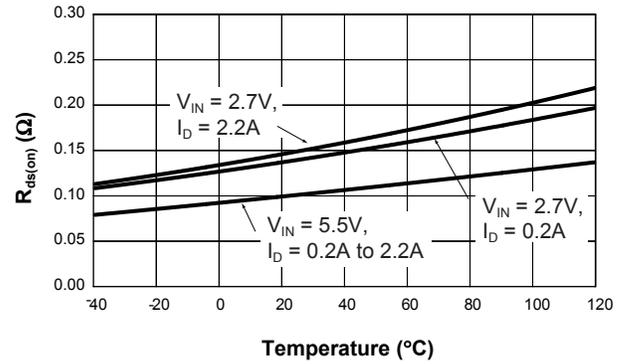


Typical Characteristics

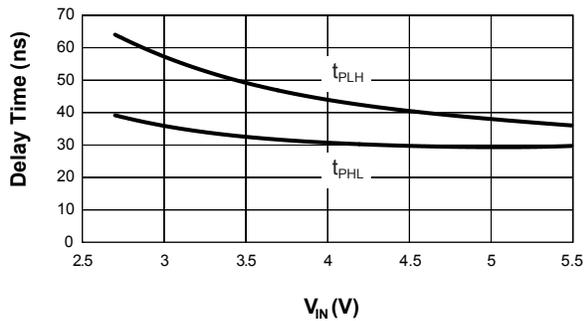
High Side $R_{ds(on)}$



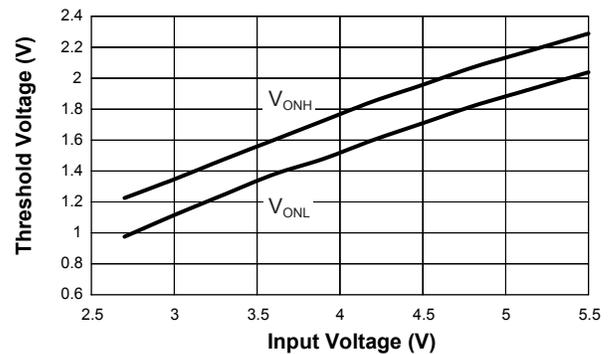
Low Side $R_{ds(on)}$



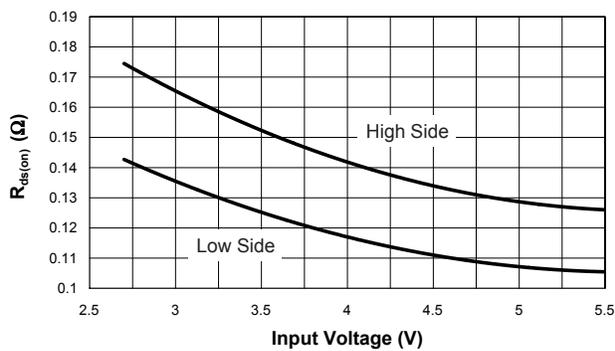
Propagation Delay vs. Input Voltage $C_L = 1000pF$



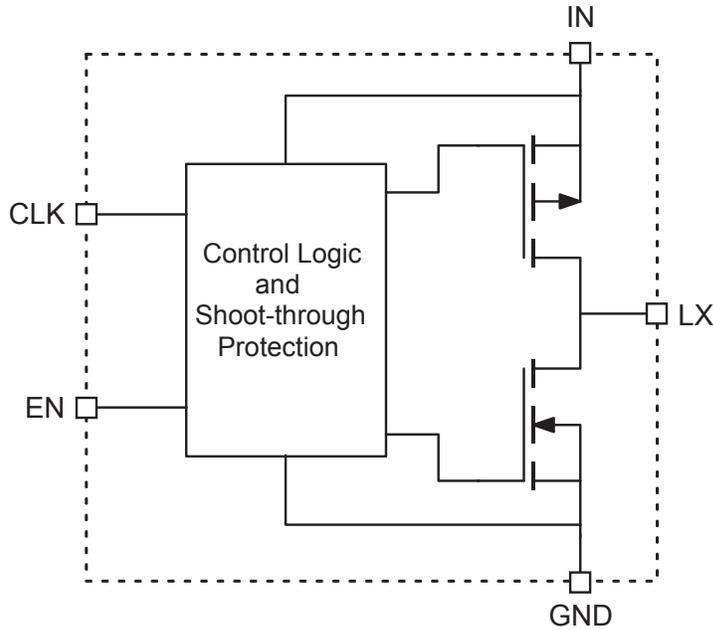
CLK/Enable Threshold vs. Input Voltage



$R_{ds(on)}$ vs. Input Voltage



Functional Block Diagram



Typical Applications

DC-DC Converter

The most common AAT4900 applications include a DC-DC converter output power stage and a MOS-FET gate drive buffer.

Figure 1 shows a common configuration when used as a DC-DC converter power stage with synchronous rectification. The enable pin can be used to

force the LX output to a high impedance state under light load conditions. This enables the output inductor to operate in discontinuous conduction mode (DCM), improving efficiency under light load conditions. The body diode associated with the low side switching device gives the AAT4900 inductive switching capability, clamping the LX node at a diode drop below GND during the break before make time.

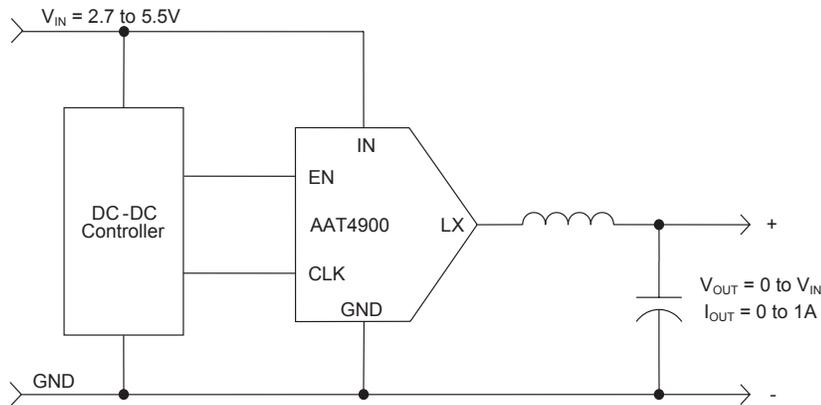


Figure 1: AAT4900 DC-DC Converter Power Stage

Synchronous Buck DC-DC Converter Application

The losses associated with the AAT4900 high side switching MOSFET are due to switching losses and conduction losses. The conduction losses are associated with the $R_{ds(on)}$ characteristics of the output switching device. At the full load condition, assuming continuous conduction mode (CCM), the on losses can be derived from the following equations.

$$D = \frac{V_o}{V_{in}}$$

D is the duty cycle

$$\Delta I = \frac{V_o}{L \cdot F} \left(1 - \frac{V_o}{V_{in}} \right)$$

ΔI is the *peak to peak* inductor ripple current.

High side switch RMS current

$$I_{rms(HS)} = \sqrt{\left(I_o^2 + \frac{\Delta I^2}{12} \right)} \cdot D$$

Low side switch RMS current

The low side RMS current is estimated by the following equation.

$$I_{rms(LS)} = \sqrt{\left(I_o^2 + \frac{\Delta I^2}{12} \right)} \cdot (1 - D)$$

Total Losses

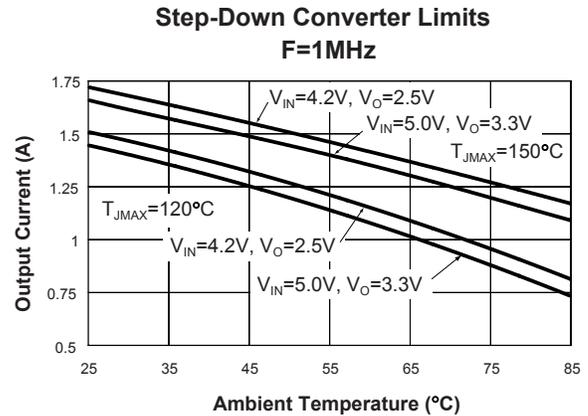
A simplified form of the above results (where the above descriptions of I_{rms} has been approximated with I_o) is given by:

$$P_{loss} = \frac{I_o^2 \cdot (R_{dson(HS)} \cdot V_o + R_{dson(LS)} \cdot (V_{in} - V_o))}{V_{in}} + (t_{sw} \cdot F \cdot I_o + I_q) \cdot V_{in}$$

Substitution of the I_{rms} equations with I_o results in very little error when the inductor ripple current is 20% to 40% of the full load current. The equation also includes switching and quiescent current losses where t_{sw} is approximated at 18 nsec and I_q is the no load quiescent current of the AAT4900. Quiescent current losses are associated with the gate drive of the output stage and biasing. Since the gate drive current varies with frequency and voltage, the bias current must be checked at the frequency, voltage, and temperature of operation with no load attached to the LX node. Once the above losses have been determined the maximum junction temperature can be calculated.

$$T_{jmax} = P_{loss} \cdot \Theta_{jc} = T_{amb}$$

Using the above equations the graph below shows the current capability for some typical applications with a maximum junction temperatures of 150°C and 120°C. The increase in $R_{ds(on)}$ vs. temperature is estimated at 3.75 mΩ for a 10°C increase in junction temperature.



Gate Drive

When used as a MOSFET gate driver the break before make shoot-thru protection significantly reduces losses associated with the driver at high frequencies.

The low $R_{ds(on)}$ of the output stage allows for a high peak gate current and fast switching speeds. A small package size facilitates close placement to the power device for optimum switching performance. The logic level inputs (CLK and EN) are high impedance inputs.

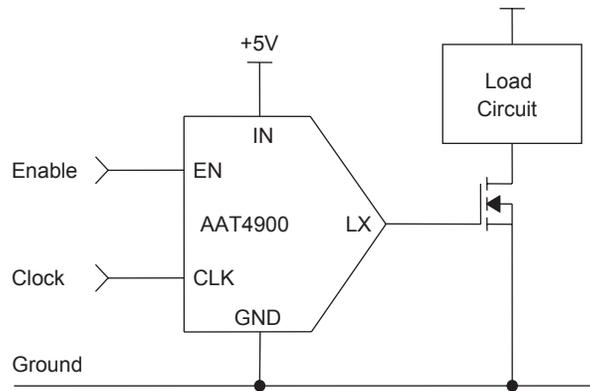


Figure 2: AAT4900 Gate Drive Configuration

Gate Drive Current Ratings

An estimate of the maximum gate drive capability with no external series resistor can be derived from equation 1. Note that the quiescent current varies with the ambient temperature, frequency of operation, and input voltage. The graphs below display the quiescent current and maximum gate charge drive capability at 85°C ambient vs. frequency for various input voltages.

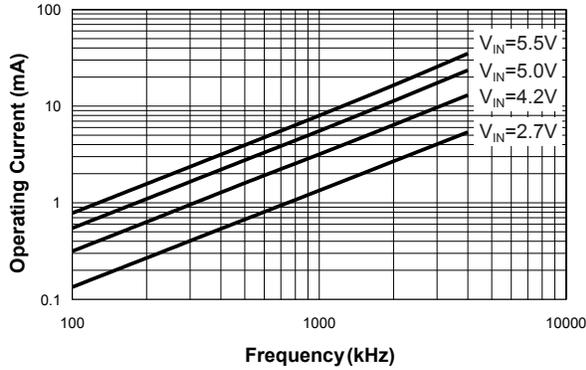
The quiescent current was first measured over temperature for various input voltages with no load

attached. Equation 1 was then used to derive the maximum gate charge capability for the desired maximum junction temperature. Q_g is the gate charge required to raise the gate of the load MOSFET to the input voltage. This value is taken from the MOSFET manufacturer's gate charge curve.

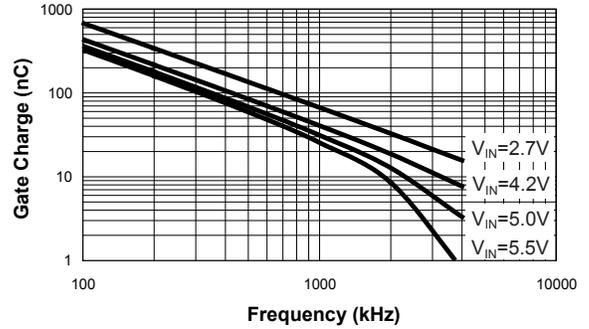
$$Q_{g \max} = \frac{1}{F_{sw}} \cdot \left(\frac{T_{j \max} - T_{amb}}{\theta_{ja}} \cdot V_{in \max} - I_q \right)$$

$$= \frac{1}{1\text{MHz}} \cdot \left(\frac{120^\circ\text{C} - 85^\circ\text{C}}{190^\circ\text{C/W} \cdot 4.2\text{V}} - 3.2\text{mA} \right) = 40\text{nC}$$

No Load Operating Current at 85°C Ambient



Maximum Gate Charge Load @ 85°C
Ambient $T_{jmax}=120°C$



The AAT4900 is also ideally suited to be used as an efficient output driver for DC Brushless Motor Control. The inductive load switching capability of the AAT4900 eliminates the need for external diodes.

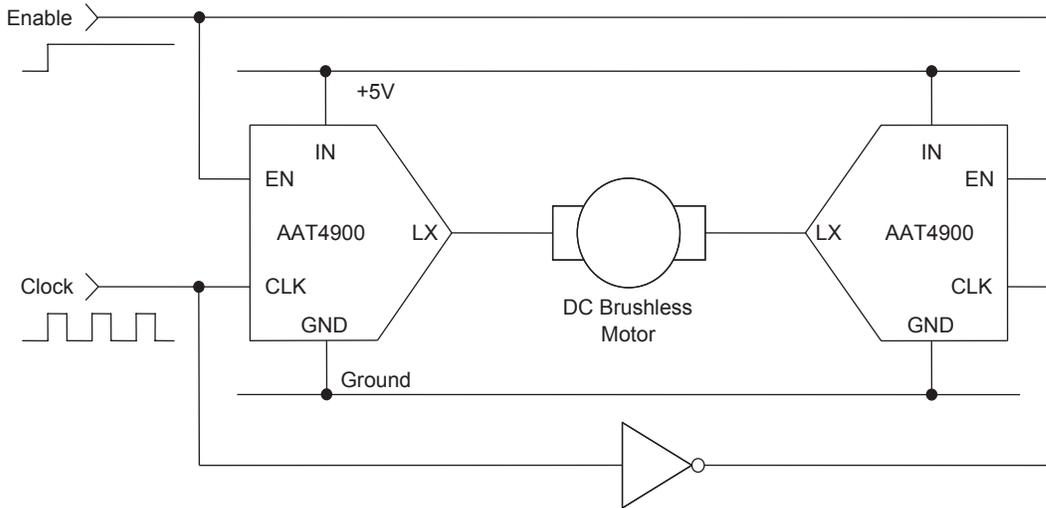
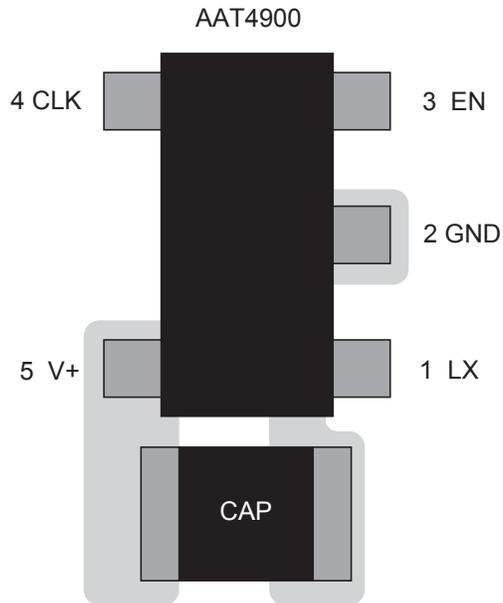


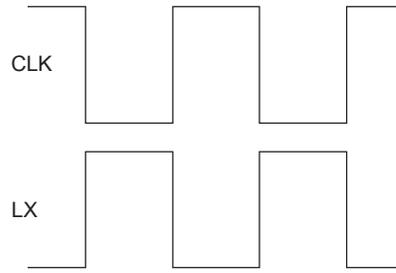
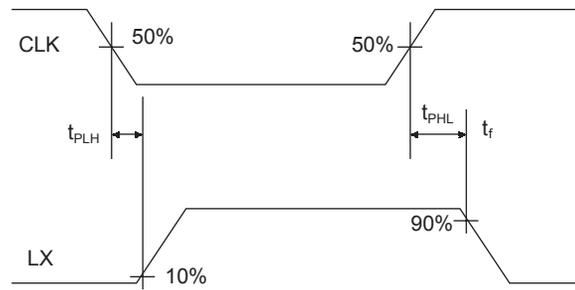
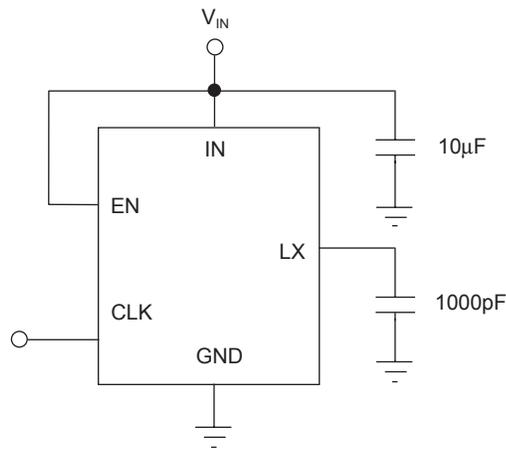
Figure 3: Typical Motor Control Block Diagram

Recommended Decoupling Layout Pattern

Because of the extremely fast switching speed and the high switching currents, optimum placement of the input capacitor is critical. It is recommended

that a 0.1 - 10 μ F 0805 or 1206 ceramic capacitor be placed as close as possible to the IC as shown in the diagram below. This helps to decouple the switching transients from the stray inductance present in the PCBoard.




Figure 5: Timing Diagram

Figure 6: Switching Time Waveforms

Figure 7: Propagation Delay Test Circuit

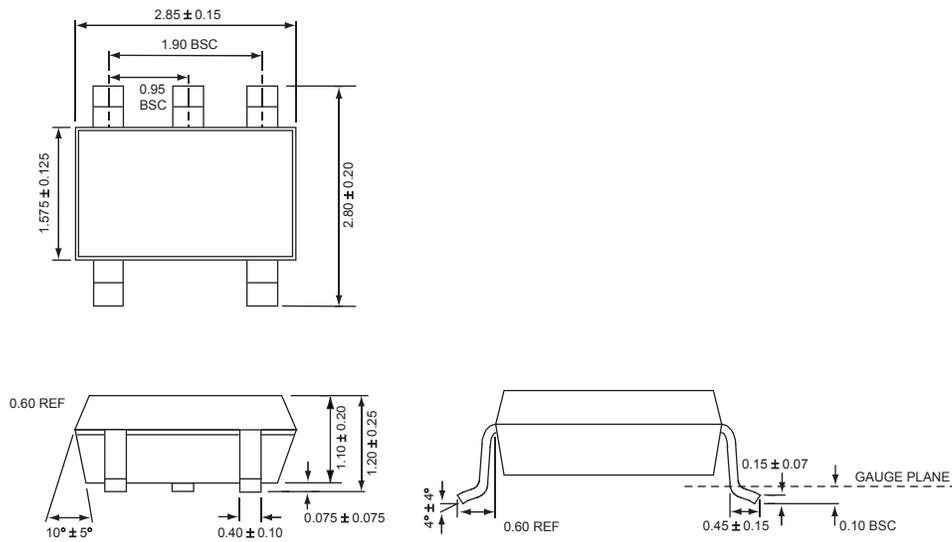
Ordering Information

Package	Marking	Part Number (Tape and Reel)
SOT23-5	ABXYY	AAT4900IGV-T1
SC70JW-8	ABXYY	AAT4900IJS-T1

Note: Sample stock is generally held on all part numbers listed in **BOLD**.
 Note 1: XYY = assembly and date code.

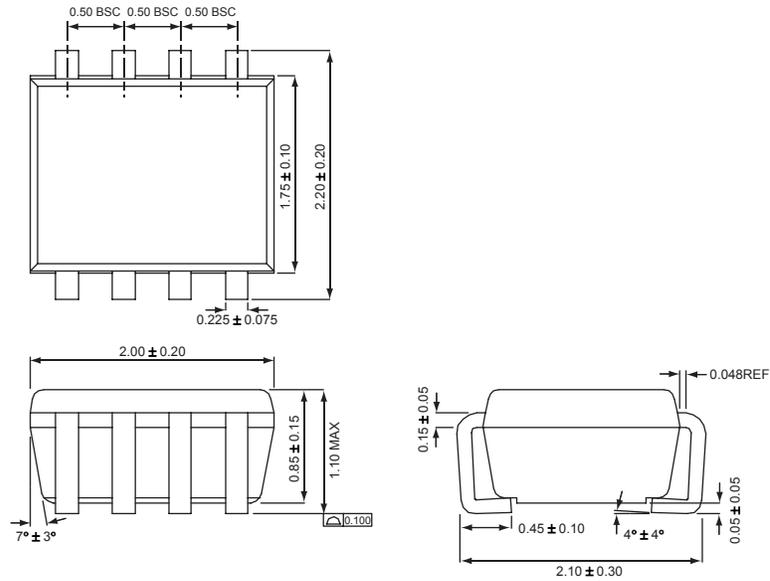
Package Information

SOT23-5



All dimensions in millimeters.

SC70JW-8



All dimensions in millimeters.

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