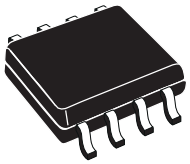
STS4NM20N

N-CHANNEL 200V - 0.11Ω - 4A SO-8
ULTRA LOW GATE CHARGE MDmesh™ II MOSFET

TARGET DATA

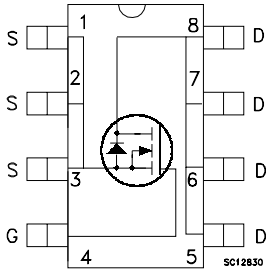
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS4NM20N	200 V	< 0.13 Ω	4A

- WORLDWIDE LOWEST GATE CHARGE
- TYPICAL $R_{DS}(on)$ = 0.11Ω
- HIGH dv/dt and AVALANCHE CAPABILITIES
- LOW INPUT CAPACITANCE
- LOW GATE RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS



SO-8

INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

This 200V MOSFET with a new advanced layout brings all unique advantages of MDmesh technology to lower voltages. The device exhibits worldwide lowest gate charge for any given on-resistance.Its use is therefore ideal as primary switch in isolated DC-DC converters for Telecom and Computer applications.Used in combination with secondary-side low-voltage STripFET™ products, it contributes to reducing losses and boosting efficiency

APPLICATIONS

The MDmesh™ family is very suitable for increasing power density allowing system miniaturization and higher efficiencies

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS4NM20N	S4NM20N	SO-8	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25°C Drain Current (continuous) at T_C = 100°C	4 2.83	A A
I_{DM} (2)	Drain Current (pulsed)	16	A
P_{TOT}	Total Dissipation at T_C = 25°C	2.5	W
	Derating Factor (1)	0.02	W/°C
d_v/d_t (3)	Peak Diode Recovery voltage slope	10	V/ns

THERMAL DATA

Rthj-pcb	Thermal Resistance Junction-pcb Max (1)	50	°C/W
T_j	Max. Operating Junction Temperature	150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	TBD	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 35 V)	TBD	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30 V			100	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.5	4.2	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 2 A		0.11	0.13	Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (4)	Forward Transconductance	V_{DS} = 15 V , I_D = 2 A		1.4		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		670 180 12		pF pF pF
$C_{oss\ eq.}$ (*)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		TBD		pF
R_G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		TBD		Ω

(*) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 100 V, I_D = 2 A R_G = 4.7Ω V_{GS} = 10 V (see test circuit, Figure 3)		TBD TBD		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 160 V, I_D = 4 A, V_{GS} = 10 V		19 3.5 11		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r\ (Voff)}$ t_f t_c	Off-Voltage Rise Time Fall Time Cross-Over Time	V_{DD} = 100 V, I_D = 2 A, R_G = 4.7Ω, V_{GS} = 10 V (see test circuit, Figure 3)		TBD TBD TBD		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				4	A
I_{SDM} (2)	Source-drain Current (pulsed)				16	A
V_{SD} (4)	Forward On Voltage	I_{SD} = 2 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 2 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 25°C (see test circuit, Figure 5)		89 300 6.5		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 2 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150°C (see test circuit, Figure 5)		TBD TBD TBD		ns nC A

Note: 1. When mounted on 1 inch^2 FR4 Board, 2oz of Cu, t≤ 10 sec.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 4$ A, di/dt ≤ 400 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{jMAX}$.
4. Pulsed: Pulse duration = 400 µs, duty cycle 1.5 %.

Fig. 1: Unclamped Inductive Load Test Circuit

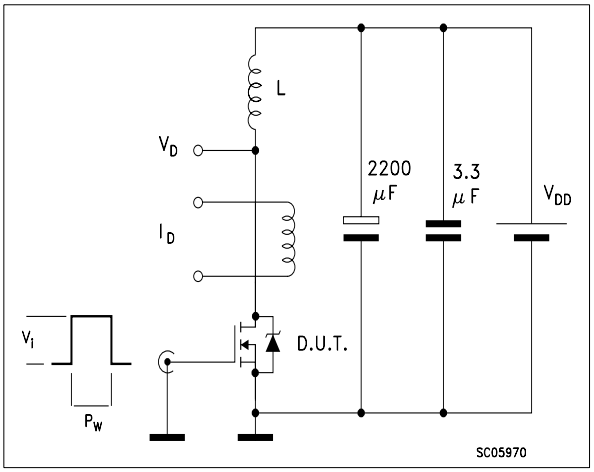


Fig. 2: Unclamped Inductive Waveform

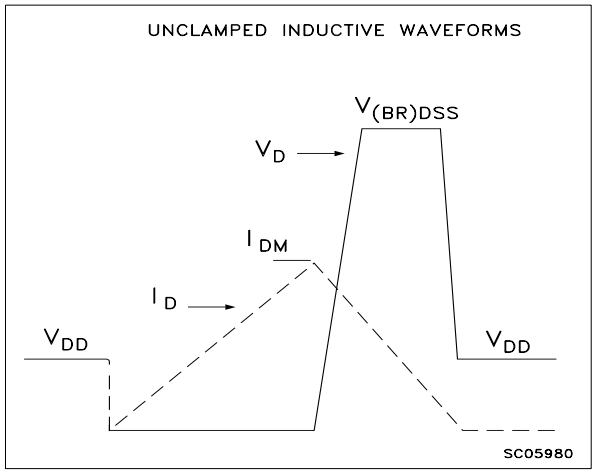


Fig. 3: Switching Times Test Circuit For Resistive Load

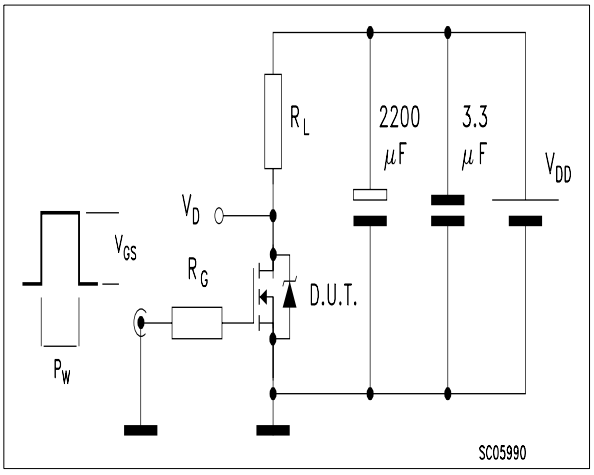


Fig. 4: Gate Charge test Circuit

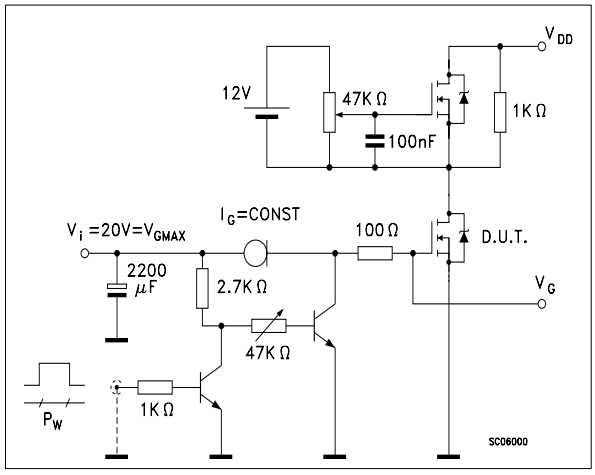
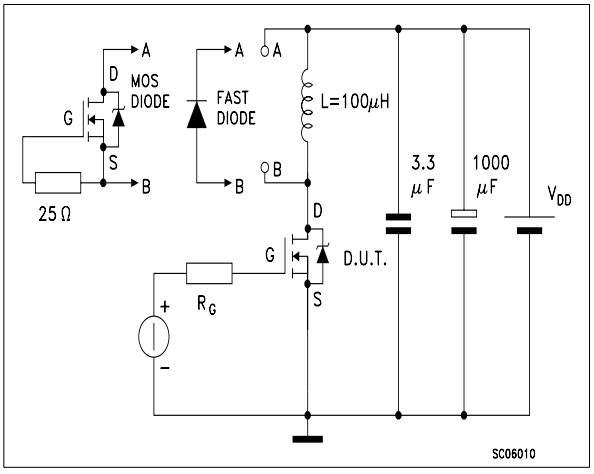
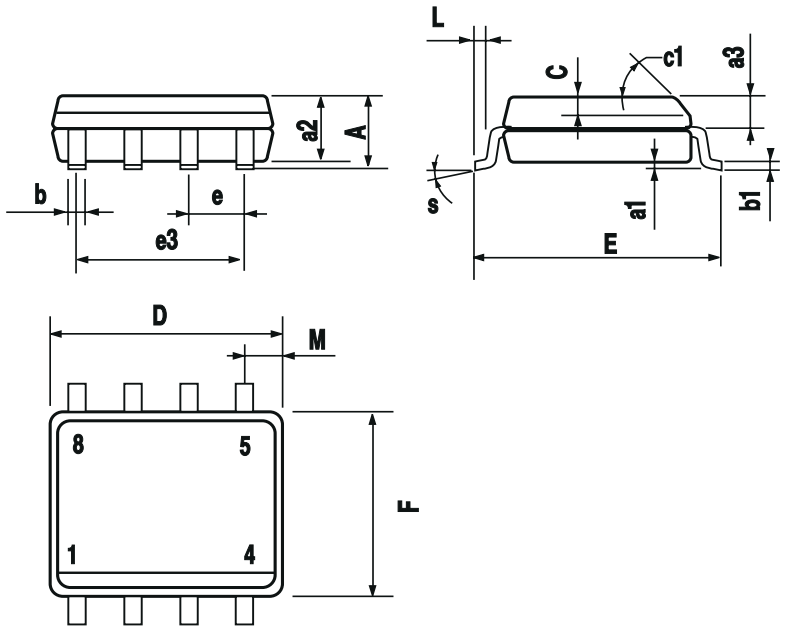


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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