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CY7C375

UltraLogic™ 128-Macrocell Flash CPLD

Features

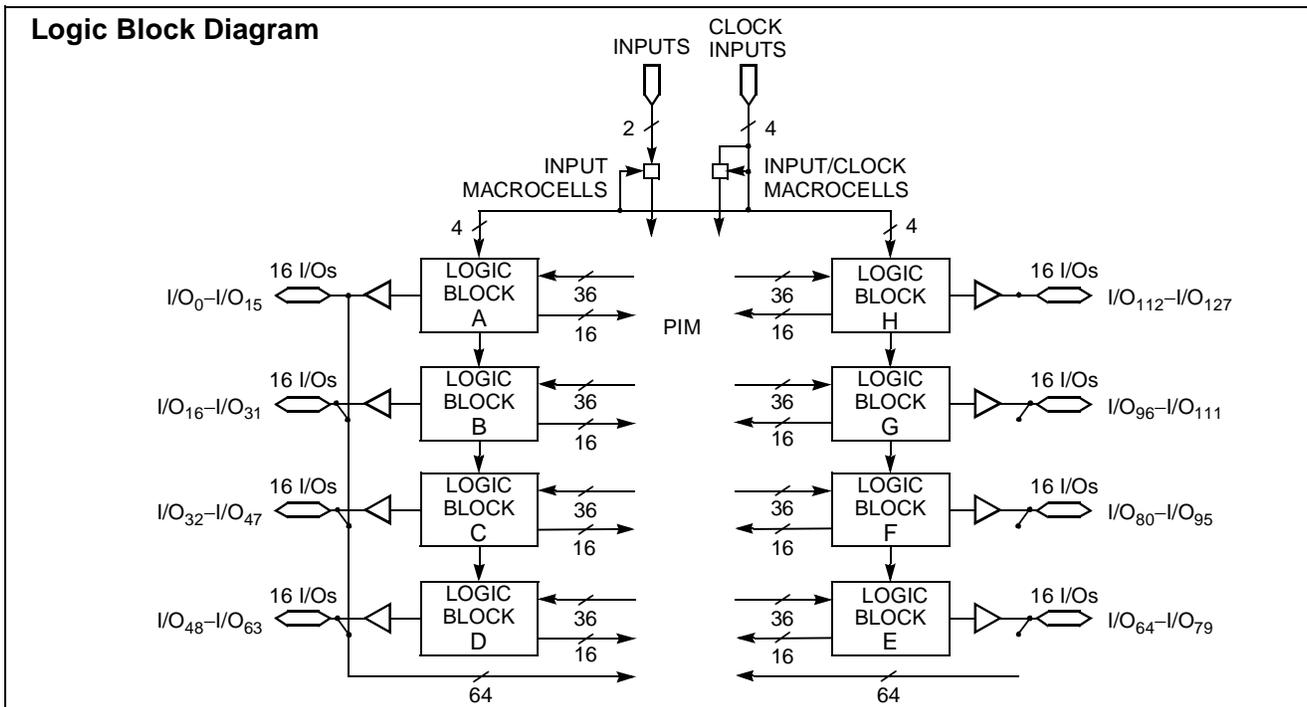
- 28 macrocells in eight logic blocks
- 28 I/O pins
- 6 dedicated inputs including 4 clock pins
- Bus Hold capabilities on all I/Os and dedicated inputs
- No hidden delays
- High speed
 - $f_{MAX} = 100 \text{ MHz}$
 - $t_{PD} = 12 \text{ ns}$
 - $t_S = 6 \text{ ns}$
 - $t_{CO} = 7 \text{ ns}$
- Electrically alterable FLASH technology
- Available in 160-pin TQFP, CQFP, and PGA packages

Functional Description

The CY7C375 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C375 is designed to bring the ease of use and high performance of the 22V10 to high-density PLDs.

The 128 macrocells in the CY7C375 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.



Selection Guide

		7C375-100	7C375-83	7C375-66	7C375L-66
Maximum Propagation Delay, t_{PD} (ns)		12	15	20	20
Minimum Set-Up, t_S (ns)		6	8	10	10
Maximum Clock to Output, t_{CO} (ns)		7	8	10	10
Maximum Supply Current, I_{CC} (mA)	Commercial	330	300	300	150
	Military/Industrial		370	370	