

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT283

4-bit binary full adder with fast carry

Product specification
File under Integrated Circuits, IC06

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74HC/HCT283

FEATURES

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT283 add two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ₁ to Σ₄) and the out-going carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the “283” can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results Σ₁ to Σ₄ and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} must be held LOW when no “carry in” is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A₁, B₁ can be assigned arbitrarily to pins 5, 6, 7, etc.

See the “583” for the BCD version.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₁ C _{IN} to Σ ₂ C _{IN} to Σ ₃ C _{IN} to Σ ₄ A _n or B _n to Σ _n C _{IN} to C _{OUT} A _n or B _n to C _{OUT}	C _L = 15 pF; V _{CC} = 5 V	16 18 20 23 21 20 20	15 21 23 27 25 23 24	ns ns ns ns ns ns ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	88	92	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

Σ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}

For HCT the condition is V_I = GND to V_{CC} – 1.5 V

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ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 1, 13, 10	Σ_1 to Σ_4	sum outputs
5, 3, 14, 12	A_1 to A_4	A operand inputs
6, 2, 15, 11	B_1 to B_4	B operand inputs
7	C_{IN}	carry input
8	GND	ground (0 V)
9	C_{OUT}	carry output
16	V_{CC}	positive supply voltage

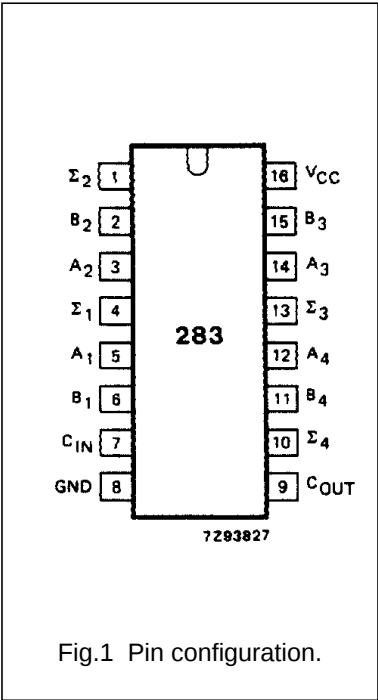


Fig.1 Pin configuration.

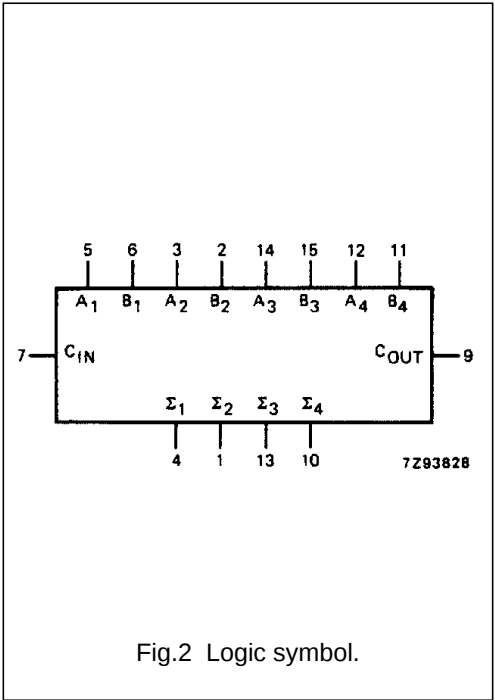


Fig.2 Logic symbol.

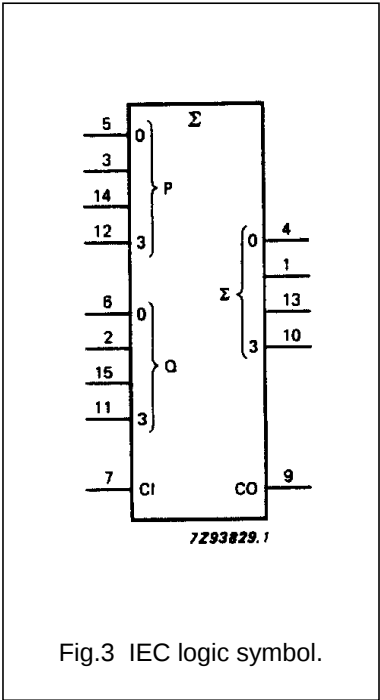


Fig.3 IEC logic symbol.

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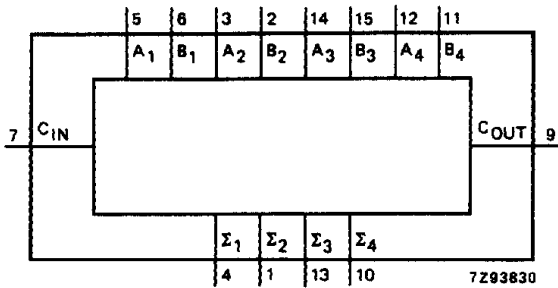


Fig.4 Functional diagram.

FUNCTION TABLE

PINS	C _{IN}	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ ₁	Σ ₂	Σ ₃	Σ ₄	C _{OUT}	EXAMPLE ⁽²⁾
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(3)
active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(4)

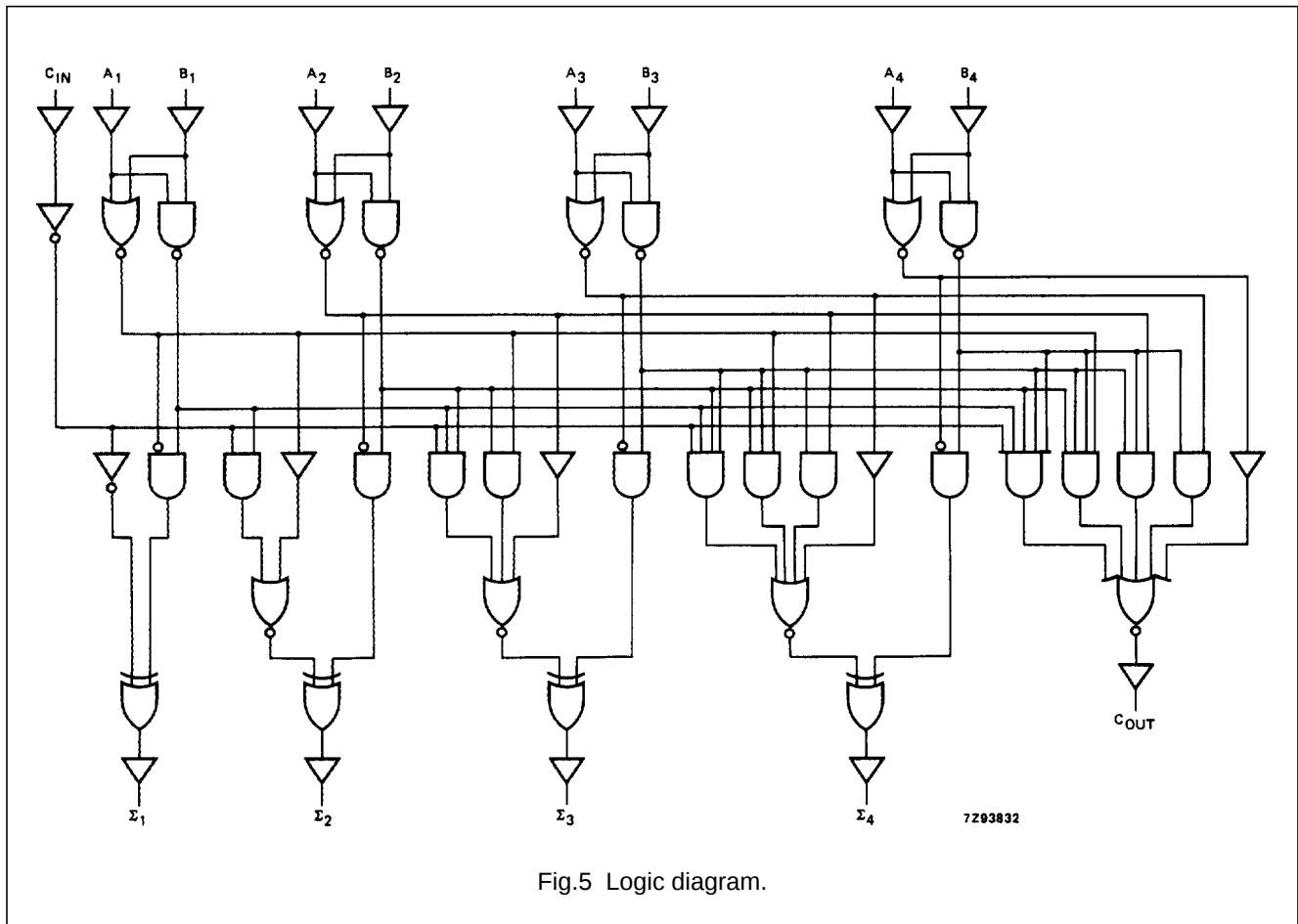
Note

1. H = HIGH voltage level
L = LOW voltage level
2. **example**
1001
1010

10011
3. for active HIGH, example = (9 + 10 = 19)
4. for active LOW, example = (carry + 6 + 5 = 12)

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₁		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₂		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₃		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₄		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay A _n or B _n to Σ _n		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay C _{IN} to C _{OUT}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay A _n or B _n to C _{OUT}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
C _{IN}	1.50
B ₂ , A ₂ , A ₁	1.00
B ₁	0.40
B ₄ , A ₄ , A ₃ , B ₃	0.50

AC CHARACTERISTICS FOR 74HCT

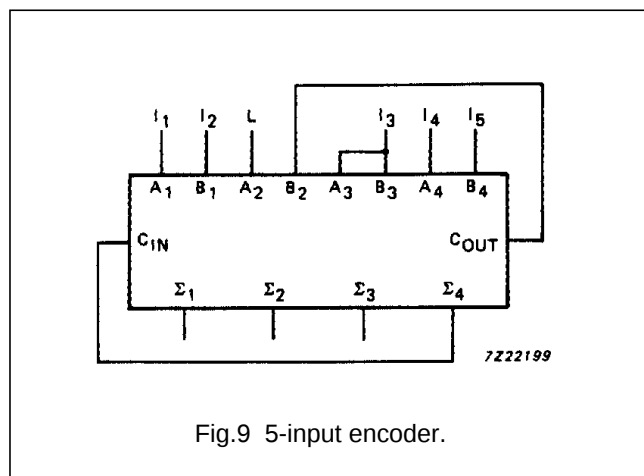
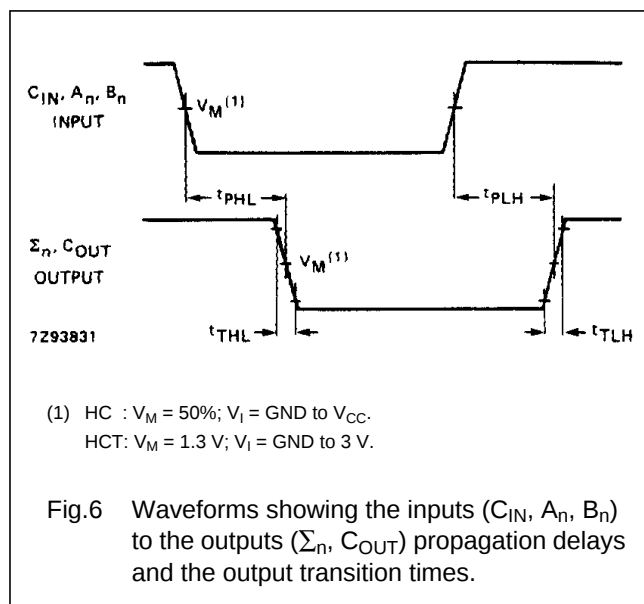
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₁		18	31		39		47	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₂		25	43		54		65	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₃		27	46		58		69	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay C _{IN} to Σ ₄		31	53		66		80	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay A _n or B _n to Σ _n		29	49		61		74	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay C _{IN} to C _{OUT}		27	46		58		69	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay A _n or B _n to C _{OUT}		28	48		60		72	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6

4-bit binary full adder with fast carry

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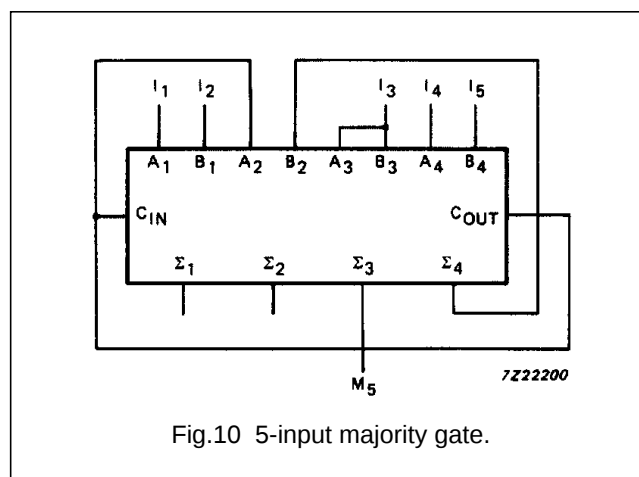
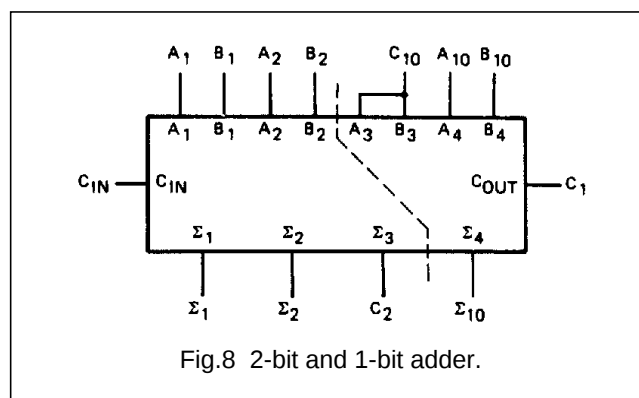
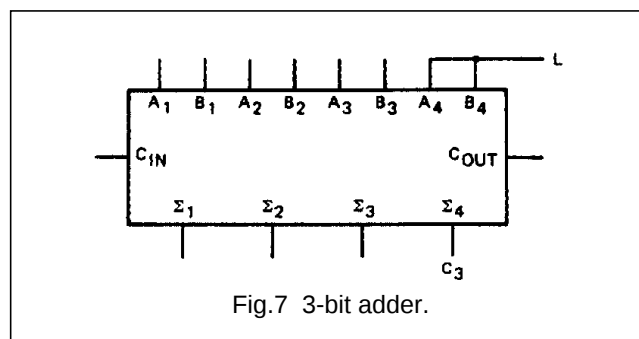
AC WAVEFORMS



Notes to Figs 7 to 10

Figure 7 shows a 3-bit adder using the "283". Tying the operand inputs of the fourth adder (A_3 , B_3) LOW makes Σ_3 dependent on, and equal to, the carry from the third adder. Based on the same principle, Figure 8 shows a method of dividing the "283" into a 2-bit and 1-bit adder. The third stage adder (A_2 , B_2 , Σ_2) is used simply as means of transferring the carry into the fourth stage (via A_2 and B_2) and transferring the carry from the second stage on Σ_2 . Note that as long as A_2 and B_2 are the same, HIGH or LOW, they do not influence Σ_2 . Similarly, when A_2 and B_2 are the same, the carry into the third stage does not influence the carry out of the third stage. Figure 9 shows a method of implementing a 5-input encoder, where the

APPLICATION INFORMATION



inputs are equally weighted. The outputs Σ_0 , Σ_1 and Σ_2 produce a binary number equal to the number inputs (I_1 to I_5) that are HIGH. Figure 10 shows a method of implementing a 5-input majority gate. When three or more inputs (I_1 to I_5) are HIGH, the output M_5 is HIGH.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".