SIEMENS

1M × 64-Bit Dynamic RAM Module

HYM 641010GS-60/-70
HYM 641020GS-60/-70

Preliminary Information

- 1 048 576 words by 64-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability with
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 9680 mW active (-60 version)
  max. 8800 mW active (-70 version)
  CMOS – 451 mW standby
  TTL – 550 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only-refresh
- 16 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully TTL compatible
- 4 Byte interleave enabled, Dual Address inputs (A0/B0)
- Buffered inputs except $\overline{\text{RAS}}$ and DQ
- 168 pin, dual read-out, Single in-Line Memory Module
- Utilizes sixteen 1M × 4 - DRAMs (HYB 514400BJ/BT) and four BiCMOS 8-bit buffers/line drivers 74ABT244
- Two version:
  HYM 641010S with SOJ-components
  (8.89 mm module thickness
  HYM 641020GS with TSOPII-components
  (4.06 mm module thickness)
- 1024 refresh cycles / 16 ms
- Gold contact pad
- double sided module with 25.35 mm (1000 mil) height

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 641020GS-60	Q67100 - Q2003	L-DIM-168-1	60 ns DRAM module
HYM 641020GS-70	on request	L-DIM-168-1	70 ns DRAM module
HYM 641010GS-60	Q67100 - Q2002	L-DIM-168-1	60 ns DRAM module
HYM 641010GS-70	on request	L-DIM-168-1	70 ns DRAM module

The HYM 641010/20GS-60/-70 is a 8 M Byte DRAM module organized as 1 048 576 words by 64-bit in a 168-pin, dual read-out, single-in-line package comprising sixteen HYB 514400BJ/BT 1M $\times$ 4 DRAMs in 300 mil wide SOJ or TSOPII - packages mounted together with sixteen 0.2 µF ceramic decoupling capacitors on a PC board. All inputs except $\overline{RAS}$ and DQ are buffered by using four BiCMOS 8-bit buffers/line drivers.

Each HYB 514400BJ/BT is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

Pin Definitions and Functions

Pin No	Function
A0-A9,B0	Address Input
DQ0 - DQ63	Data Input/Output
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$	Read / Write Input
$\overline{OE0}$, $\overline{OE2}$	Output Enable
V_{cc}	Power (+ 5 V)
V_{ss}	Ground
PD1 - PD8	Presence Detect Pins
PDE	Presence Detect Enable
ID0 , ID1	ID indentification bit
N.C.	No Connection

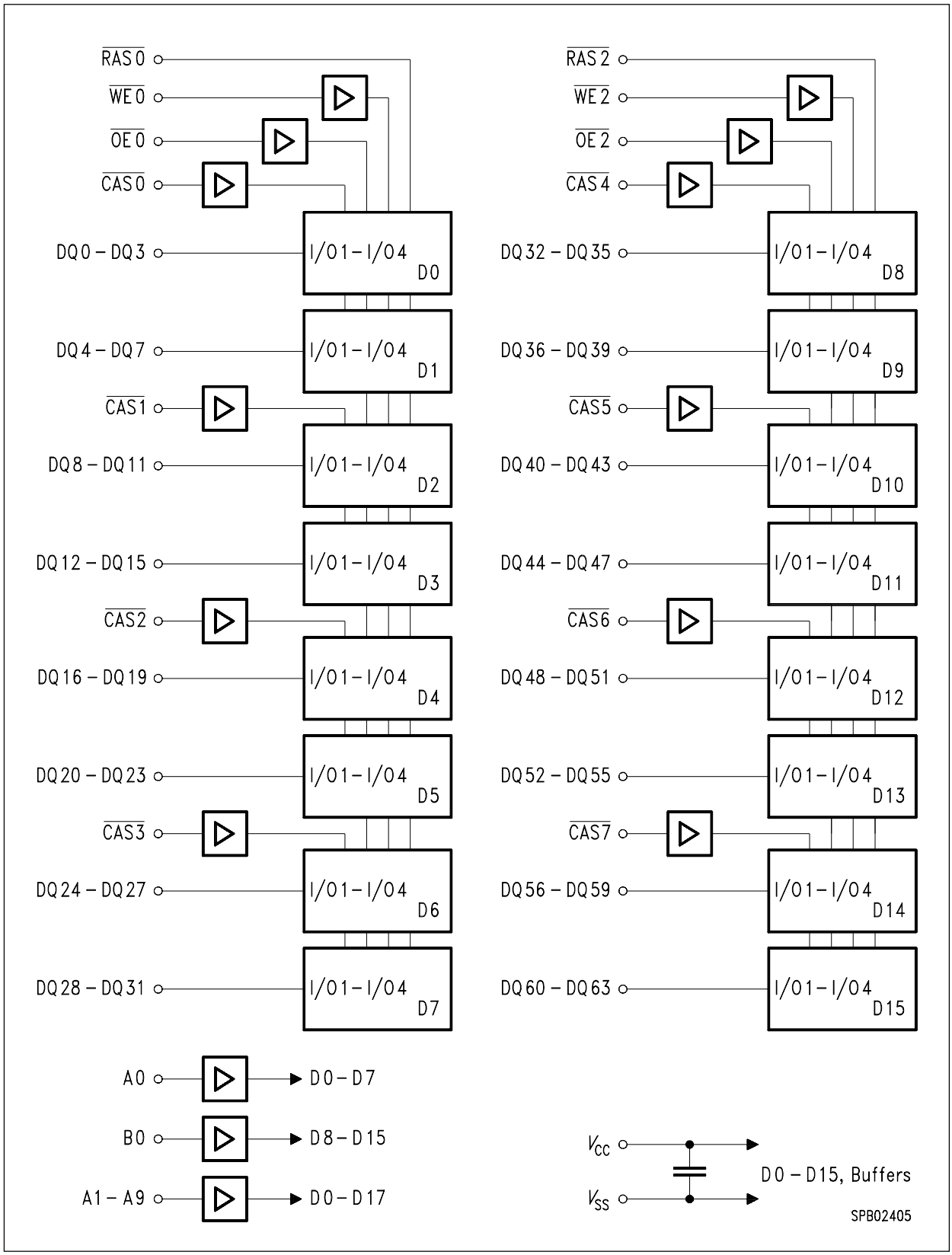
Presence-Detect and ID-pin Thruth Table:

Module	ID0	ID1	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8
HYM 641010/20GS-60	V_{ss}	V_{ss}	0	0	1	0	0	1	1	1
HYM 641010/20GS-70	V_{ss}	V_{ss}	0	0	1	0	0	0	1	1

Note: 1= high level (driver output), 0 = low level (driver output) for $\overline{PDE}$ active (ground) . For $\overline{PDE}$ at a high level all PD terminals are in tri-state.

Pin Configuration

PIN #	Symbol	PIN #	Symbol		PIN #	Symbol	PIN #	Symbol
1	V_{ss}	43	V_{ss}		85	V_{ss}	127	V_{ss}
2	DQ0	44	OE2		86	DQ32	128	NC
3	DQ1	45	RAS2		87	DQ33	129	NC
4	DQ2	46	CAS4		88	DQ34	130	CAS5
5	DQ3	47	CAS6		89	DQ35	131	CAS7
6	V_{CC}	48	WE2		90	V_{CC}	132	PDE
7	DQ4	49	V_{CC}		91	DQ36	133	V_{CC}
8	DQ5	50	NC		92	DQ37	134	NC
9	DQ6	51	NC		93	DQ38	135	NC
10	DQ7	52	DQ16		94	DQ39	136	DQ48
11	NC	53	DQ17		95	NC	137	DQ49
12	V_{ss}	54	V_{ss}		96	V_{ss}	138	V_{ss}
13	DQ8	55	DQ18		97	DQ40	139	DQ50
14	DQ9	56	DQ19		98	DQ41	140	DQ51
15	DQ10	57	DQ20		99	DQ42	141	DQ52
16	DQ11	58	DQ21		100	DQ43	142	DQ53
17	DQ12	59	V_{CC}		101	DQ44	143	V_{CC}
18	V_{CC}	60	DQ22		102	V_{CC}	144	DQ54
19	DQ13	61	NC		103	DQ45	145	NC
20	DQ14	62	NC		104	DQ46	146	NC
21	DQ15	63	NC		105	DQ47	147	NC
22	NC	64	NC		106	NC	148	NC
23	V_{ss}	65	DQ23		107	V_{ss}	149	DQ55
24	NC	66	NC		108	NC	150	NC
25	NC	67	DQ24		109	NC	151	DQ55
26	V_{CC}	68	V_{ss}		110	V_{CC}	152	V_{ss}
27	WE0	69	DQ25		111	NC	153	DQ57
28	CAS0	70	DQ26		112	CAS1	154	DQ58
29	CAS2	71	DQ27		113	CAS3	155	DQ59
30	RAS0	72	DQ28		114	NC	156	DQ60
31	OE0	73	V_{CC}		115	NC	157	V_{CC}
32	V_{ss}	74	DQ29		116	V_{ss}	158	DQ61
33	A0	75	DQ30		117	A1	159	DQ62
34	A2	76	DQ31		118	A3	160	DQ63
35	A4	77	NC		119	A5	161	NC
36	A6	78	V_{ss}		120	A7	162	V_{ss}
37	A8	79	PD1		121	A9	163	PD2
38	NC	80	PD3		122	NC	164	PD4
39	NC	81	PD5		123	NC	165	PD6
40	V_{CC}	82	PD7		124	V_{CC}	166	PD8
41	NC	83	ID0		125	NC	167	ID1
42	NC	84	V_{CC}		126	B0	168	V_{CC}



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 ˚C
Storage temperature range..... – 55 to + 125 ˚C
Soldering temperature ..... 260 ˚C
Soldering time..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage..... – 1 to + 7 V
Power dissipation..... 12,32 W
Data out current (short circuit) ..... 50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics [1)]

T_A = 0 to 70 ˚C; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	5.5	V	–
Input low voltage	V_{IL}	– 1.0	0.8	V	–
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	–
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	–
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	–
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	–
Average V_{CC} supply current: HYM 641010/20GS-60 HYM 641010/20GS-70 ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	I_{CC1}	 – –	 1760 1600	 mA mA	2), 3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	50	mA	–
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles: HYM 641010/20GS-60 HYM 641010/20GS-70 ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	I_{CC3}	 – –	 1760 1600	 mA mA	2)

DC Characteristics (cont'd) [1)]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode:	I_{CC4}				[2), 3)]
HYM 641010/20GS-60		–	1120	mA	
HYM 641010/20GS-70		–	1120	mA	
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	30	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				[1)]
HYM 641010/20GS-60		–	1760	mA	
HYM 641010/20GS-70		–	1600	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					

Capacitance
T_A = 0 to 70 ˚C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9,B0)	C_{I1}	–	20	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	80	pF
Input capacitance ($\overline{CAS0}$-$\overline{CAS7}$)	C_{I3}	–	20	pF
Input capacitance ($\overline{WE0}$,$\overline{WE2}$,$\overline{OE0}$,$\overline{OE2}$)	C_{I4}	–	20	pF
I/O capacitance (DQ0-DQ63)	C_{IO1}	–	20	pF

AC Characteristics [4) 5)14)]

T_A = 0 to 70 ˚C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 641010/20GS-60		HYM 641010/20GS-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	ns
Fast page mode cycle time	t_{PC}	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11) 12)]	t_{RAC}	–	60	–	70	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	15	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	200000	70	200000	ns
$\overline{CAS}$ precharge to $\overline{RAS}$ delay	t_{RHCP}	35	–	40	–	ns
$\overline{RAS}$ hold time	t_{RSH}	15	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	45	20	50	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	ns

AC Characteristics (cont'd) [4) 5)14)]

T_A = 0 to 70 ˚C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values				Unit
		HYM 641010/20GS-60		HYM 641010/20GS-70		
		min.	max.	min.	max.	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	ns
Read command setup time	t_{RCS}	0	–	0	–	ns
Read command hold time [8)]	t_{RCH}	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8)]	t_{RRH}	0	–	0	–	ns
Write command hold time	t_{WCH}	10	–	15	–	ns
Write command pulse width	t_{WP}	10	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	15	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	15	–	20	–	ns
Data setup time [9)]	t_{DS}	0	–	0	–	ns
Data hold time [9)]	t_{DH}	15	–	15	–	ns
Refresh period	t_{REF}	–	16	–	16	ms
Write command setup time [10)]	t_{WCS}	0	–	0	–	ns
$\overline{CAS}$ setup time [13)]	t_{CSR}	5	–	5	–	ns
$\overline{CAS}$ hold time [13)]	t_{CHR}	15	–	15	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	ns
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns
Write to $\overline{RAS}$ precharge time [13)]	t_{WRP}	10	–	10	–	ns
Write to time ref. to $\overline{RAS}$ [13)]	t_{WRH}	10	–	10	–	ns

Notes

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles out of which at least one cycle has to be a refresh cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalant of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{\text{CAS}}$ leading edge.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

13) For $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycles only.

14) A $\pm$ 2 ns timing skew has to be added to all values due to the use of the buffers / line drivers