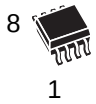
# M41T56

## 512 bit (64b x8) Serial Access TIMEKEEPER® SRAM

- 5V ± 10% SUPPLY VOLTAGE
- COUNTERS for SECONDS, MINUTES, HOURS, DAY, DATE, MONTH, YEARS and CENTURY
- YEAR 2000 COMPLIANT
- SOFTWARE CLOCK CALIBRATION
- AUTOMATIC POWER-FAIL DETECT and SWITCH CIRCUITRY
- $I^2C$ BUS COMPATIBLE
- 56 BYTES of GENERAL PURPOSE RAM
- ULTRA-LOW BATTERY SUPPLY CURRENT of 500nA
- LOW OPERATING CURRENT of 300µA
- OPERATING TEMPERATURE of –40 to 85°C
- AUTOMATIC LEAP YEAR COMPENSATION
- SPECIAL SOFTWARE PROGRAMMABLE OUTPUT




SO8 (M)
150mil Width

**DESCRIPTION**

The M41T56 TIMEKEEPER® is a low power 512 bit static CMOS RAM organized as 64 words by 8 bits. A built-in 32.768 kHz oscillator (external crystal controlled) and the first 8 bytes of the RAM are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. Addresses and data are transferred serially via a two-line bi-directional bus. The built-in address register is incremented automatically after each write or read data byte.

**Table 1. Signal Names**

| | |
|---|---|
| OSCI | Oscillator Input |
| OCSO | Oscillator Output |
| FT/OUT | Frequency Test / Output Driver (Open Drain) |
| SDA | Serial Data Address Input / Output |
| SCL | Serial Clock |
| $V_{BAT}$ | Battery Supply Voltage |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |

**Figure 1. Logic Diagram**

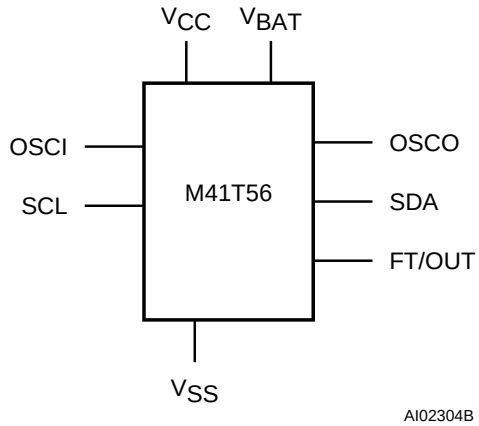


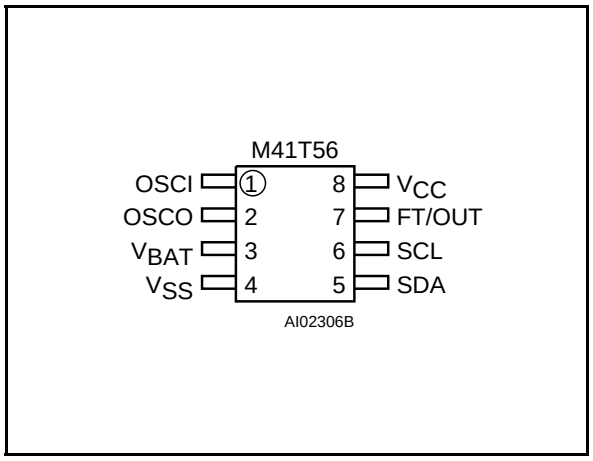
**Table 2. Absolute Maximum Ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | –40 to 85 | °C |
| $T_{STG}$ | Storage Temperature ($V_{CC}$ Off, Oscillator Off) | –55 to 125 | °C |
| $V_{IO}$ | Input or Output Voltages | –0.3 to 7 | V |
| $V_{CC}$ | Supply Voltage | –0.3 to 7 | V |
| $I_O$ | Output Current | 20 | mA |
| $P_D$ | Power Dissipation | 0.25 | W |

**Note:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

***CAUTION:*** *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

**Figure 2. SOIC Pin Connections**




**DESCRIPTION** (cont'd)

The M41T56 clock has a built-in power sense circuit which detects power failures and automatically switches to the battery supply during power failures. The energy needed to sustain the RAM and clock operations can be supplied from a small lithium coin cell.

Typical data retention time is in excess of 10 years with a 50mAh 3V lithium cell. The M41T56 is supplied in 8 lead Plastic SOIC package.

**OPERATION**

The M41T56 clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 64 bytes contained in the device can then be accessed sequentially in the following order:

1. Seconds Register
2. Minutes Register
3. Century/Hours Register
4. Day Register
5. Date Register
6. Month Register
7. Years Register
8. Control Register

9 to 64. RAM

The clock continually monitors $V_{CC}$ for an out of tolerance condition. Should $V_{CC}$ fall below $V_{PFD}$, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When $V_{CC}$ falls below $V_{BAT}$, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. Upon power-up, the device switches from battery to $V_{CC}$ at $V_{BAT}$ and recognizes inputs when $V_{CC}$ goes above $V_{PFD}$ volts.

**Figure 3. Block Diagram**

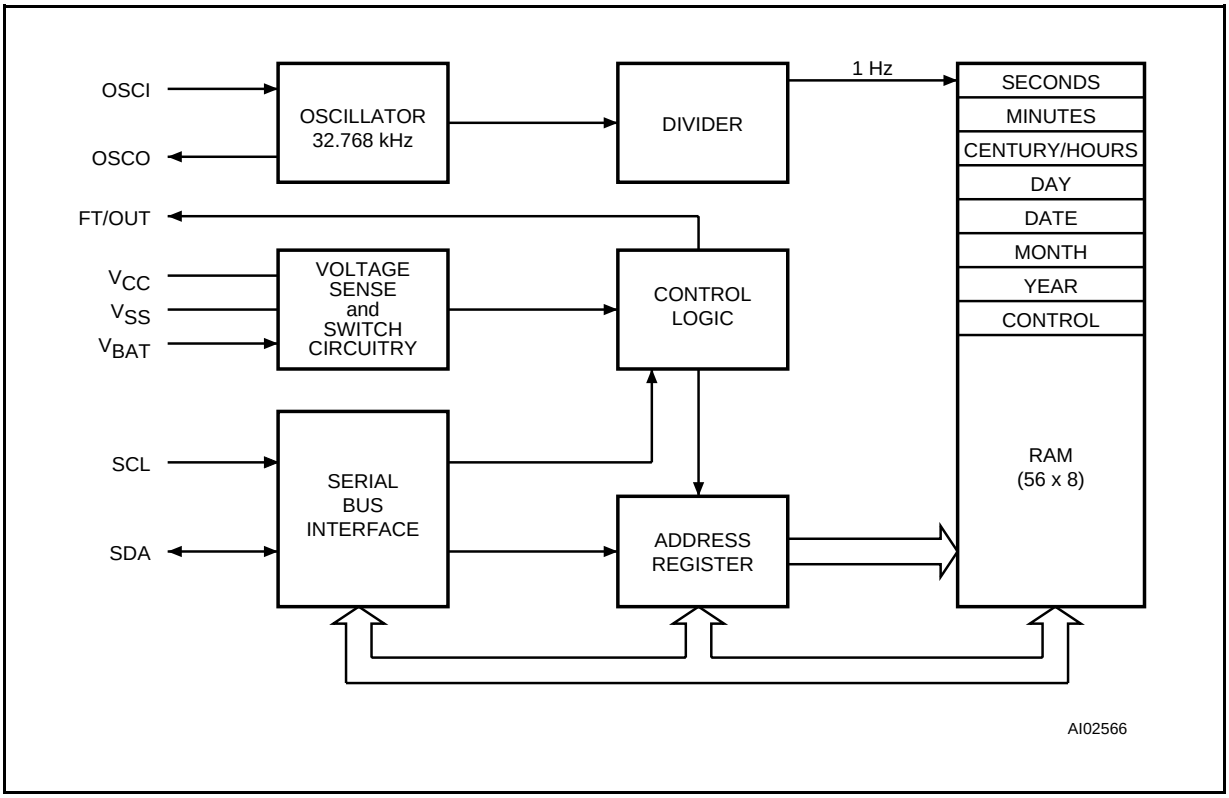



**Table 3. Register Map**

| Address | Data | | | | | | | | Function/Range BCD Format | |
|---|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | ST | 10 Seconds | | | Seconds | | | | Seconds | 00-59 |
| 1 | X | 10 Minutes | | | Minutes | | | | Minutes | 00-59 |
| 2 | CEB (1) | CB | 10 Hours | | Hours | | | | Century/Hour | 0-1/00-23 |
| 3 | X | X | X | X | X | Day | | | Day | 01-07 |
| 4 | X | X | 10 Date | | Date | | | | Date | 01-31 |
| 5 | X | X | X | 10 M. | Month | | | | Month | 01-12 |
| 6 | 10 Years | | | | Years | | | | Year | 00-99 |
| 7 | OUT | FT | S | Calibration | | | | | Control | |

**Keys:** **S** = SIGN Bit; **FT** = FREQUENCY TEST Bit; **ST** = STOP Bit; **OUT** = Output level; **X** = Don't care; **CEB** = Century Enable Bit; **CB** = Century Bit.

**Note:** 1. When **CEB** is set to '1', **CB** will toggle from '0' to '1' or from '1' to '0' every 100 years (dependent upon the initial value set). When **CEB** is set to '0', **CB** will not toggle.

**Table 4. AC Measurement Conditions**

| | |
|---|---|
| Input Rise and Fall Times | ≤ 5ns |
| Input Pulse Voltages | 0 to 3V |
| Input and Output Timing Ref. Voltages | 1.5V |

Note that Output Hi-Z is defined as the point where data is no longer driven.

## 2-WIRE BUS CHARACTERISTICS

This bus is intended for communication between different ICs. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

– Data transfer may be initiated only when the bus is not busy.

– During data transfer, the data line must remain stable whenever the clock line is High.

– Changes in the data line while the clock line is High will be interpreted as control signals.

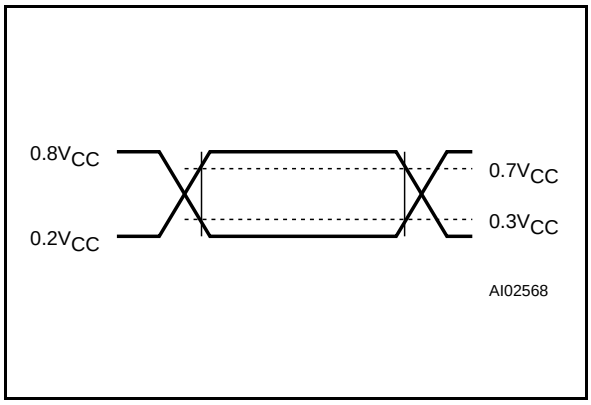
Accordingly, the following bus conditions have been defined:

**Bus not busy.** Both data and clock lines remain High.

**Start data transfer.** A change in the state of the data line, from High to Low, while the clock is High, defines the START condition.

**Stop data transfer.** A change in the state of the data line, from Low to High, while the clock is High, defines the STOP condition.

**Figure 4. AC Testing Load Circuit**




**Data valid.** The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition, a device that gives out a message is called "transmitter", the receiving device that gets the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

**Table 5. Capacitance (1,2)**
($T_A$ = 25 °C, f = 1 MHz )

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance (SCL) | | 7 | pF |
| $C_{OUT}$ (3) | Output Capacitance (SDA, FT/OUT) | | 10 | pF |
| $t_{LP}$ | Low-pass filter input time constant (SDA and SCL) | 0.25 | 1 | µs |

**Notes:** 1. Effective capacitance measured with power supply at 5V.
2. Sampled, not 100% tested.
3. Outputs deselected.

**Table 6. DC Characteristics**
($T_A$ = –40 to 85°C; $V_{CC}$ = 4.5V to 5.5V)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | | ±1 | µA |
| $I_{CC1}$ | Supply Current | Switch Frequency = 100kHz | | | 300 | µA |
| $I_{CC2}$ | Supply Current (Standby) | SCL, SDA = $V_{CC}$ – 0.3V | | 100 | | µA |
| $V_{IL}$ | Input Low Voltage | | –0.3 | | 1.5 | V |
| $V_{IH}$ | Input High Voltage | | 3 | | $V_{CC}$ + 0.8 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 5mA, $V_{CC}$ = 4.5V | | | 0.4 | V |
| $V_{BAT}$(1) | Battery Supply Voltage | | 2.5 | 3 | 3.5 | V |
| $I_{BAT}$ | Battery Supply Current | $T_A$ = 25°C, $V_{CC}$ = 0V, Oscillator ON, $V_{BAT}$ = 3V | | 450 | 550 | nA |

**Note:** 1. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) as the battery supply.

**Table 7. Power Down/Up Trip Points DC Characteristics (1)**
($T_A$ = –40 to 85°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{PFD}$ | Power-fail Deselect Voltage | 1.2 $V_{BAT}$ | 1.25 $V_{BAT}$ | 1.285 $V_{BAT}$ | V |
| $V_{SO}$ | Battery Back-up Switchover Voltage | | $V_{BAT}$ | | V |

**Note:** 1. All voltages referenced to $V_{SS}$.

**Table 8. Crystal Electrical Characteristics**
(Externally Supplied)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_O$ | Resonant Frequency | | 32.768 | | kHz |
| $R_S$ | Series Resistance | | | 35 | kΩ |
| $C_L$ | Load Capacitance | | 12.5 | | pF |

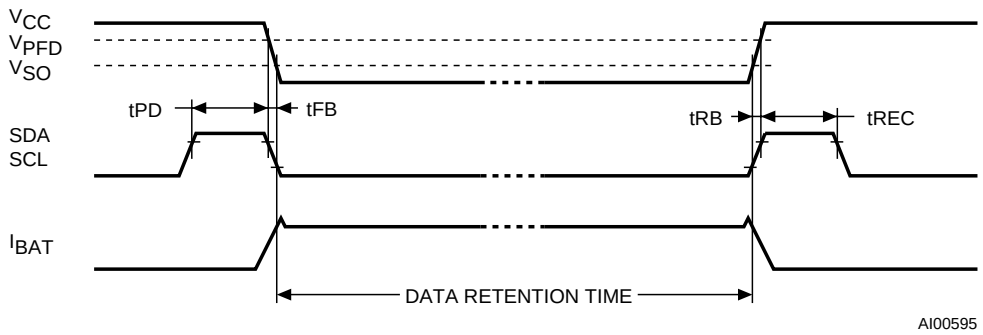
**Notes:** Load capacitors are integrated within the M41T56. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

*STMicroelectronics recommends the KDS DT-38 Tuning Fork Type quartz crystal for industrial temperature operations. KDS can be contacted at 913-491-6825 or http://www.kdsj.co.jp for further information on this crystal type.*

**Table 9. Power Down/Up Mode AC Characteristics**
($T_A$ = –40 to 85°C)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PD}$ | SCL and SDA at $V_{IH}$ before Power Down | 0 | | ns |
| $t_{FB}$ | $V_{PFD}$ (min) to $V_{SO}$ $V_{CC}$ Fall Time | 300 | | µs |
| $t_{RB}$ | $V_{SO}$ to $V_{PFD}$ (min) $V_{CC}$ Rise Time | 100 | | µs |
| $t_{REC}$ | SCL and SDA at $V_{IH}$ after Power Up | 200 | | µs |

**Figure 5. Power Down/Up Mode AC Waveforms**




**2-WIRE BUS CHARACTERISTICS** (cont'd)

**Acknowledge.** Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

**Table 10. AC Characteristics**
($T_A$ = –40 to 85°C; $V_{CC}$ = 4.5V to 5.5V)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{SCL}$ | SCL Clock Frequency | 0 | 100 | kHz |
| $t_{LOW}$ | Clock Low Period | 4.7 | | µs |
| $t_{HIGH}$ | Clock High Period | 4 | | µs |
| $t_R$ | SDA and SCL Rise Time | | 1 | µs |
| $t_F$ | SDA and SCL Fall Time | | 300 | ns |
| $t_{HD:STA}$ | START Condition Hold Time (after this period the first clock pulse is generated) | 4 | | µs |
| $t_{SU:STA}$ | START Condition Setup Time (only relevant for a repeated start condition) | 4.7 | | µs |
| $t_{SU:DAT}$ | Data Setup Time | 250 | | ns |
| $t_{HD:DAT}$ (1) | Data Hold Time | 0 | | µs |
| $t_{SU:STO}$ | STOP Condition Setup Time | 4.7 | | µs |
| $t_{BUF}$ | Time the bus must be free before a new transmission can start | 4.7 | | µs |

**Note:** 1. Transmitter must internally provide a hold time to bridge the undefined region (300ns max.) of the falling edge of SCL.

### WRITE MODE

In this mode the master transmitter transmits to the M41T56 slave receiver. Bus protocol is shown in Figure 10. Following the START condition and slave address, a logic '0' ($R/\overline{W}$ = 0) is placed on the bus and indicates to the addressed device that word address $A_n$ will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge clock. The M41T56 slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address and again after it has received the word address and each data byte (see Figure 9).

### READ MODE

In this mode, the master reads the M41T56 slave after setting the slave address (see Figure 11). Following the write mode control bit ($R/\overline{W}$ = 0) and the acknowledge bit, the word address $A_n$ is written to the on-chip address pointer. Next the START condition and slave address are repeated, followed by the READ mode control bit ($R/\overline{W}$ = 1). At this point, the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The M41T56 slave transmitter will now place the data byte at address An + 1 on the bus. The master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented, whereby the master reads the M41T56 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer, see Figure 12.

**Figure 6. Serial Bus Data Transfer Sequence**

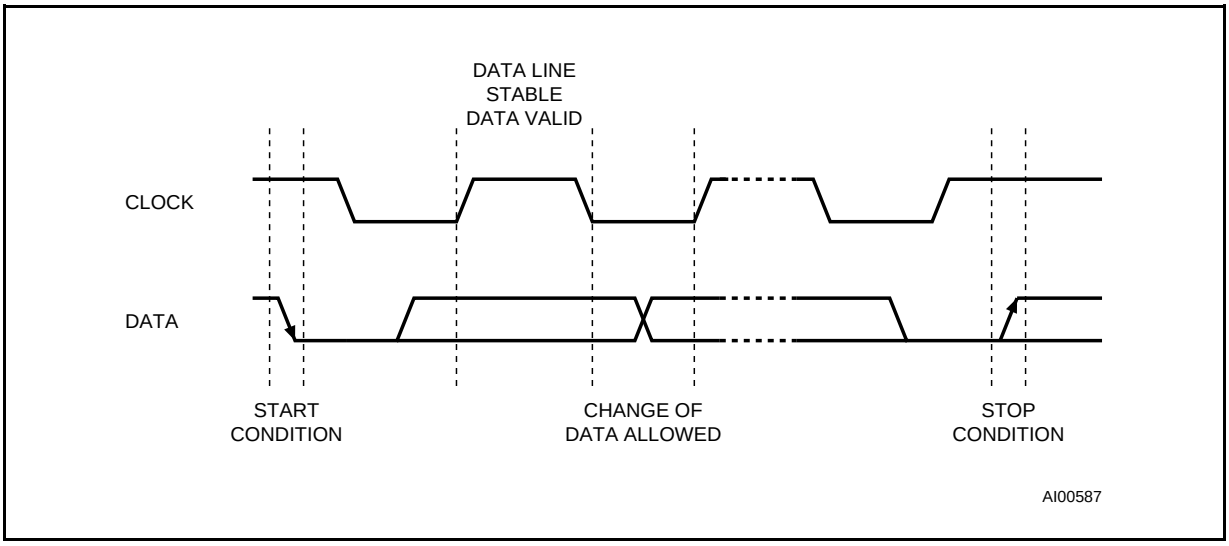
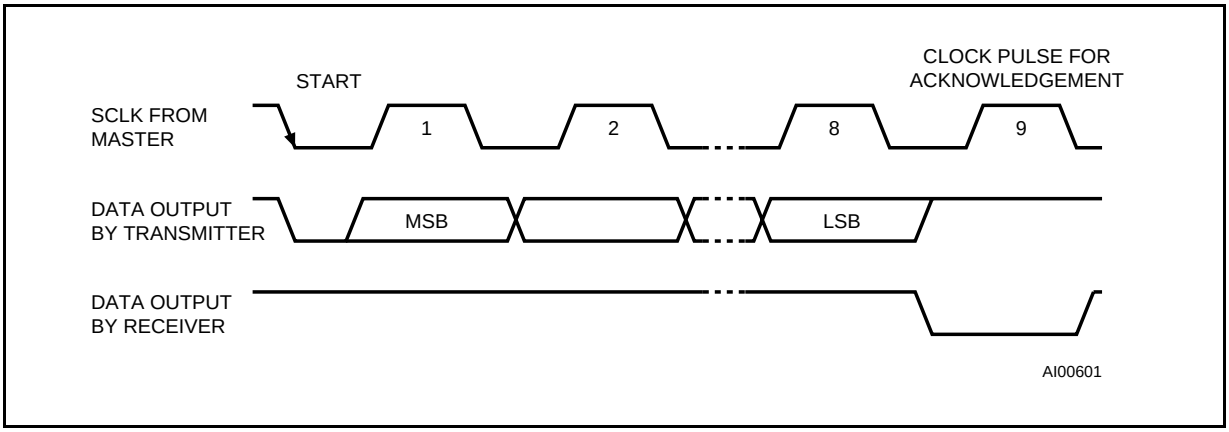



**Figure 7. Acknowledgement Sequence**



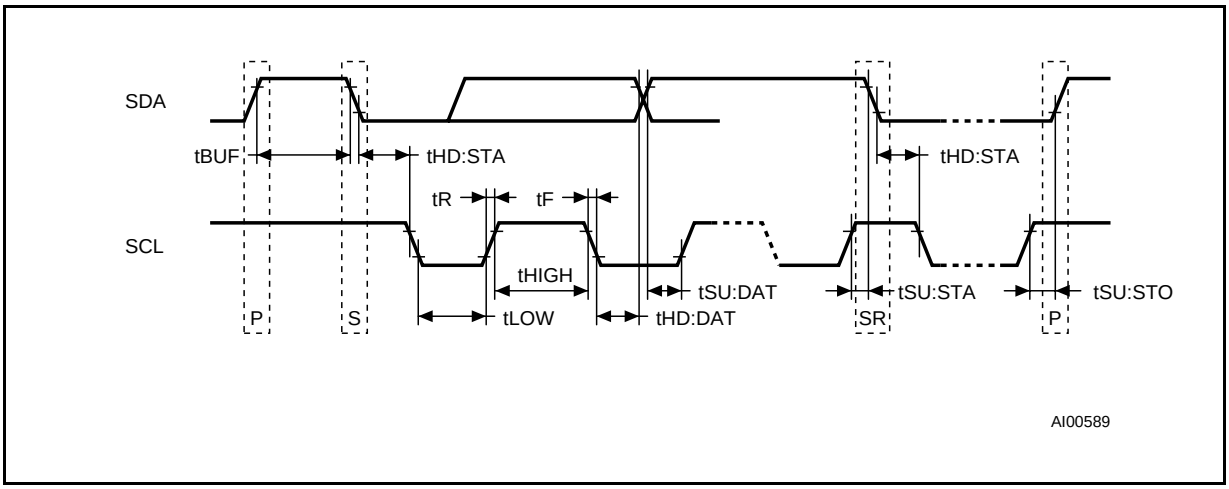

## CLOCK OPERATION

The eight byte clock register (see Table 3) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Seconds, Minutes, and Hours are contained within the first three registers. Bits D6 and D7 of clock register 2 (Hours Register) contain the CENTURY ENABLE Bit (CEB) and the CENTURY Bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0', CB will not toggle. Bits D0 through D2 of register 3 contain the Day (day of week). Registers 4, 5 and 6 contain the Date (day of month), Month and Years. The final register is the Control Register (this is described in the Clock Calibration section). Bit D7 of register 0 contains the STOP Bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The seven Clock Registers may be read one byte at a time, or in a sequential block. The Control Register (Address location 7) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be delayed by 250ms to allow the read to be completed before the update occurs. This will prevent a transition of data during the read.

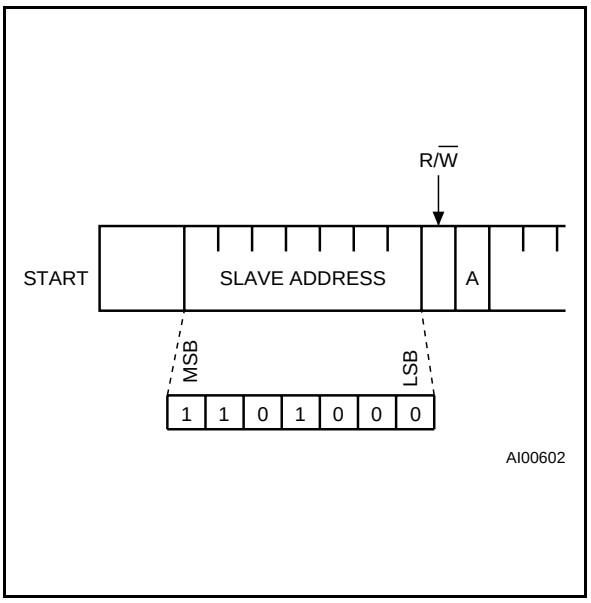
Note: This 250ms delay affects only the clock register update and does not alter the actual clock time.

**Figure 8. Bus Timing Requirements Sequence**




**Note:** P = STOP and S = START

**Figure 9. Slave Address Location**




## CLOCK CALIBRATION

The M41T56 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ± 1.53 minutes per month. With the calibration bits properly set, the accuracy of each M41T56 improves to better than +1/–2 ppm at 25°C.

The oscillation rate of any crystal changes with temperature (see Figure 14). Most clock chips compensate for crystal frequency and temperature shift error with cumbersome trim capacitors. The M41T56 design, however, employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 13. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five bit Calibration byte found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration byte occupies the five lower order bits (D4-D0) in the Control register (Addr 7). This byte can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minutes cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is + 4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is in fact running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

**Figure 10. Write Mode Sequence**

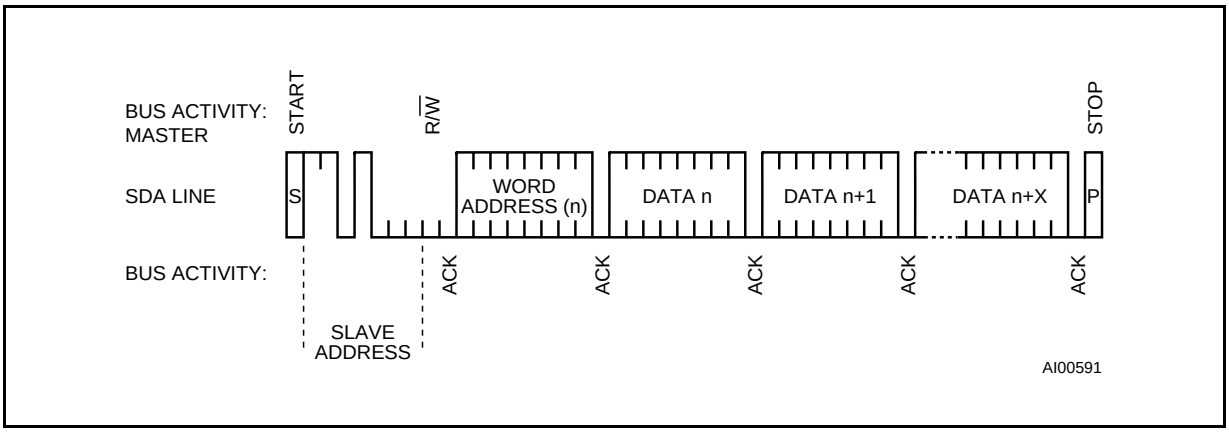



**Figure 11. Read Mode Sequence**

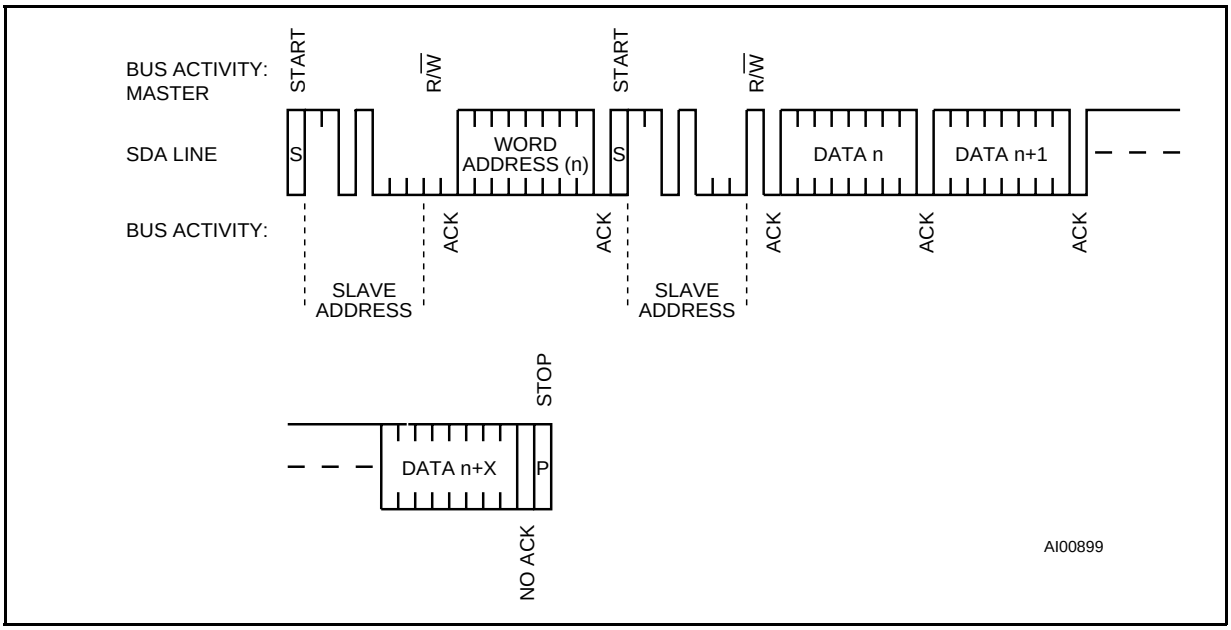



**Figure 12. Alternate Read Mode Sequence**

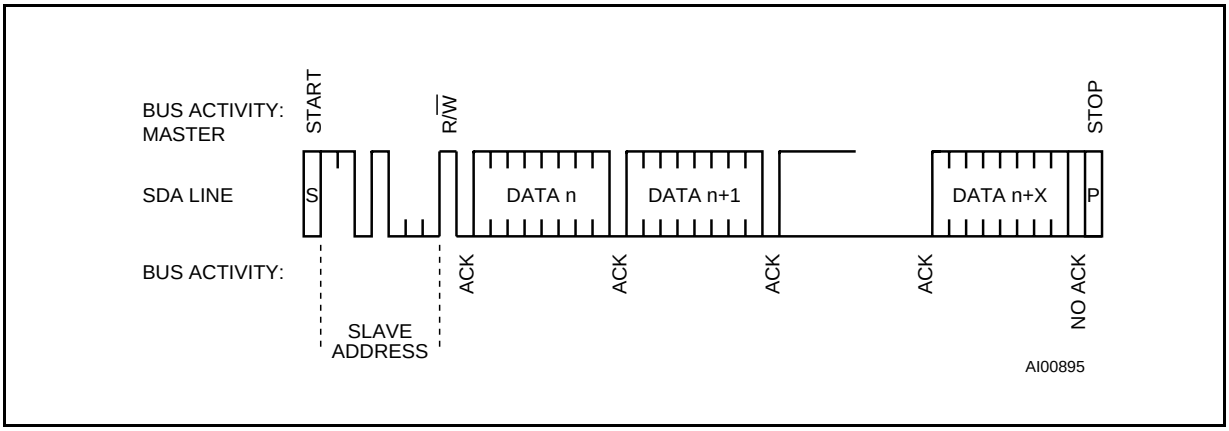
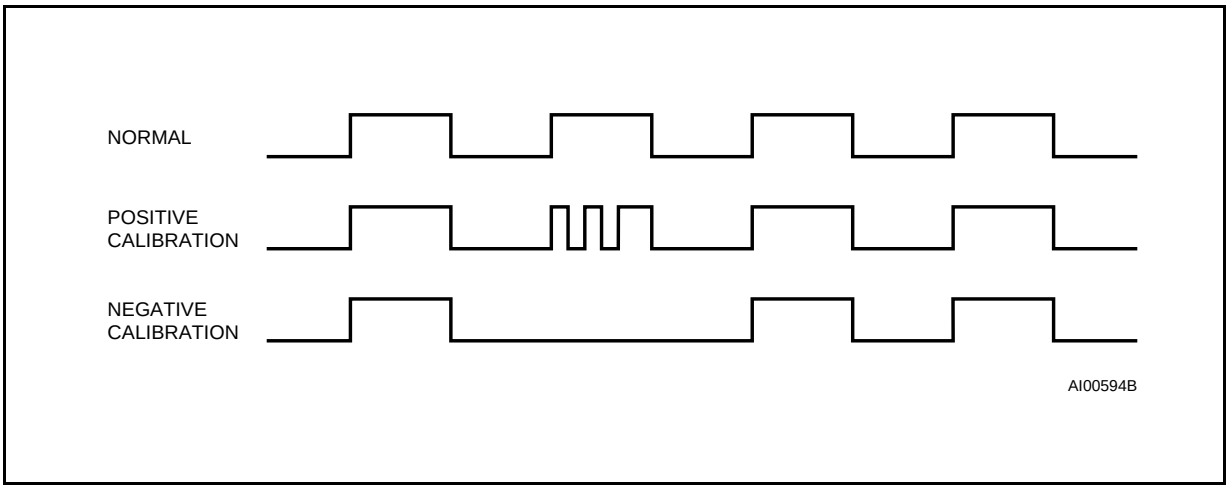


**Figure 13. Clock Calibration**




**CLOCK CALIBRATION** (cont'd)

Two methods are available for ascertaining how much calibration a given M41T56 may require. The first involves simply setting the clock, letting it run for a month and comparing it to a known accurate reference (like WWV broadcasts). While that may seem crude, it allows the designer to give the end user the ability to calibrate his clock as his environment may require, even after the final product is packaged in a non-user serviceable enclosure. All the designer has to do is provide a simple utility that accessed the Calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of some test equipment. When the Frequency Test (FT) bit, the seventh-most significant bit in the Control Register, is set to a '1', and the oscillator is running at 32,768 Hz, the FT/OUT pin of the device will toggle at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature.

For example, a reading of 512.01024 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10(XX001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

**OUTPUT DRIVER PIN**

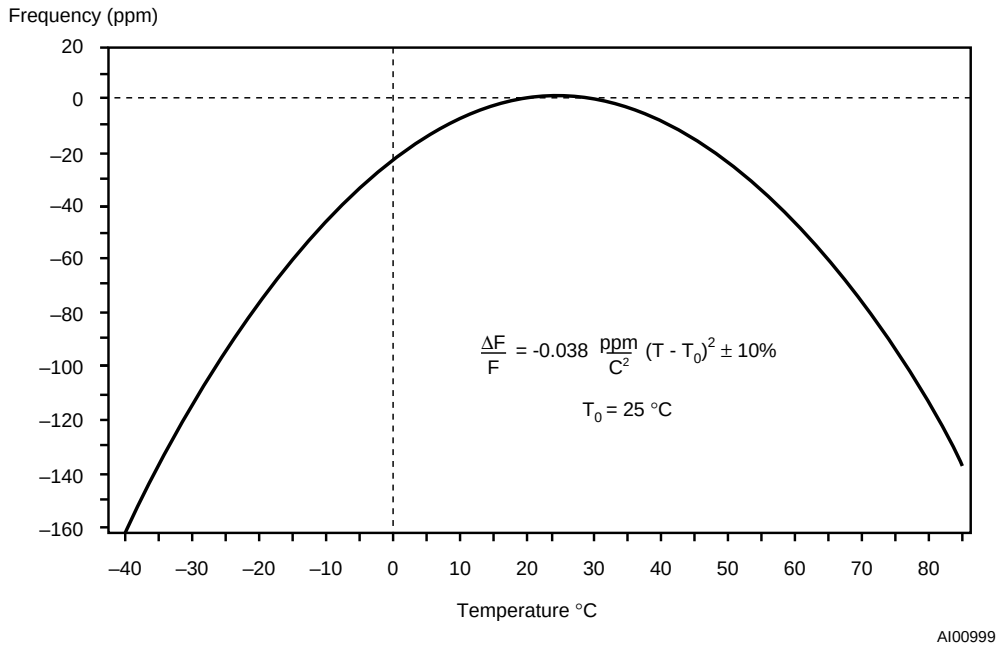
When the FT bit is not set, the FT/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words, when D6 of location 7 is a zero and D7 of location 7 is a zero and then the FT/OUT pin will be driven low.

**Note:** The FT/OUT pin is open drain which requires an external pull-up resistor.

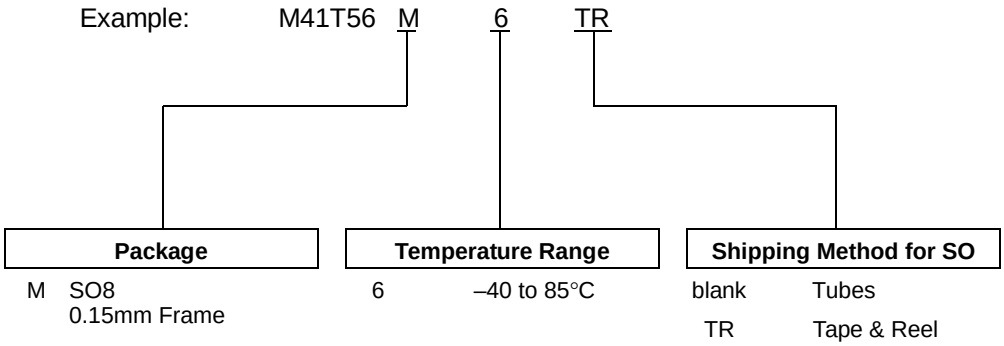
**POWER-ON DEFAULTS**

Upon initial application of power to the device, the FT bit will be set to a '0' and the OUT bit will be set to a '1'. All other Register bits will initially power-on in a random state.

**Figure 14. Crystal Accuracy Across Temperature**



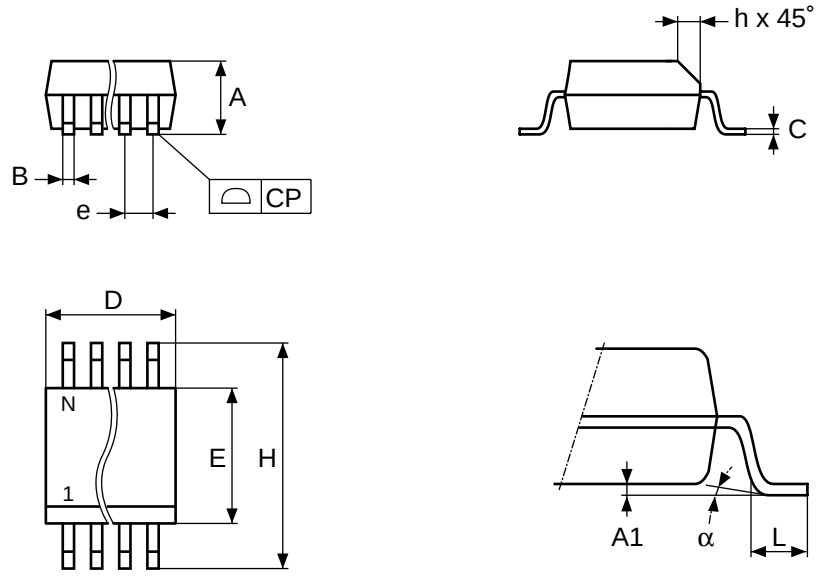
**ORDERING INFORMATION SCHEME**




For a list of available options or for further information or any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

## SO8 - 8 lead Plastic Small Outline, 150 mils body width

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 1.35 | 1.75 | | 0.053 | 0.069 |
| A1 | | 0.10 | 0.25 | | 0.004 | 0.010 |
| B | | 0.33 | 0.51 | | 0.013 | 0.020 |
| C | | 0.19 | 0.25 | | 0.007 | 0.010 |
| D | | 4.80 | 5.00 | | 0.189 | 0.197 |
| E | | 3.80 | 4.00 | | 0.150 | 0.157 |
| e | 1.27 | – | – | 0.050 | – | – |
| H | | 5.80 | 6.20 | | 0.228 | 0.244 |
| h | | 0.25 | 0.50 | | 0.010 | 0.020 |
| L | | 0.40 | 0.90 | | 0.016 | 0.035 |
| α | | 0° | 8° | | 0° | 8° |
| N | 8 | | | 8 | | |
| CP | | | 0.10 | | | 0.004 |




SO-a

Drawing is not to scale.