
HB56A172E Series

1,048,576-word $\times$ 72-bit High Density Dynamic RAM Module

HITACHI

Description

The HB56A172E belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications.

The HB56A172E is a 1 M $\times$ 72 ECC mode dynamic RAM module, mounted 18 pieces of 4 Mbit DRAM(HM514400CTT) sealed in TSOP package and 2 pieces of 16 bit BiCMOS line driver (74ABT16244) sealed in TSSOP package. An outline of the HB56A172E is 168-pin socket type package (dual lead out).

Therefore, the HB56A172E makes high density mounting possible without surface mount technology. The HB56A172E provides common data inputs and outputs. Decoupling capacitors are mounted beside the each TSOP on the module board.

Features

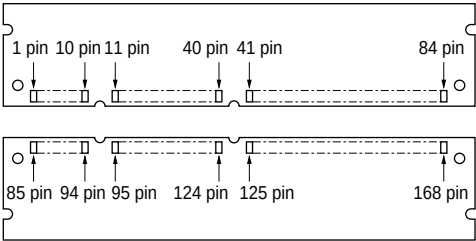
- 168-pin socket type package (Dual lead out)
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm$ 5%) supply
- High speed
 - Access time: $t_{\text{RAC}} = 60/70/80$ ns (max)
 $t_{\text{CAC}} = 20/25/25$ ns (max)
- Low power dissipation
 - Active mode: 10.73/9.79/8.84 W (max)
 - Standby mode: 525 mW (max)
- Buffered inputs except $\overline{\text{RAS}}$ and DQ
- 4 Byte interleave enabled, Dual Address inputs (A0/B0)
- Fast page mode capability
- 1,024 refresh cycle : 16 ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- TTL compatible

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Ordering Information

Type No.	Access time	Package	Contact pad
HB56A172E-6C	60 ns	168-pin dual lead out socket type	Gold
HB56A172E-7C	70 ns		
HB56A172E-8C	80 ns		

Pin Arrangement



Pin Assignment

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	27	$\overline{\text{WE0}}$	53	DQ19	79	PD1
2	DQ0	28	$\overline{\text{CE0}}$	54	V _{SS}	80	PD3
3	DQ1	29	NC	55	DQ20	81	PD5
4	DQ2	30	$\overline{\text{RE0}}$	56	DQ21	82	PD7
5	DQ3	31	$\overline{\text{OE0}}$	57	DQ22	83	ID0 (V _{SS})
6	V _{CC}	32	V _{SS}	58	DQ23	84	V _{CC}
7	DQ4	33	A0	59	V _{CC}	85	V _{SS}
8	DQ5	34	A2	60	DQ24	86	DQ36
9	DQ6	35	A4	61	NC	87	DQ37
10	DQ7	36	A6	62	NC	88	DQ38
11	DQ8	37	A8	63	NC	89	DQ39
12	V _{SS}	38	NC	64	NC	90	V _{CC}
13	DQ9	39	NC	65	DQ25	91	DQ40
14	DQ10	40	V _{CC}	66	DQ26	92	DQ41
15	DQ11	41	NC	67	DQ27	93	DQ42
16	DQ12	42	NC	68	V _{SS}	94	DQ43
17	DQ13	43	V _{SS}	69	DQ28	95	DQ44
18	V _{CC}	44	$\overline{\text{OE2}}$	70	DQ29	96	V _{SS}
19	DQ14	45	$\overline{\text{RE2}}$	71	DQ30	97	DQ45
20	DQ15	46	$\overline{\text{CE4}}$	72	DQ31	98	DQ46
21	DQ16	47	NC	73	V _{CC}	99	DQ47
22	DQ17	48	$\overline{\text{WE2}}$	74	DQ32	100	DQ48
23	V _{SS}	49	V _{CC}	75	DQ33	101	DQ49
24	NC	50	NC	76	DQ34	102	V _{CC}
25	NC	51	NC	77	DQ35	103	DQ50
26	V _{CC}	52	DQ18	78	V _{SS}	104	DQ51

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Pin Assignment (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
105	DQ52	122	NC	139	DQ56	156	DQ67
106	DQ53	123	NC	140	DQ57	157	V _{CC}
107	V _{SS}	124	V _{CC}	141	DQ58	158	DQ68
108	NC	125	NC	142	DQ59	159	DQ69
109	NC	126	B0	143	V _{CC}	160D	DQ70
110	V _{CC}	127	V _{SS}	144	DQ60	161	DQ71
111	NC	128	NC	145	NC	162	V _{SS}
112	NC	129	NC	146	NC	163	PD2
113	NC	130	NC	147	NC	164	PD4
114	NC	131	NC	148	NC	165	PD6
115	NC	132	$\overline{\text{PDE}}$	149	DQ61	166	PD8
116	V _{SS}	133	V _{CC}	150	DQ62	167	ID1 (V _{SS})
117	A1	134	NC	151	DQ63	168	V _{CC}
118	A3	135	NC	152	V _{SS}		
119	A5	136	DQ54	153	DQ64		
120	A7	137	DQ55	154	DQ65		
121	A9	138	V _{SS}	155	DQ66		

Pin Description

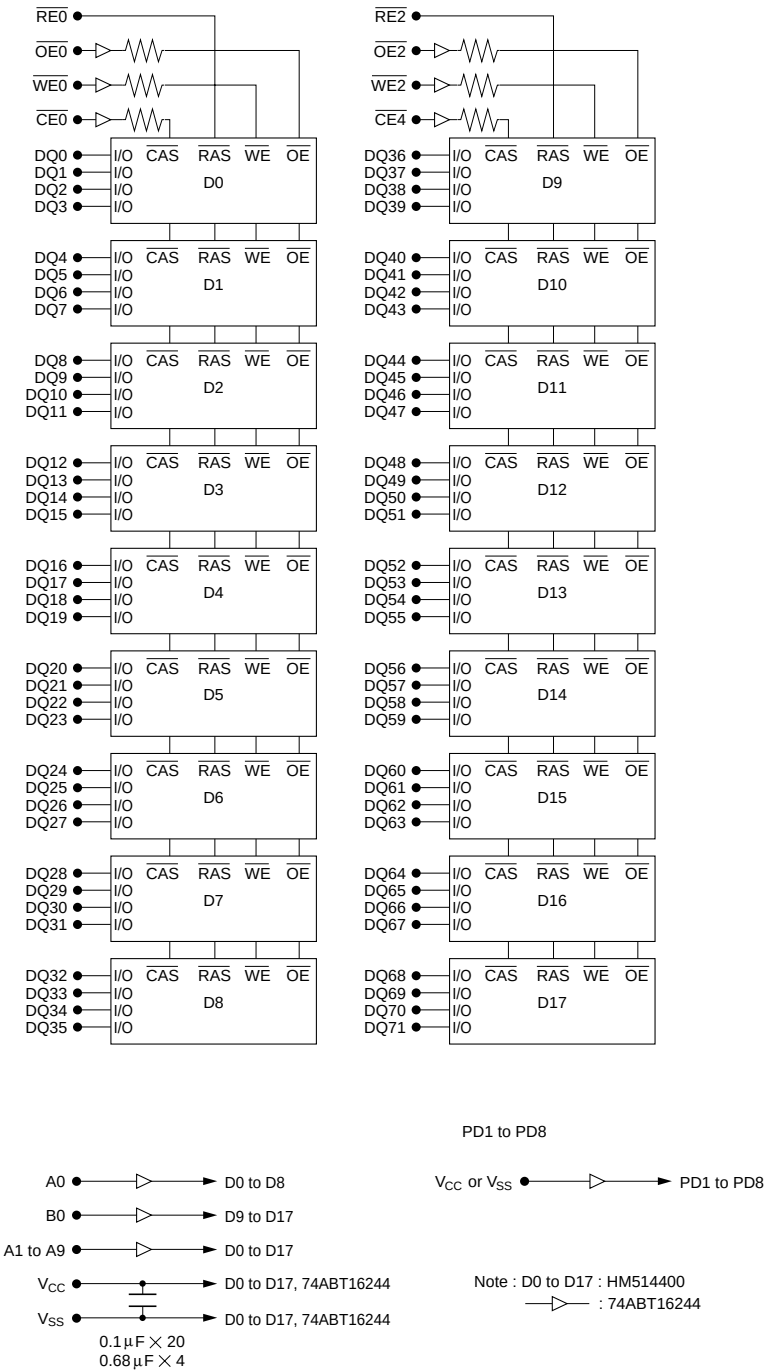
Pin name	Function
A0 - A9, B0	Address input: A0 - A9, B0 Row address: A0 - A9, B0 Column address: A0 - A9, B0 Refresh Address: A0 - A9, B0
DQ0 - DQ71	Data-in/Data-out
$\overline{\text{RE0}}, \overline{\text{RE2}}$	Row address strobe ($\overline{\text{RAS}}$)
$\overline{\text{CE0}}, \overline{\text{CE4}}$	Column address strobe ($\overline{\text{CAS}}$)
$\overline{\text{WE0}}, \overline{\text{WE2}}$	Read/write enable
$\overline{\text{OE0}}, \overline{\text{OE2}}$	Output enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 - PD8	Presence detect
ID0, ID1	ID bit
PDE	Presence detect enable
NC	No connection

Presence Detect Pin Assignment

Pin name	Pin No.	$\overline{\text{PDE}} = \text{Low}$			$\overline{\text{PDE}} = \text{High}$
		60 ns	70 ns	80 ns	All
PD1	79	0	0	0	High-Z
PD2	163	0	0	0	High-Z
PD3	80	1	1	1	High-Z
PD4	164	0	0	0	High-Z
PD5	81	0	0	0	High-Z
PD6	165	1	0	1	High-Z
PD7	82	1	1	0	High-Z
PD8	166	0	0	0	High-Z

Note: 1: High level (Driver output)
0: Low level (Driver output)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS} .	V_T	−0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	19	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltatge	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−0.5	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

HB56A172E										
Parameter	Symbol	60 ns		70 ns		80 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	2044	—	1864	—	1684	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	100	—	100	—	100	mA	TTL interface R _{AS} , C _{AS} = V _{IH} , Dout = High-Z	
		—	82	—	82	—	82	mA	CMOS interface R _{AS} , C _{AS} ≥ V _{CC} -0.2 V Dout = High-Z	
R _{AS} -only refresh current	I _{CC3}	—	2044	—	1864	—	1684	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	154	—	154	—	154	mA	R _{AS} = V _{IH} , C _{AS} = V _{IL} , Dout = enable	1
C _{AS} -before-R _{AS} refresh current	I _{CC6}	—	2044	—	1864	—	1684	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	2044	—	1864	—	1684	mA	t _{PC} = min	1, 3
Input leakage current	I _{LI}	-1.0	1.0	-1.0	1.0	-1.0	1.0	μA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I _{LO}	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V _{CC}	2.4	V	High Iout = -5.0 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while R_{AS} = V_{IL}.
3. Address can be changed once or less while C_{AS} = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	20	pF	1
Input capacitance (Clock)	C _{I2}	—	20	pF	1
Input capacitance (R _{AS})	C _{I3}	—	78	pF	1
I/O capacitance (DQ)	C _{I/O}	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. C_{AS} = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, VCC = 5 V ± 5%, VSS = 0 V)*1, *14, *15

Read, Write, Read-Modity-Write and Refresh Cycles (Common parameters)

		HB56A172E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	110	—	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	15	10000	20	10000	20	10000	ns	
Row address setup time	t _{ASR}	5	—	5	—	5	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	40	20	45	20	55	ns	8
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	15	35	ns	9
$\overline{\text{RAS}}$ hold time	t _{RSH}	20	—	25	—	25	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	15	—	15	—	15	—	ns	
$\overline{\text{OE}}$ to Din delay time	t _{ODD}	20	—	25	—	25	—	ns	
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ delay time from Din	t _{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	7
Refresh period	t _{REF}	—	16	—	16	—	16	ms	

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Read Cycle

		HB56A172E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	20	—	25	—	25	ns	3, 4, 13
Access time from address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access time from $\overline{\text{OE}}$	t_{OAC}	—	20	—	25	—	25	ns	3
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	16
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	16
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Output buffer turn-off time	t_{OFF1}	0	20	0	25	0	25	ns	6
Output buffer turn-off to $\overline{\text{OE}}$	t_{OFF2}	0	20	0	25	0	25	ns	6
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	20	—	25	—	25	—	ns	
$\overline{\text{OE}}$ pulse width	t_{OEP}	15	—	20	—	20	—	ns	

Write Cycle

Parameter		Symbol		HB56A172E						Unit	Notes
				60 ns		70 ns		80 ns			
				Min	Max	Min	Max	Min	Max		
Write command setup time	t _{WCS}	0	—	0	—	0	—	ns	10		
Write command hold time	t _{WCH}	15	—	15	—	15	—	ns			
Write command pulse width	t _{WP}	10	—	10	—	10	—	ns			
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	20	—	25	—	25	—	ns			
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	15	—	20	—	20	—	ns			
Data-in setup time	t _{DS}	0	—	0	—	0	—	ns	11		
Data-in hold time	t _{DH}	20	—	20	—	20	—	ns	11		

Read-Modify-Write Cycle

		HB56A172E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	150	—	180	—	200	—	ns	
RAS to $\overline{WE}$ delay time	t _{RWD}	85	—	100	—	110	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t _{CWD}	35	—	45	—	45	—	ns	10
Column address to $\overline{WE}$ delay time	t _{AWD}	50	—	60	—	65	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t _{OEh}	15	—	20	—	20	—	ns	

Refresh Cycle

		HB56A172E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t _{CSR}	15	—	15	—	15	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t _{CHR}	10	—	10	—	10	—	ns	
$\overline{WE}$ setup time	t _{WS}	5	—	5	—	5	—	ns	
$\overline{WE}$ hold time	t _{WH}	10	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t _{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t _{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

		HB56A172E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t _{PC}	40	—	45	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	10	—	10	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t _{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HB56A172E							
		60 ns		70 ns		80 ns			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	t_{PCM}	80	—	95	—	100	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	55	—	65	—	70	—	ns	10

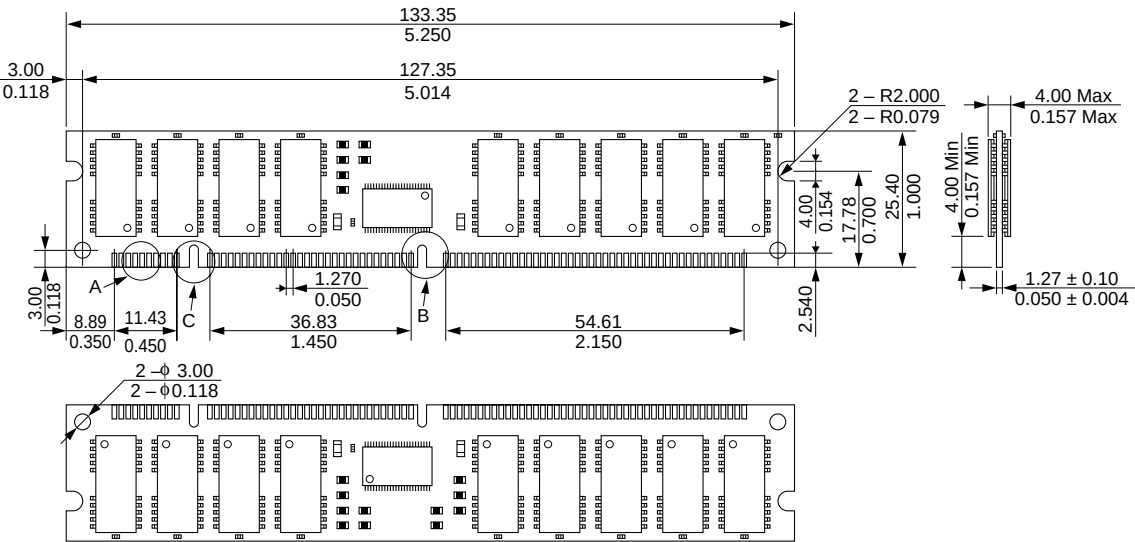
- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} < t_{RCD}(\text{max})$ and $t_{RAD} < t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ and $t_{OEZ}(\text{max})$ is define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{CPW} \geq t_{CPW}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referred to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
 12. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
 13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA} .
 14. An initial pause of 100 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ -only refresh or $\overline{CAS}$ -before- $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles are required.
 15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
 16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.

Timing Waveforms

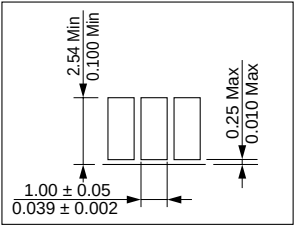
Refer to the HB56G236B/SB Series.

Physical Outline

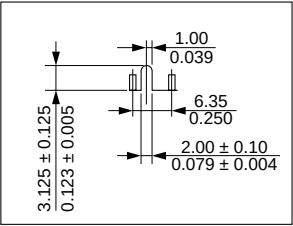
Unit: mm/inch



Detail A



Detail B



Detail C

