HM51W4400B Series

1,048,576-word × 4-bit Dynamic Random Access Memory

HITACHI

Description

The Hitachi HM51W4400B is a CMOS dynamic RAM organized 1,048,576-word × 4-bit. HM51W4400B has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM51W4400B offers Fast Page Mode as a high speed access mode. Multiplexed address input permits the HM51W4400B to be packaged in standard 300-mil 26-pin plastic SOJ and standard 300-mil 26-pin plastic TSOP II.

Features

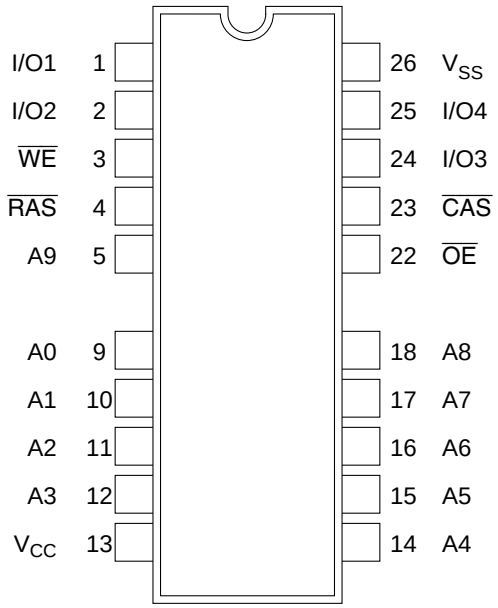
- Single 3.3 V (± 0.3 V)
- High speed
  - — Access time: 70 ns/80 ns (max)
- Low power dissipation
  - — Active mode: 252 mW/216 mW (max)
  - — Standby mode: 7.2 mW (max)
    0.18 mW (max) (L-version)
- Fast page mode capability
- 1024 refresh cycles : 16 ms
  : 128 ms (L-version)
- 4 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
  - — Self refresh (L-version)
- Test function
- Battery backup operation (L-version)

Ordering Information

Type No.	Access time	Package
HM51W4400BS-7	70 ns	300-mil 26-pin plastic SOJ (CP-26/20D)
HM51W4400BS-8	80 ns	
HM51W4400BLS-7	70 ns	
HM51W4400BLS-8	80 ns	
HM51W4400BTT-7	70 ns	300-mil 26-pin plastic TSOP (TTP-26/20D)
HM51W4400BTT-8	80 ns	
HM51W4400BLTT-7	70 ns	
HM51W4400BLTT-8	80 ns	

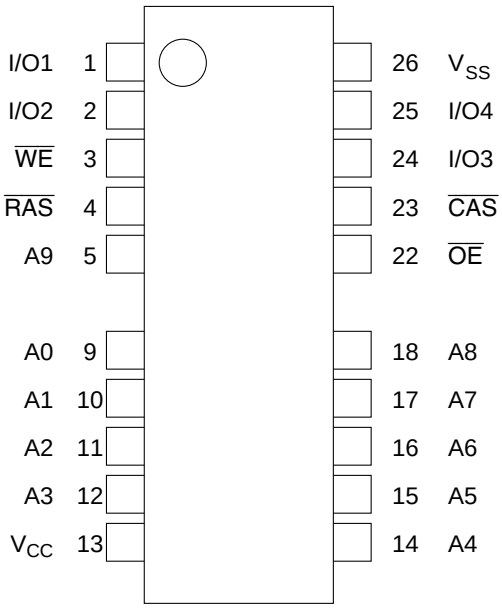
Pin Arrangement

HM51W4400BS/BLS Series



(Top view)

HM51W4400BTT/BLTT Series

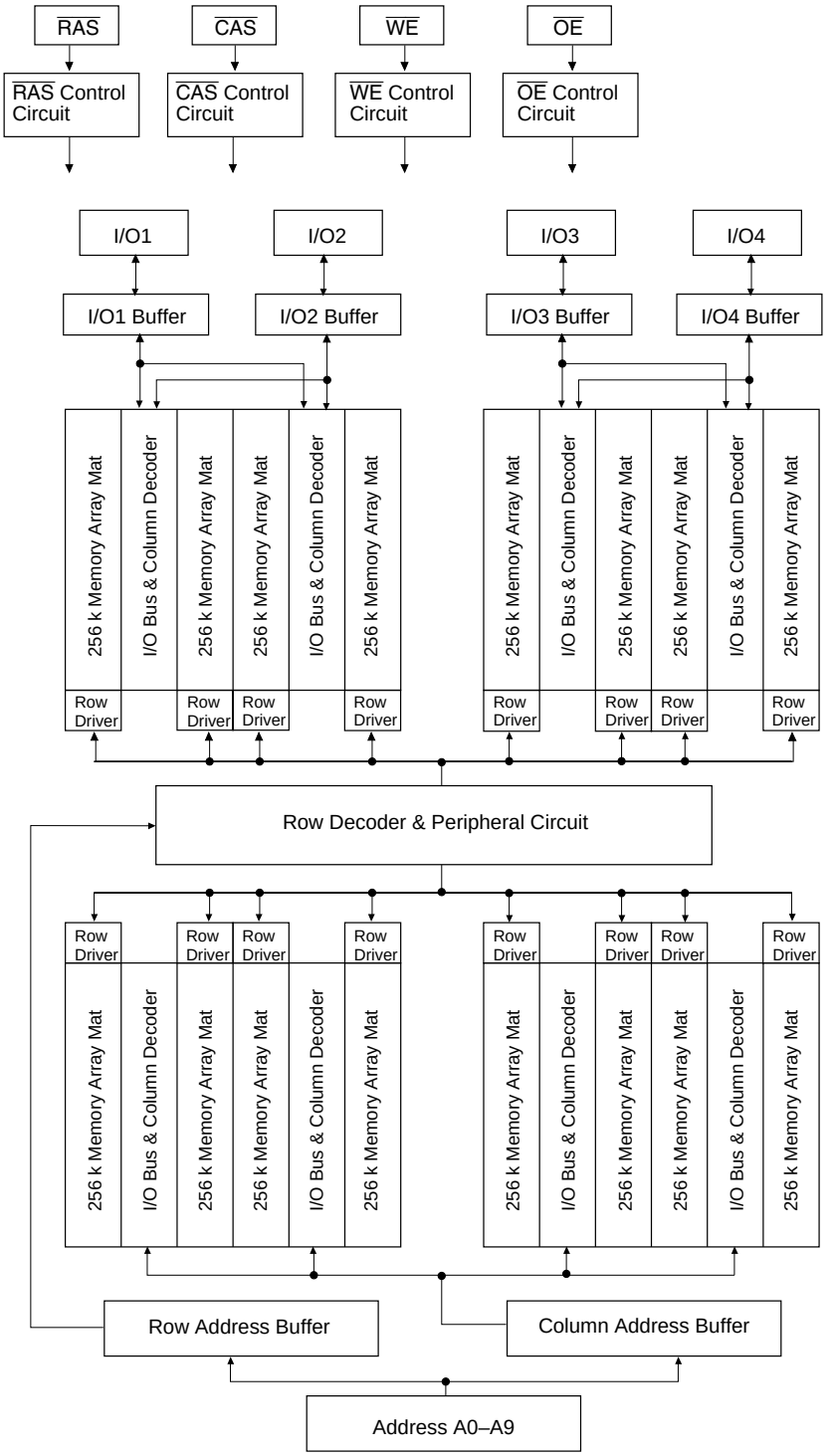


(Top view)

Pin Description

Pin name	Function
A0 to A9	Address inputs
A0 to A9	Refresh address inputs
I/O1 to I/O4	Data-in/Data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
V_{CC}	Power (+3.3 V typ)
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	–0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HM51W4400B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Operating current*1, 2	I_{CC1}	—	70	—	60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z
		—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current*4 (L-version)	I_{CC2}	—	50	—	50	µA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} $\overline{WE}$, $\overline{OE}$, Address and Din = V_{IH} or V_{IL} Dout = High-Z

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (cont)

		HM51W4400B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
$\overline{RAS}$-only refresh current[*2]	I_{CC3}	—	70	—	60	mA	t_{RC} = min
Standby current[*1]	I_{CC5}	—	4	—	4	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	70	—	60	mA	t_{RC} = min
Fast page mode current[*1, 3]	I_{CC7}	—	60	—	50	mA	t_{PC} = min
Battery backup current[*4] (standby with CBR refresh) (L-version)	I_{CC10}	—	100	—	100	µA	t_{RC} = 125 µs $t_{RAS} \leq$ 1 µs, $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, $\overline{OE}$, Address, Din = V_{IH} or V_{IL}, Dout = High-Z
Self-refresh current[*4] (L-version)	I_{CC11}	—	100	—	100	µA	$\overline{RAS}$, $\overline{CAS}$ = V_{IL}, $\overline{OE}$, Address, $\overline{WE}$ and Din = V_{IH} or V_{IL}, Dout = High-Z
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed twice or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. $V_{IH} \geq V_{CC}$ – 0.2 V, 0V ≤ $V_{IL} \leq$ 0.2 V.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{RAS}$ and $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)[*1, *14, *15, *16]

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing referen,ce levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM51W4400B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	ns	19
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	ns	20
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	ns	9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	20	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	tT	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	ms	

Read Cycle

		HM51W4400B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	ns	2, 3, 17
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	ns	3, 4, 13, 17
Access time from address	t_{AA}	—	35	—	40	ns	3, 5, 13, 17
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	ns	3, 17
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	18
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	18
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF1}	—	20	—	20	ns	6
Output buffer turn-off time to $\overline{OE}$	t_{OFF2}	—	20	—	20	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	20	—	ns	
$\overline{OE}$ pulse width	t_{OEP}	20	—	20	—	ns	

Write Cycle

		HM51W4400B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	ns	11

Read-Modify-Write Cycle

		HM51W4400B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	180	—	200	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	95	—	105	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	65	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	20	—	20	—	ns	

Refresh Cycle

		HM51W4400B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	ns	

Fast Page Mode Cycle

		HM51W4400B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode cycle time	t_{PC}	45	—	50	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	ns	3, 13, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	45	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HM51W4400B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	t_{PCM}	95	—	100	—	ns	
Fast page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	65	—	70	—	ns	10

Test Mode Cycle

		HM51W4400B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	10	—	10	—	ns	

Counter Test Cycle

		HM51W4400B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	40	—	ns	

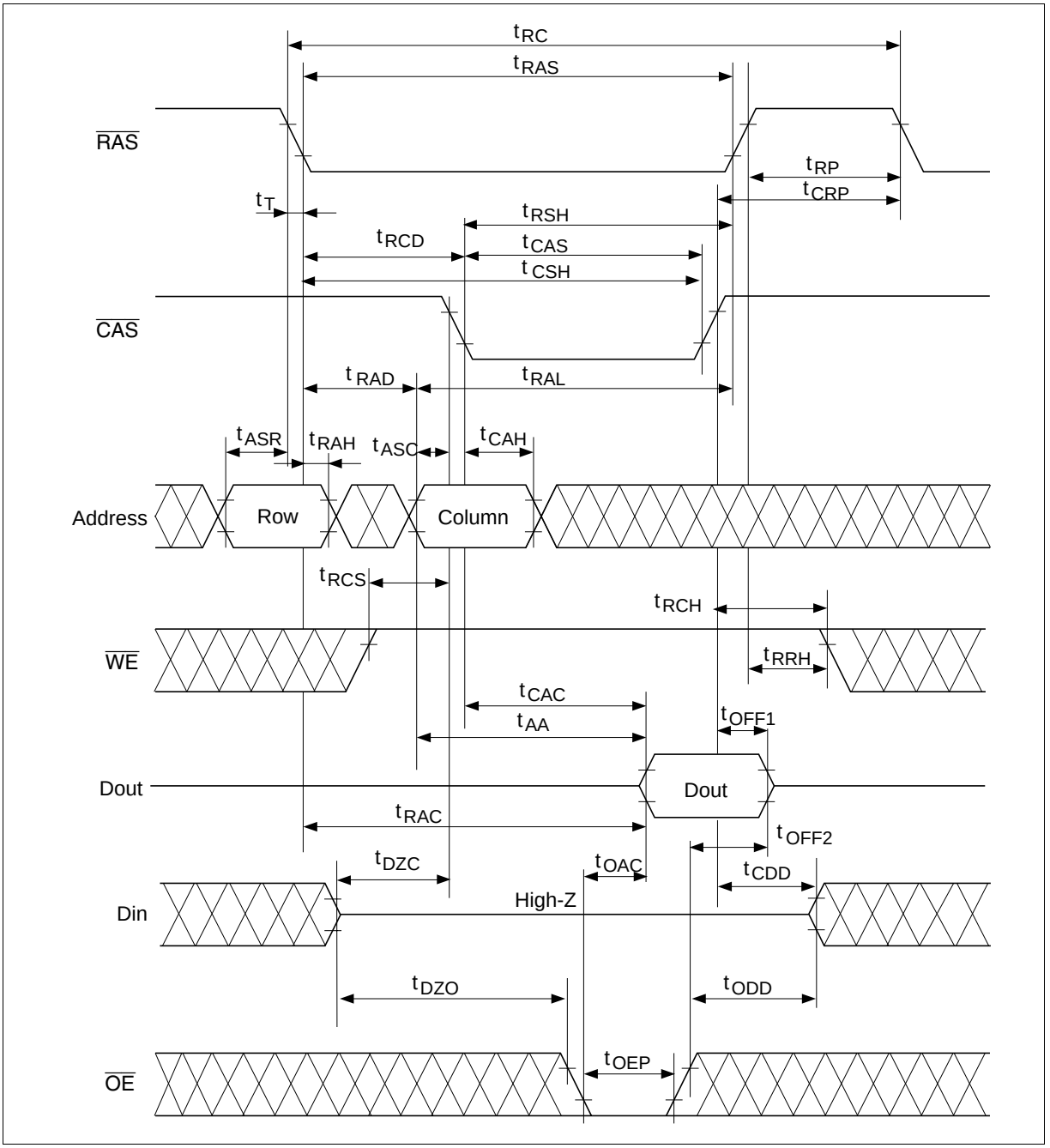
Self Refresh Mode (L-version)

		HM51W4400BL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	µs	
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	130	—	150	—	ns	
$\overline{CAS}$ hold time (self refresh)	t_{CHS}	–50	—	–50	—	ns	

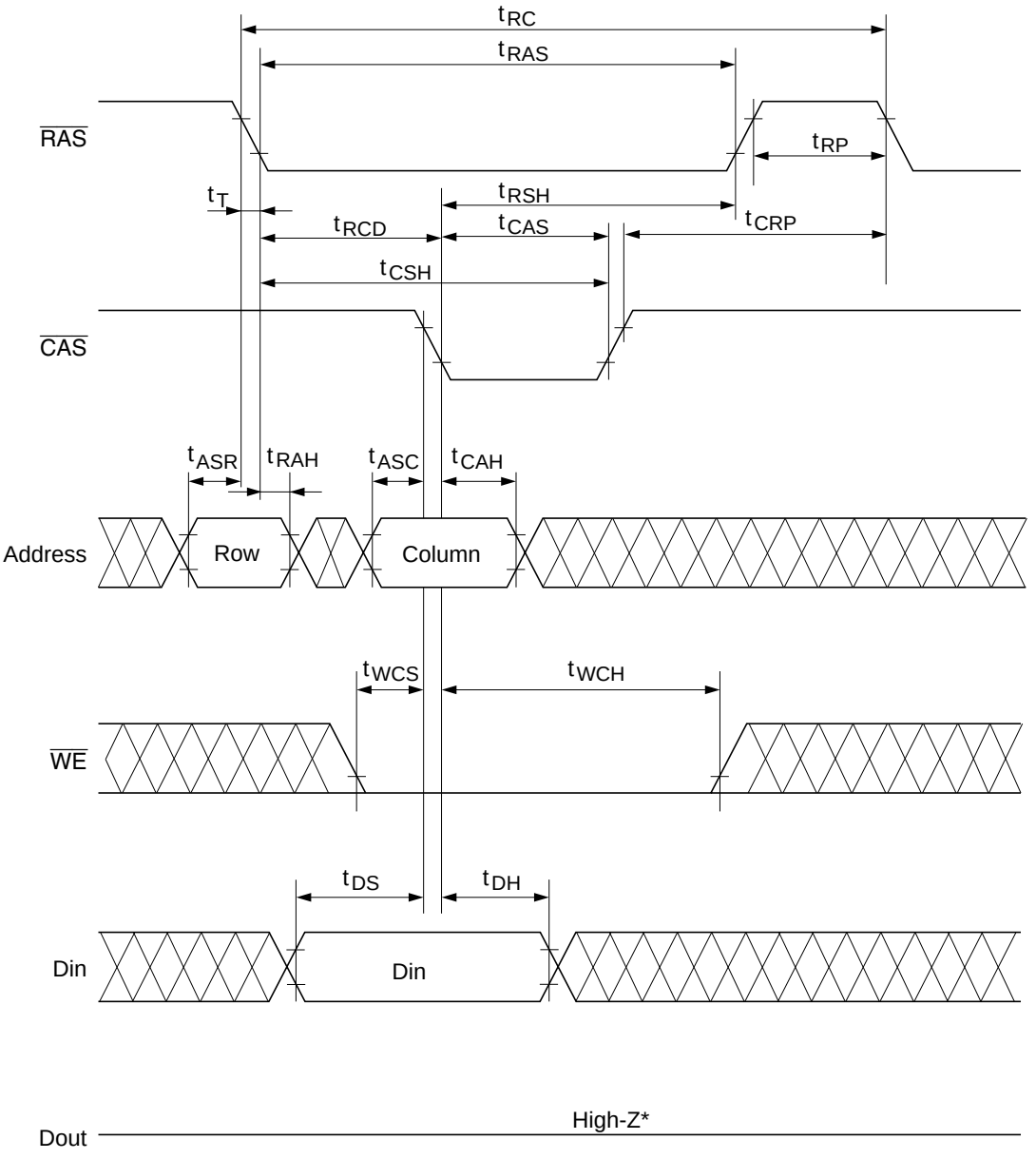
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{CPW} \geq t_{CPW}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 2-bit test function controlled by control address bits - - - CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. Either t_{RCH} or t_{RRH} must be satisfied
19. t_{RAS} (min) = t_{RWD} (min) + t_{RWL} (min) + t_T in read-modify-write cycle.
20. t_{CAS} (min) = t_{CWD} (min) + t_{CWL} (min) + t_T in read-modify-write cycle.
21. XXXX H or L (H: V_{IH} (min) ≤ Vin ≤ V_{IH} (max), L: V_{IL} (min) ≤ Vin ≤ V_{IL} (max)
    //////// Invalid Dout

Timing Waveforms[*21]

Read Cycle



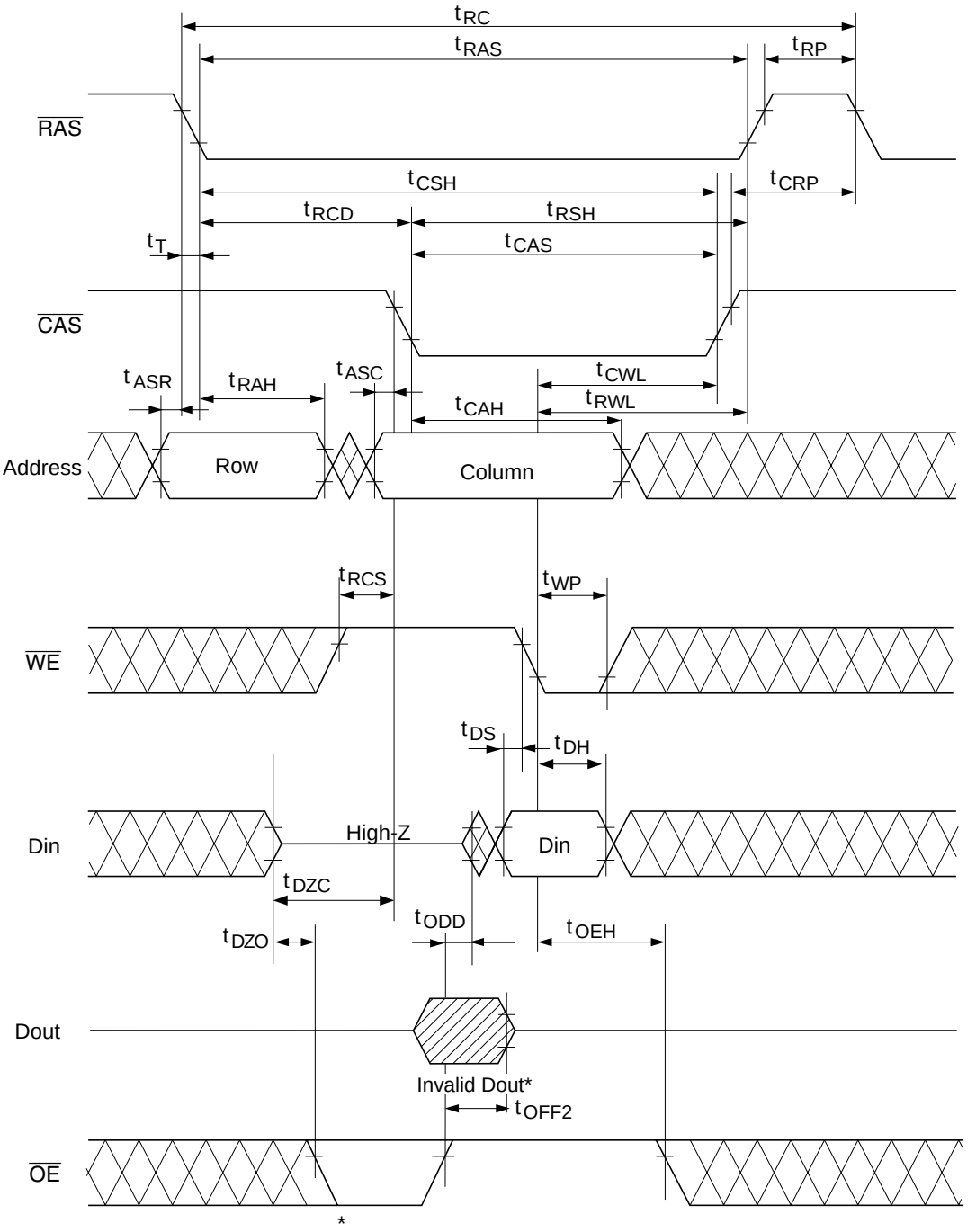
Early Write Cycle



* $t_{WCS} \geqq t_{WCS}$(min)

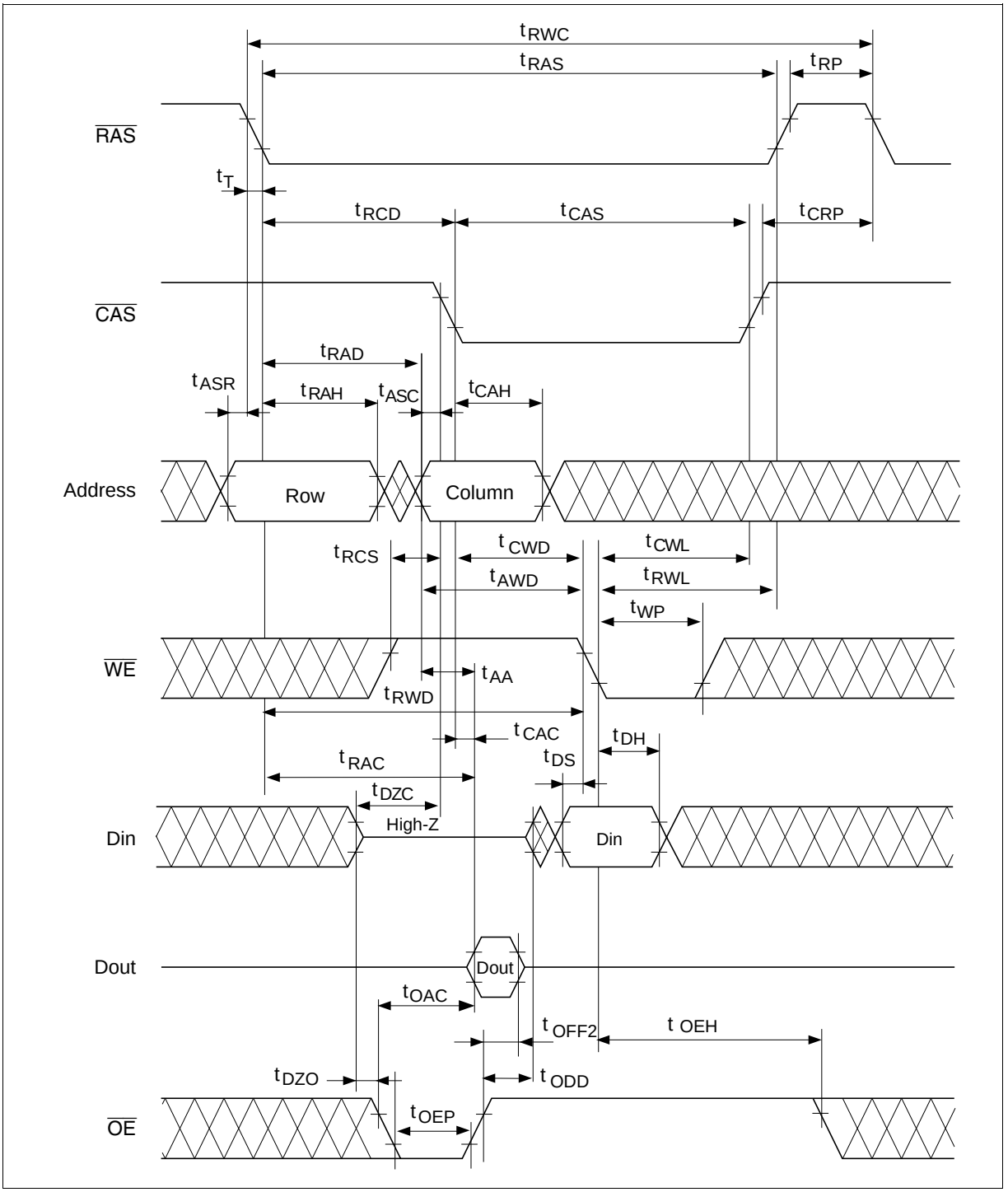
** $\overline{OE}$: H or L

Delayed Write Cycle

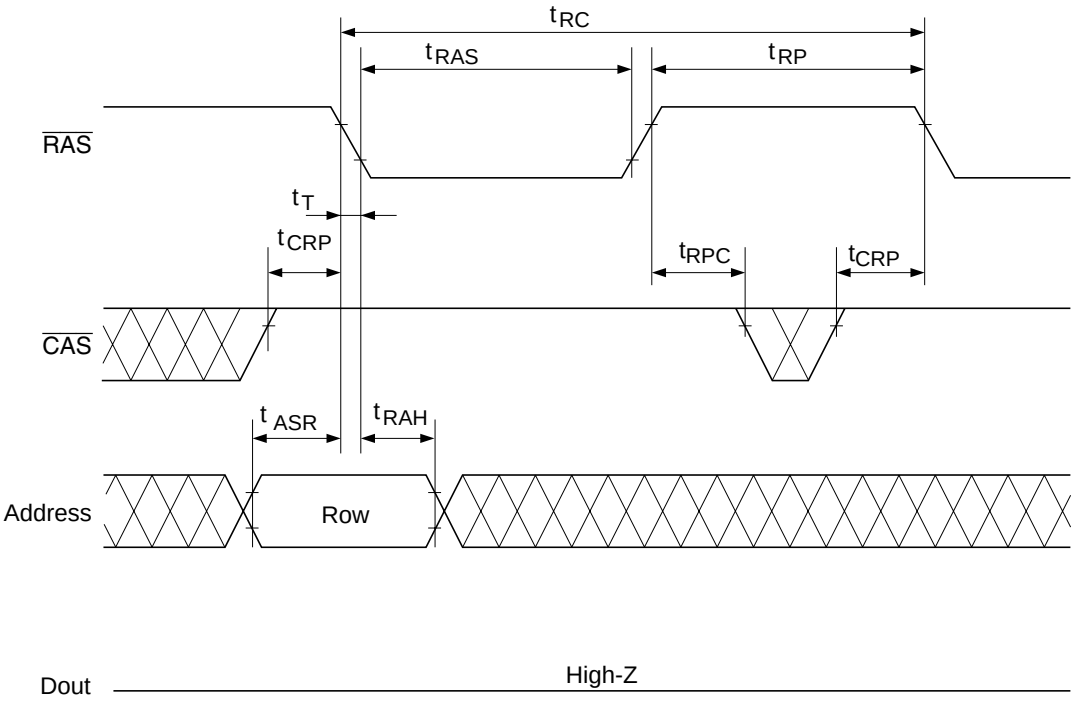


* Invalid Dout comes out, when $\overline{OE}$ is low level.

Read-Modify-Write Cycle



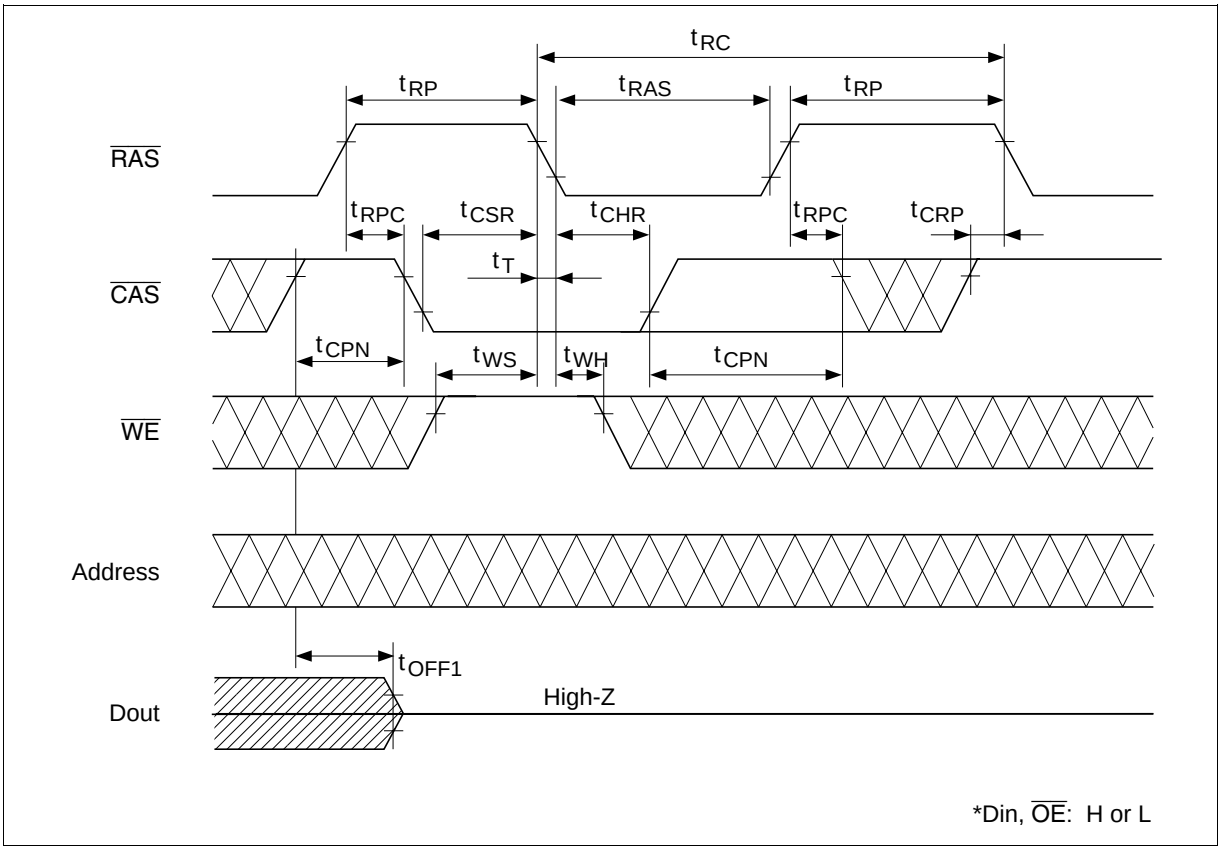
$\overline{\text{RAS}}$-Only Refresh Cycle



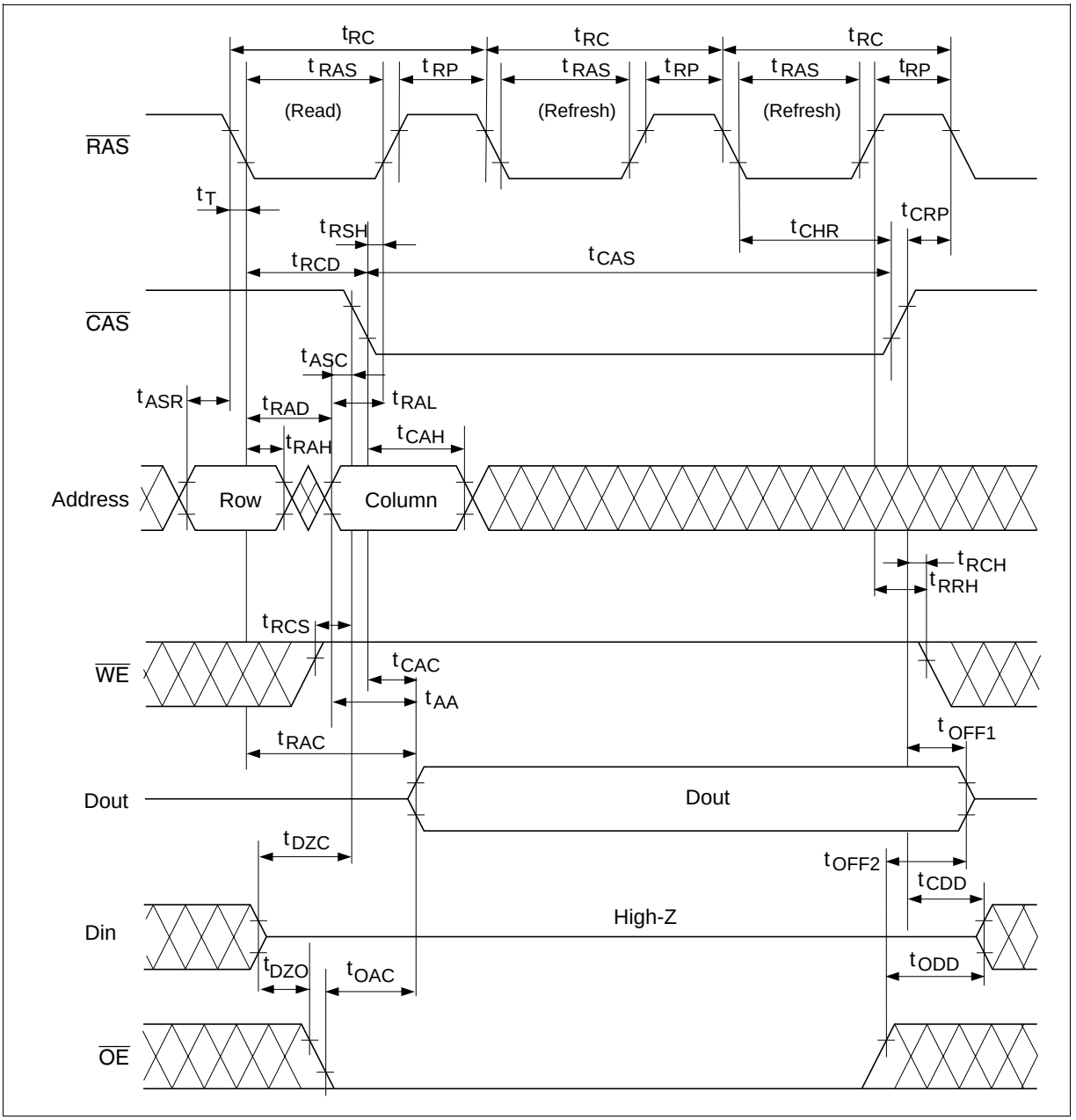
* Refresh address : A0 – A9 (AX0 – AX9)

** $\overline{\text{WE}}$, Din, $\overline{\text{OE}}$: H or L

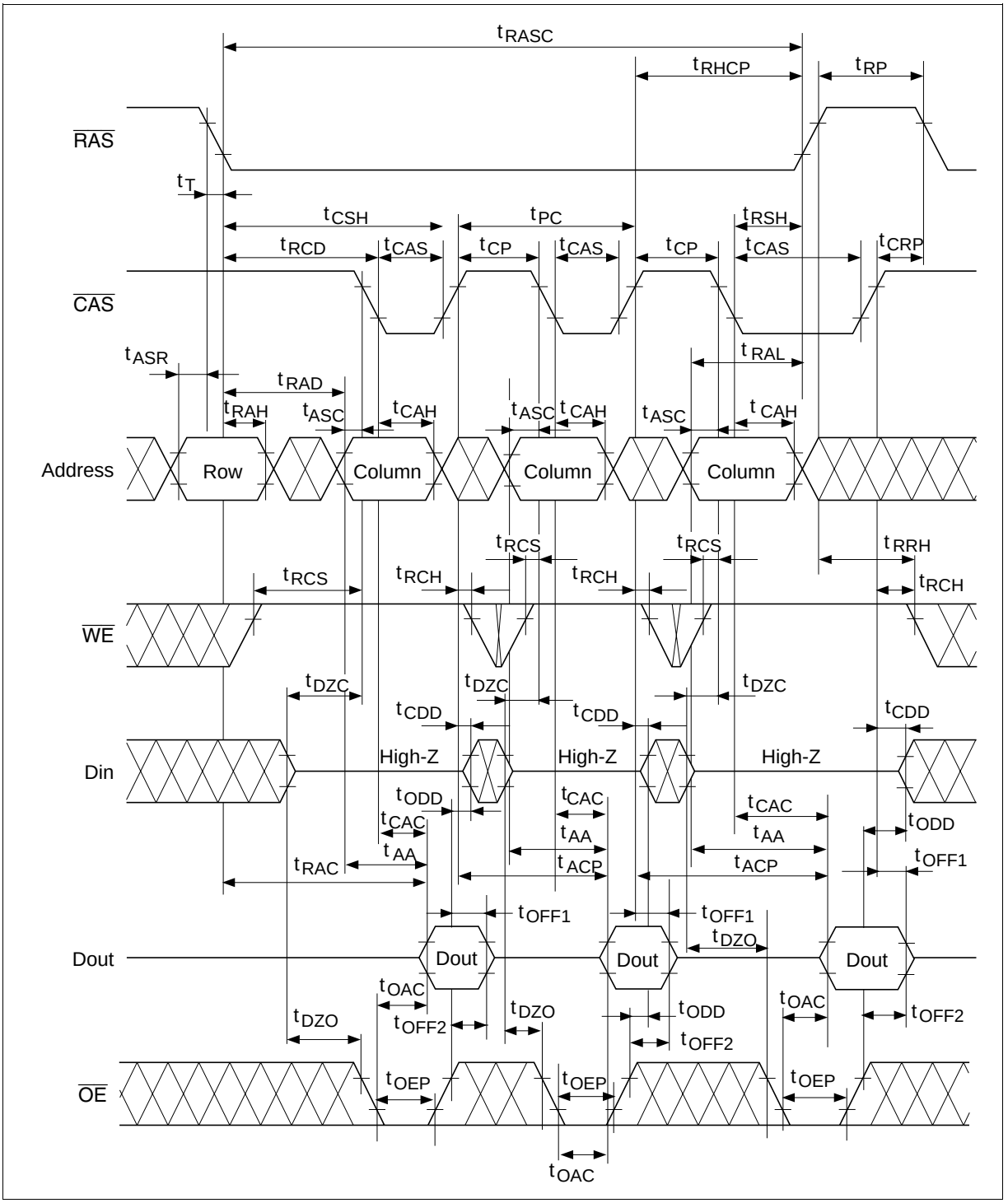
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



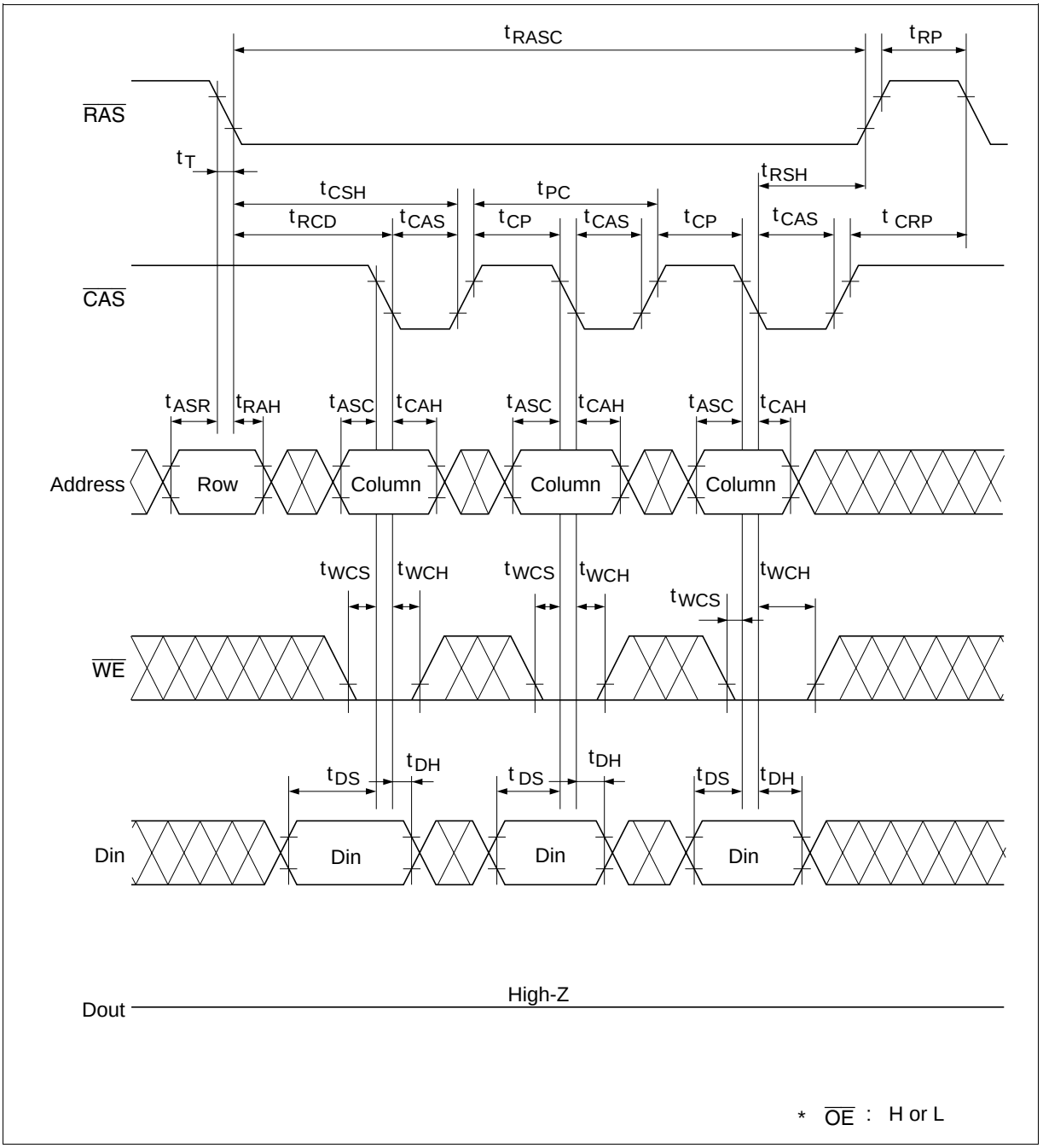
Hidden Refresh Cycle



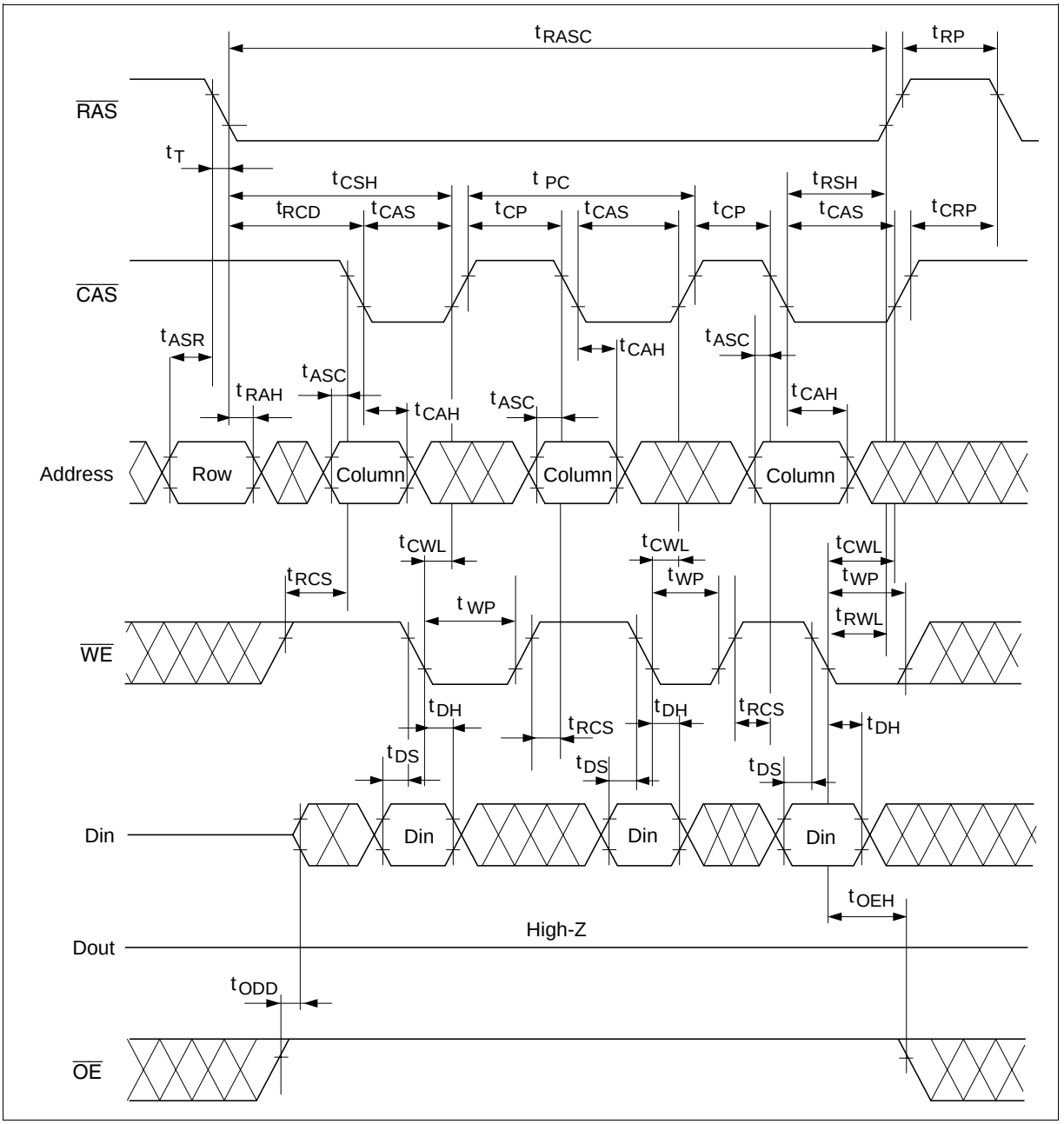
Fast Page Mode Read Cycle



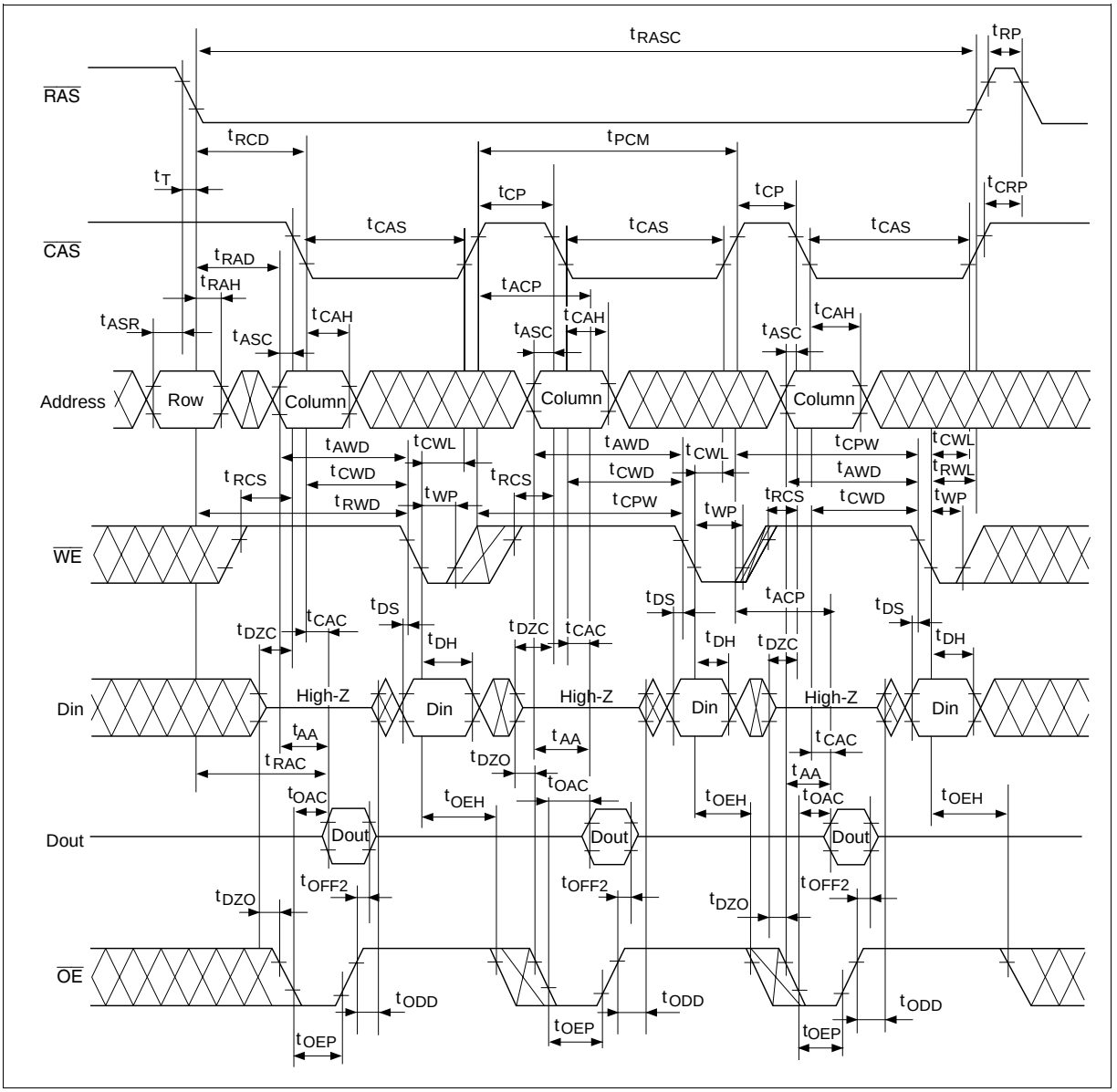
Fast Page Mode Early Write Cycle



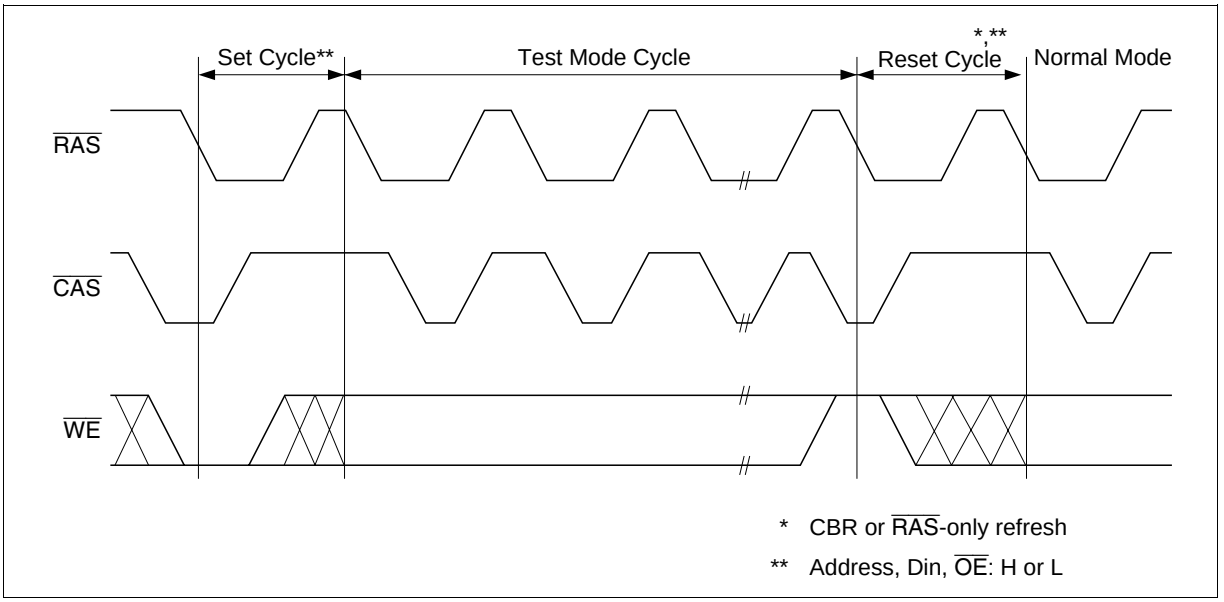
Fast Page Mode Delayed Write Cycle



Fast Page Mode Read-Modify-Write Cycle

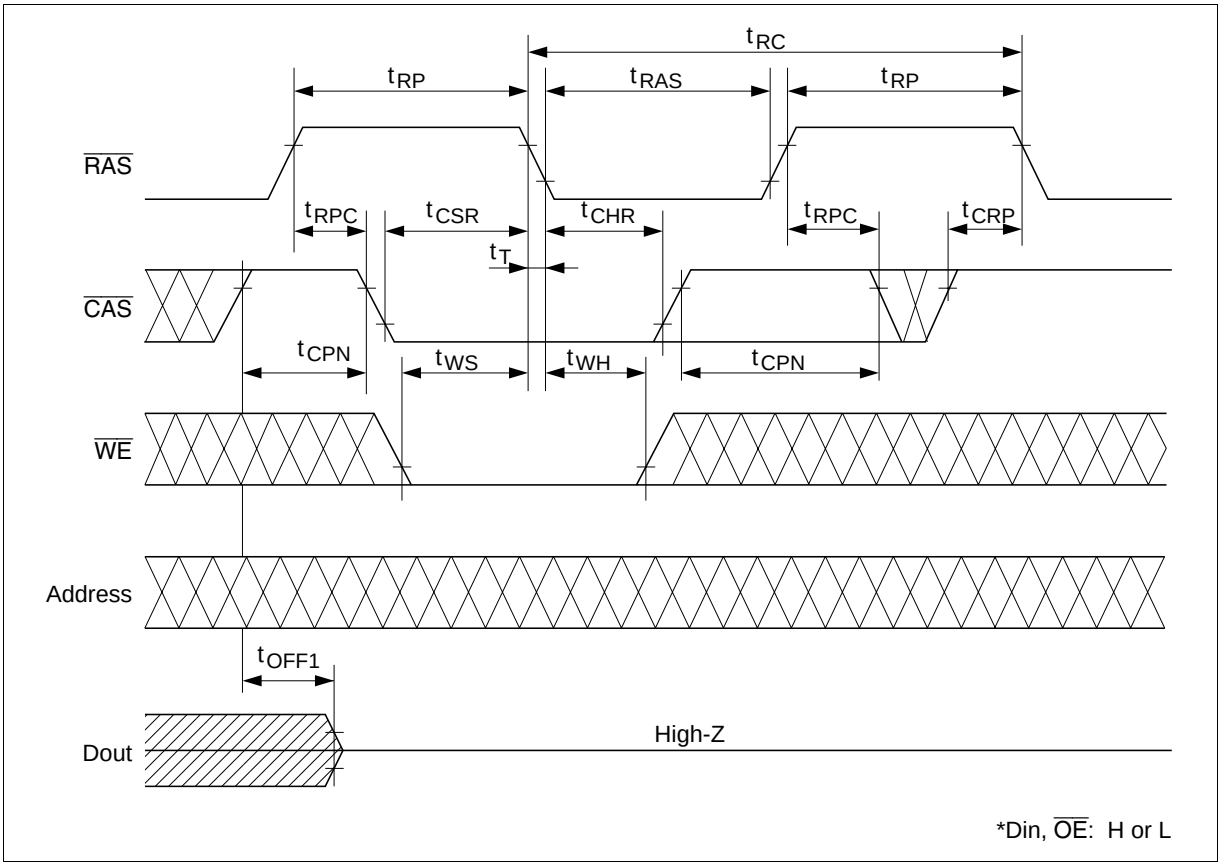


Test Mode Cycle

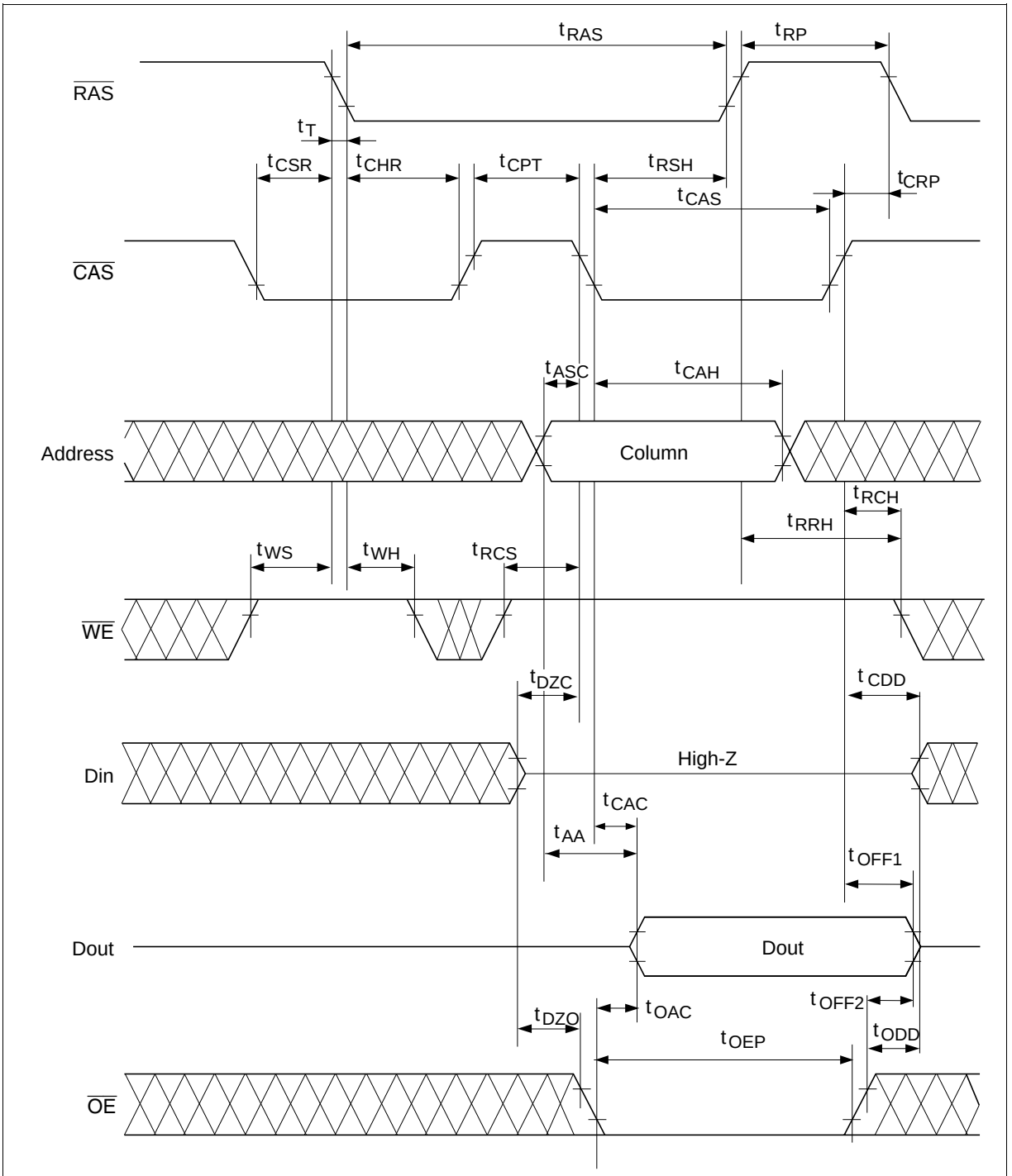


Test Mode Set Cycle

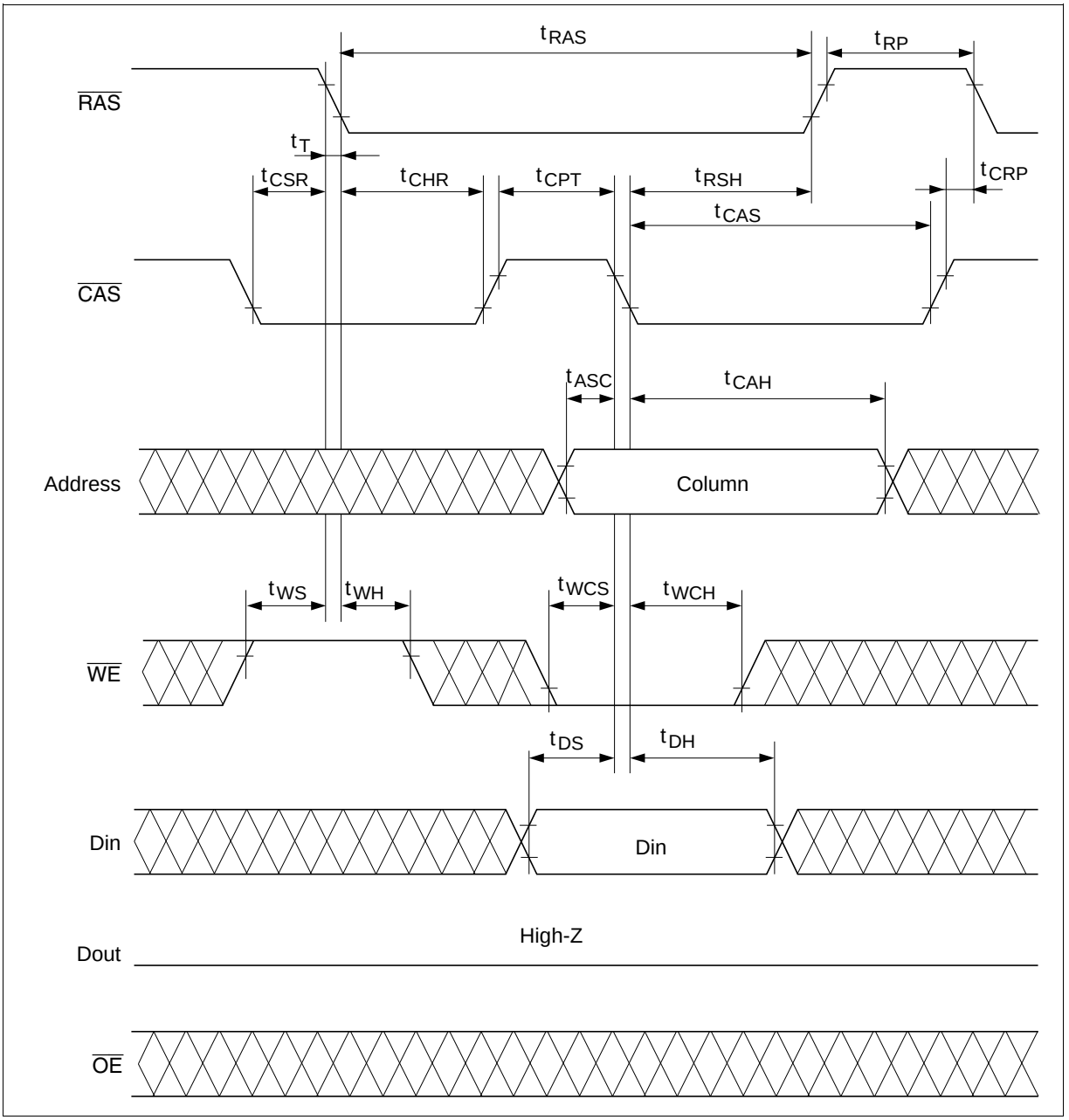
$\overline{WE}$-and-$\overline{CAS}$-Before $\overline{RAS}$-Refresh Cycle



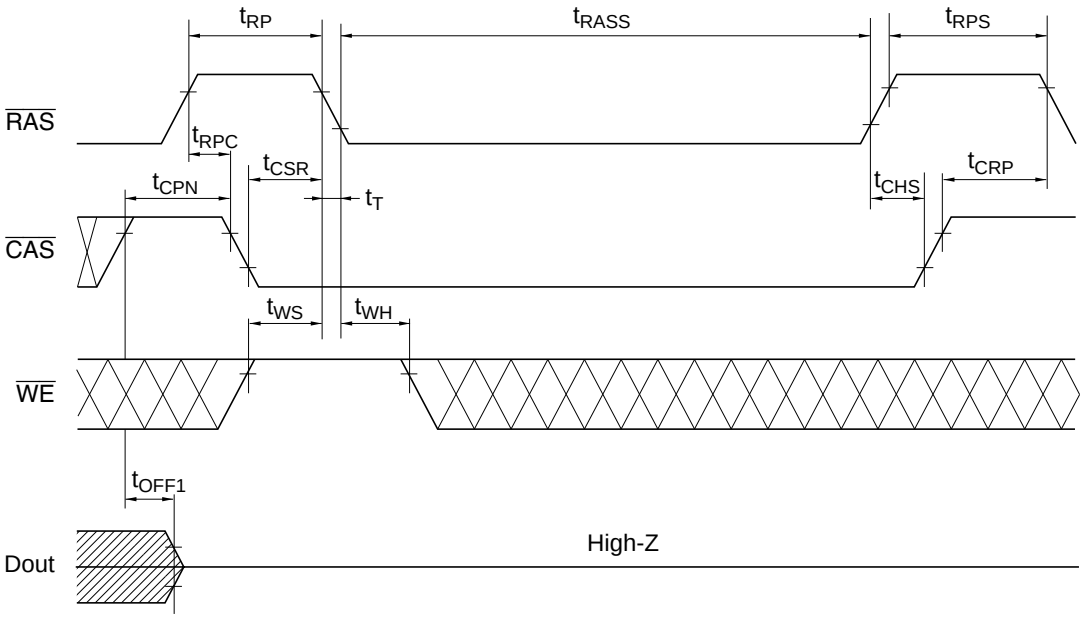
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Check Cycle (Read)



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Check Cycle (Write)



Self Refresh Cycle (L-version)



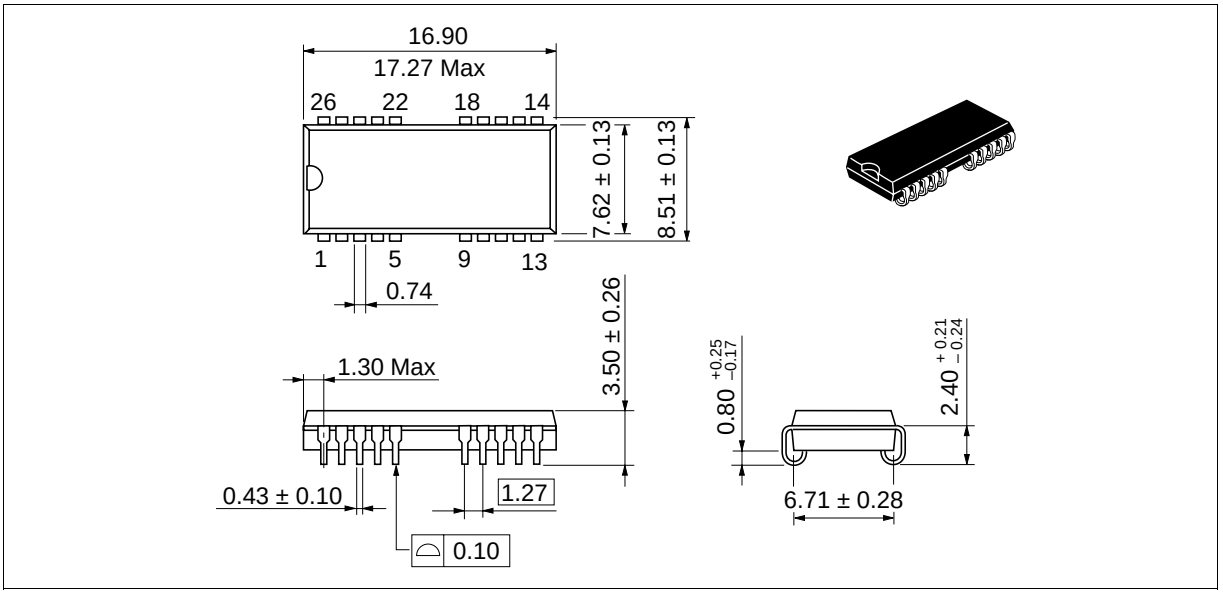
∗ Address, Din, $\overline{OE}$: H or L

The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

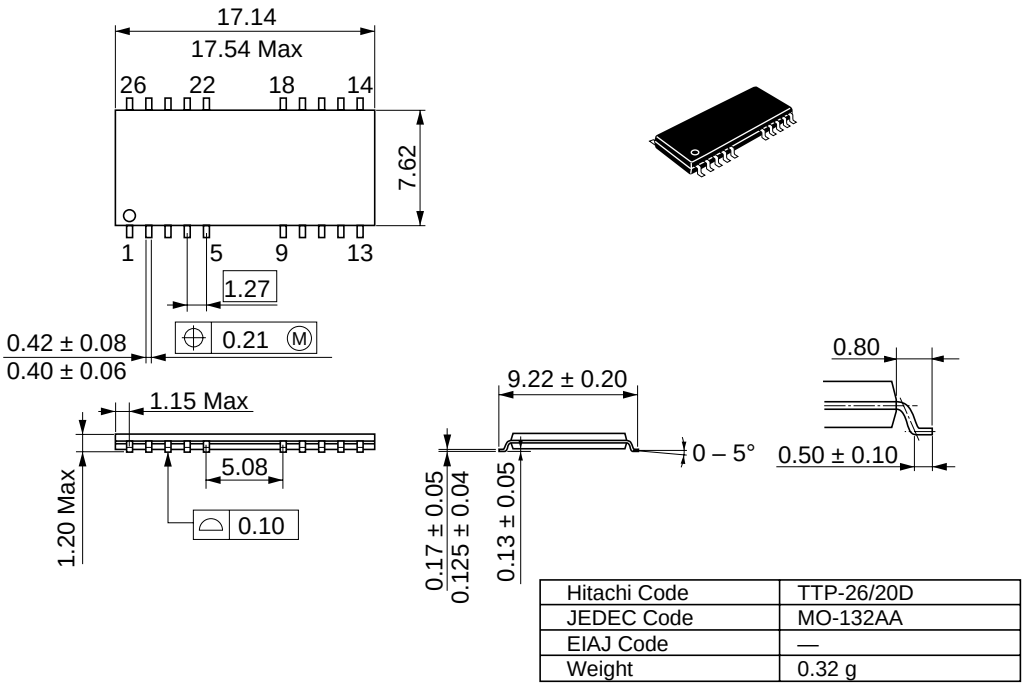
1. Please do not use t_{RASS} timing, 10 µs ≤ t_{RASS} ≤ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If t_{RASS} ≥ 100 µs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

Package Dimensions

HM51W4400BS/BLS Series (CP-26/20D) Unit: mm



HM51W4400BTT/BLTT Series (TTP-26/20D) Unit: mm



Hitachi Code	TTP-26/20D
JEDEC Code	MO-132AA
EIAJ Code	—
Weight	0.32 g