



74LVQ574

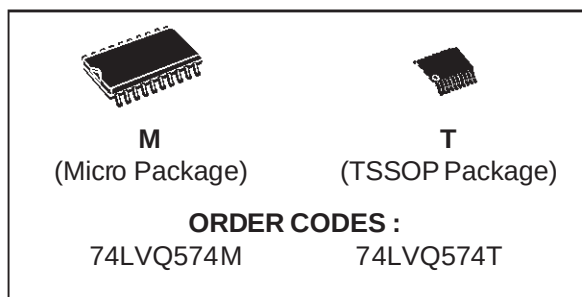
OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUTS NON INVERTING

- HIGH SPEED:
 $f_{MAX} = 180 \text{ MHz (TYP.)}$ at $V_{CC} = 3.3\text{V}$
- COMPATIBLE WITH TTL OUTPUTS
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A (MAX.)}$ at $T_A = 25^\circ\text{C}$
- LOW NOISE:
 $V_{OLP} = 0.5 \text{ V (TYP.)}$ at $V_{CC} = 3.3\text{V}$
- 75Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 12 \text{ mA (MIN)}$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \equiv t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2\text{V to } 3.6\text{V (1.2V Data Retention)}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 574
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The LVQ574 is a low voltage CMOS OCTAL D-TYPE FLIP FLOP with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring $C^2\text{MOS}$ technology. It is ideal for low power and low noise 3.3V applications.

These 8 bit D-Type flip-flops are controlled by a clock input (CK) and an output enable input (OE).



On the positive transition of the clock, the Q outputs will be set to logic state that were setup at the D inputs.

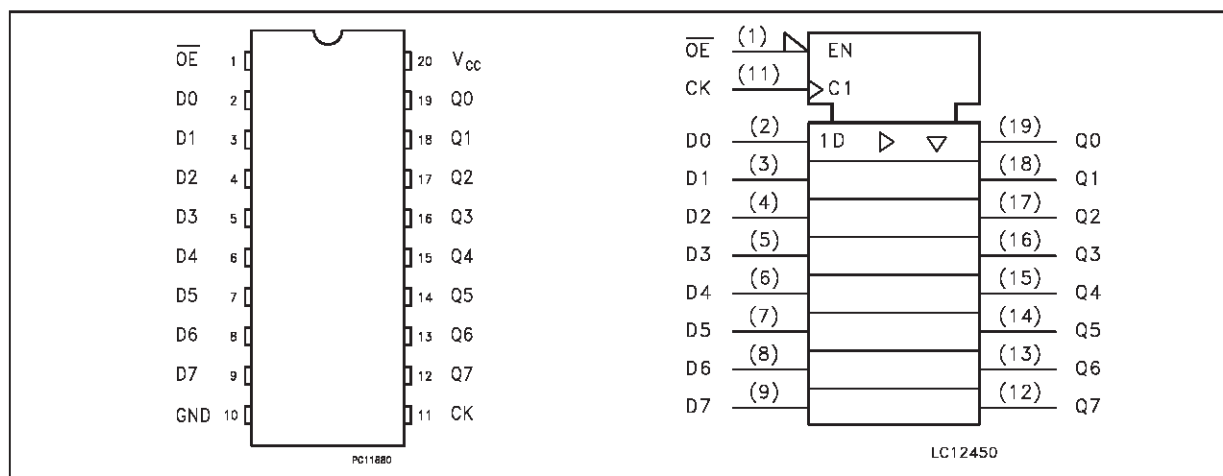
While the ($\overline{OE}$) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level, the outputs will be in a high impedance state.

The output control does not affect the internal operation of flip flop, that is, the old data can be retained or the new data can be entered even while the outputs are off.

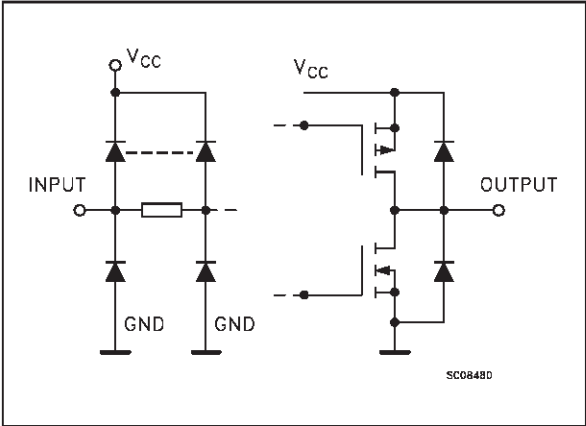
It has better speed performance at 3.3V than 5V LS-TTL family combined with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

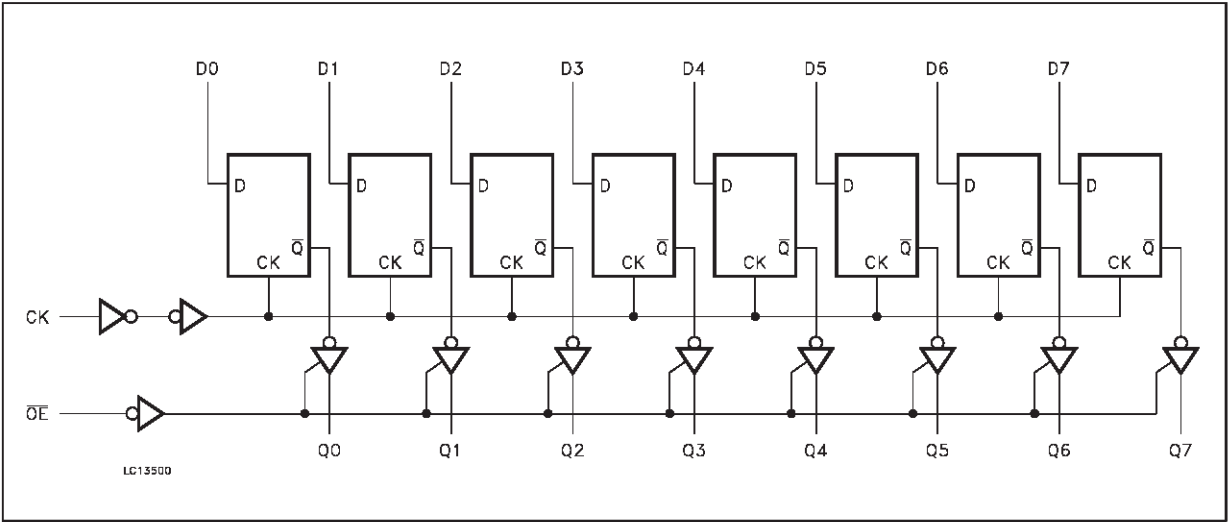
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3 State Outputs
11	CLOCK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

X: "H" or "L"
Z: High Impedance

LOGIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature (10 sec)	300	$^{\circ}\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature:	-40 to +85	$^{\circ}\text{C}$
dt/dv	Input Rise and Fall Time ($V_{CC} = 3\text{V}$) (note 2)	0 to 10	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2V

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C			
				Min.	Typ.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	3.0 to 3.6		2.0			2.0		V	
V _{IL}	Low Level Input Voltage					0.8		0.8	V	
V _{OH}	High Level Output Voltage	3.0	V _I ^(*) = V _{IH} or V _{IL}	I _O = -50 μA	2.9	2.99		2.9		V
				I _O = -12 mA	2.58			2.48		
				I _O = -24 mA				2.2		
V _{OL}	Low Level Output Voltage	3.0	V _I ^(*) = V _{IH} or V _{IL}	I _O = 50 μA		0.002	0.1		0.1	V
				I _O = 12 mA		0	0.36		0.44	
				I _O = 24 mA					0.55	
I _I	Input Leakage Current	3.6	V _I = V _{CC} or GND			±0.1		±1	μA	
I _{OZ}	3 State Output Leakage Current	3.6	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		±2.5	μA	
I _{CC}	Quiescent Supply Current	3.6	V _I = V _{CC} or GND			4		40	μA	
I _{OLD}	Dynamic Output Current	3.6	V _{OLD} = 0.8 V max				36		mA	
I _{OHD}	(note 1, 2)		V _{OHD} = 2 V min				-25		mA	

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.

(*) All outputs loaded.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{OLP}	Dynamic Low Voltage	3.3	C _L = 50 pF		0.5	0.8			V
V _{OLV}	Quiet Output (note 1, 2)			-0.8	-0.6				
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3				2			
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3		0.8					

1) Worst case package

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND

3) max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f=1MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 3 \text{ ns}$)

Symbol	Parameter	Test Condition		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time CK to Q	2.7 3.3 ^(*)			7.5 6.0	17.0 11.0		18.0 12.0	ns
t _{PLZ} t _{PHZ}	Output Disable Time	2.7 3.3 ^(*)			8.0 6.5	20.0 14.0		21.0 15.0	
t _{PZL} t _{PZH}	Output Enable Time	2.7 3.3 ^(*)			8.0 6.5	18.0 12..0		19.0 13.0	ns
t _w	Clock pulse Width, HIGH or LOW	2.7 3.3 ^(*)			2.0 1.5	5.0 4.0		6.0 4.0	
t _{sL} t _{sH}	Setup Time D to CK HIGH or LOW	2.7 3.3 ^(*)			0.0 0.0	2.5 2.0		3.0 2.5	ns
t _{hL} t _{hH}	Hold Time D to CK HIGH or LOW	2.7 3.3 ^(*)			0.0 0.0	2.5 2.0		3.0 2.5	
f _{MAX}	Maximum Clock Frequency	2.7 3.3 ^(*)		80 100	150 180		70 90		MHz
t _{OSLH} t _{OSHL}	Output to Output Skew Time (note 1, 2)	2.7 3.3 ^(*)			0.5 0.5	1.0 1.0		1.5 1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHl}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLl}|$)

2) Parameter guaranteed by design

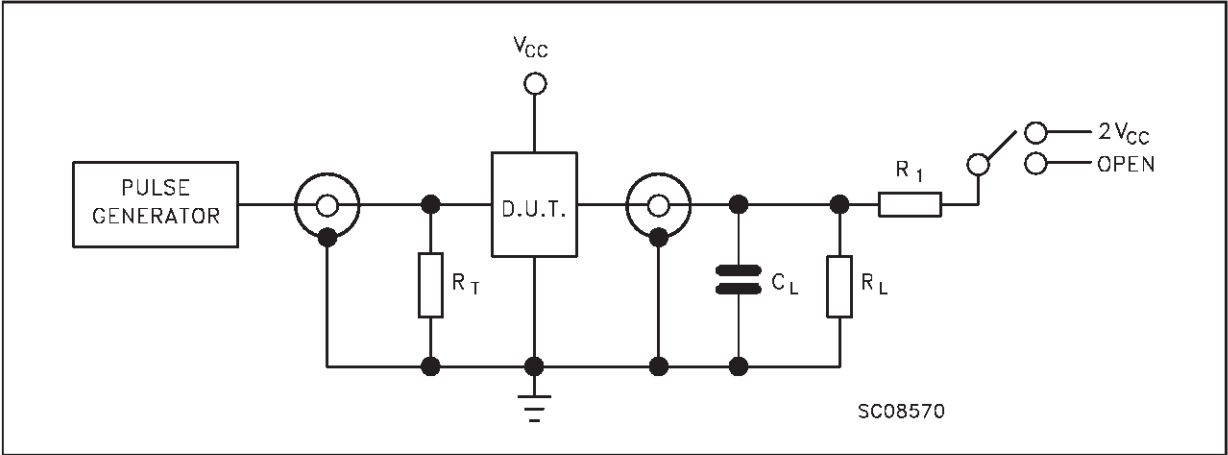
(*) Voltage range is $3.3V \pm 0.3V$

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance	3.3			4				pF
C _{OUT}	Output Capacitance	3.3			10				pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3	f _{IN} = 10 MHz		15				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CD}/8$ (per Flip Flop)

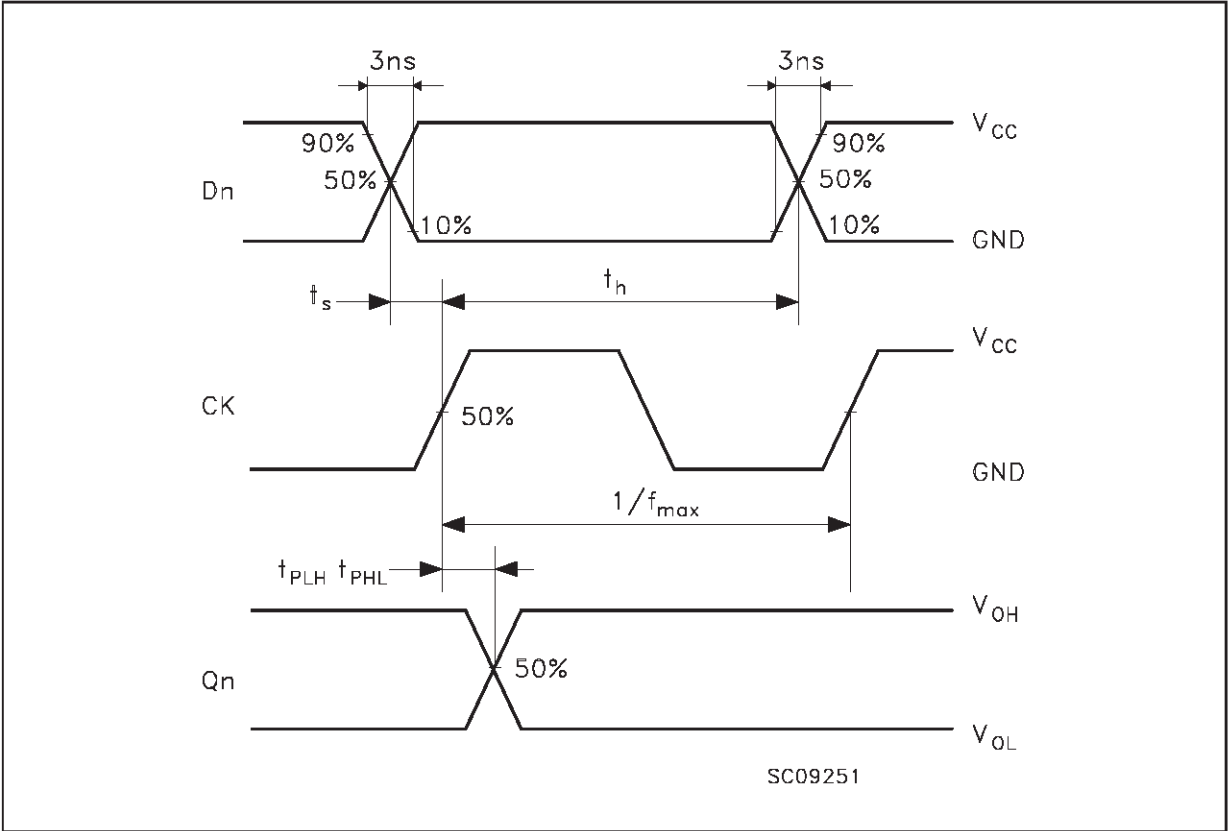
TEST CIRCUIT

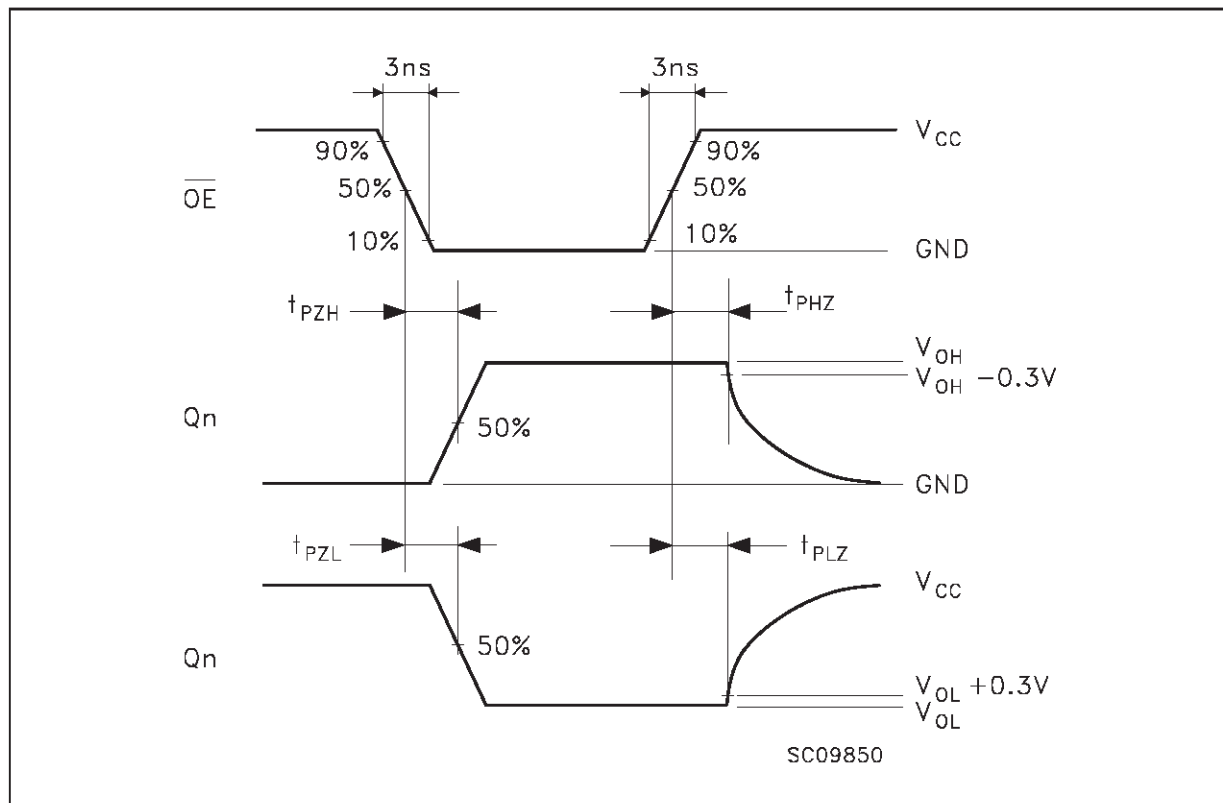
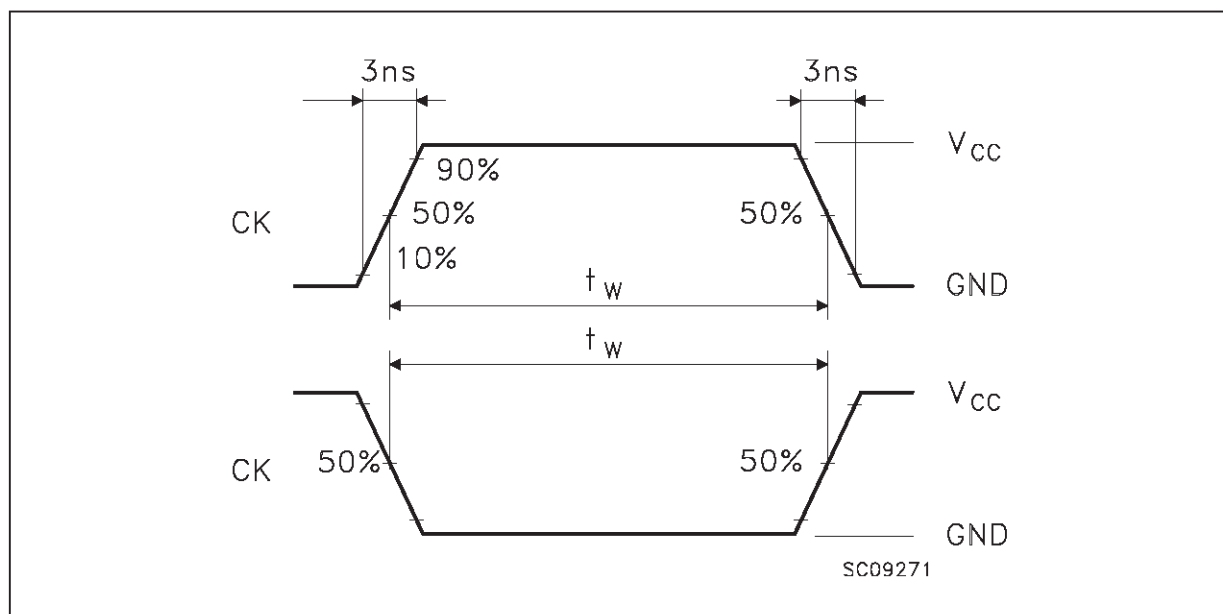


TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	$2V_{CC}$
t_{PZH} , t_{PHZ}	Open

C_L = 50 pF or equivalent (includes jig and probe capacitance)
 R_L = R_1 = 500 Ω or equivalent
 R_T = Z_{OUT} of pulse generator (typically 50 Ω)

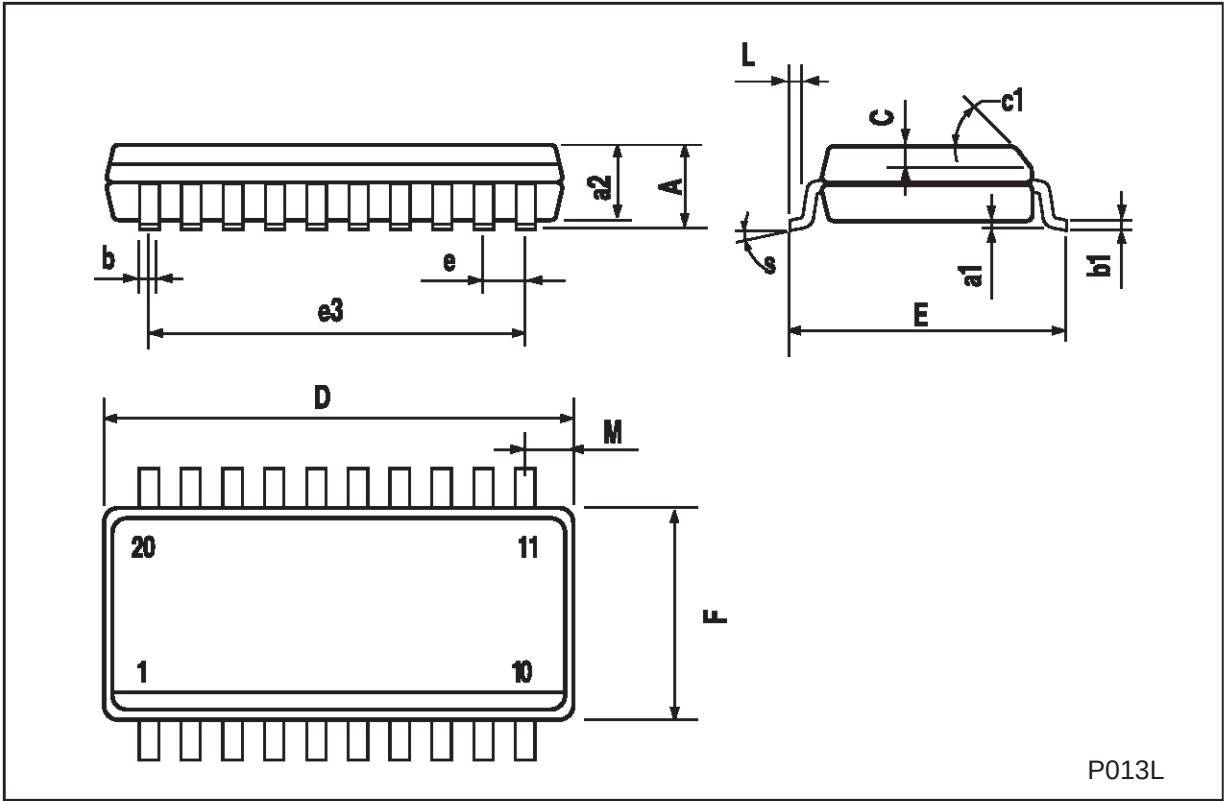
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 3: PULSE WIDTH**

SO-20 MECHANICAL DATA

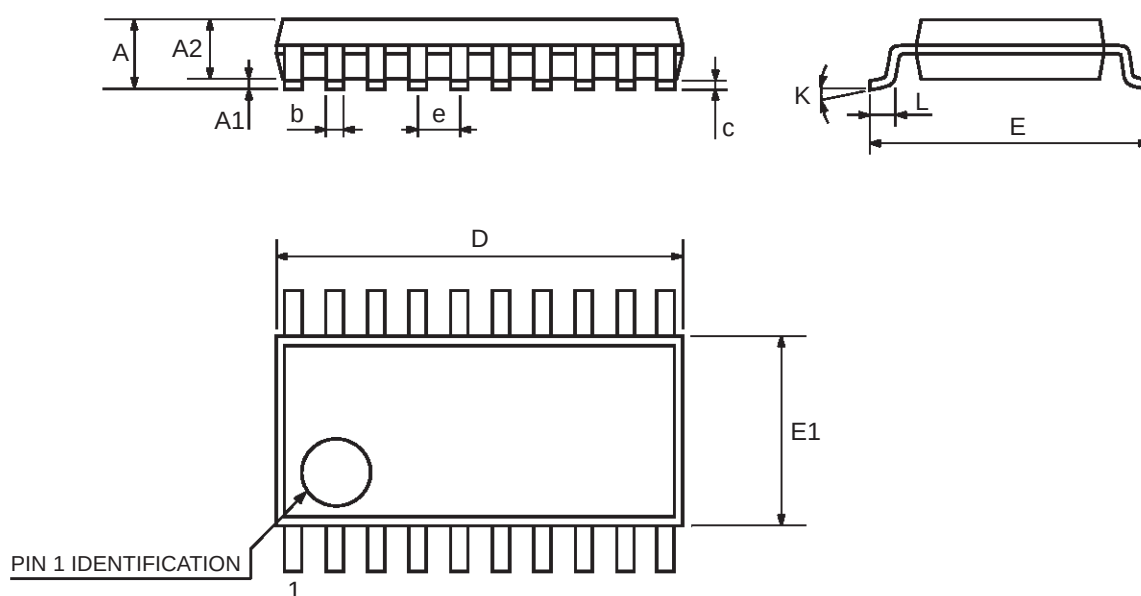
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45 (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
M			0.75			0.029
S	8 (max.)					



P013L

TSSOP20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.2	0.0035		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1999 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands - Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.

<http://www.st.com>