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CDB4329
CDB4390

Evaluation Board for CS4329 and CS4390

Features

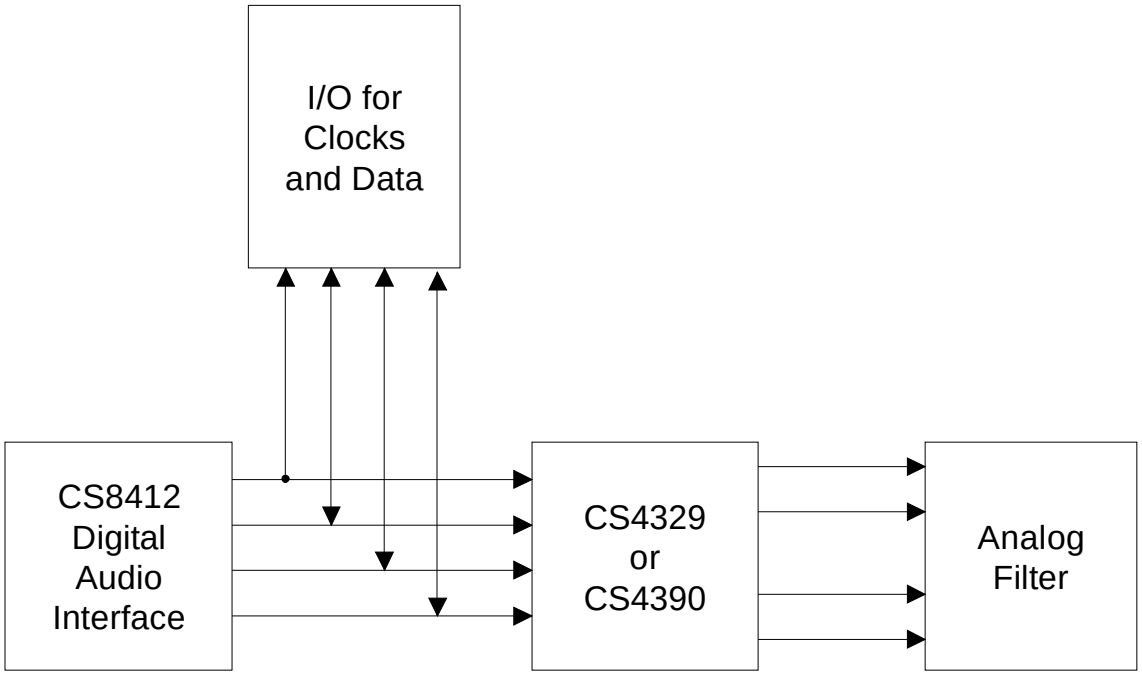
- Demonstrates recommended layout and grounding arrangements
- CS8412 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

Description

The CDB4329/90 evaluation board is an excellent means for quickly evaluating the CS4329 or CS4390 24-bit, stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source and a power supply. Analog outputs are provided via RCA connectors for both channels.

The CS8412 digital audio receiver I.C. provides the system timing necessary to operate the CS4329/90 and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFO
CDB4329
CDB4390



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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CDB4329/90 SYSTEM OVERVIEW

The CDB4329/90 evaluation board is an excellent means of quickly evaluating the CS4329/90. The CS8412 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply clocks and data through a 10-pin header for system development.

The CDB4329/90 schematic has been partitioned into 8 schematics shown in Figures 2 through 9. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

CS4329/90 Digital to Analog Converter

A description of the CS4329 or CS4390 is included in the CS4329 and CS4390 data sheets.

CS8412 Digital Audio Receiver

The system receives and decodes the standard S/PDIF data format using a CS8412 Digital Audio Receiver, Figure 9. The outputs of the CS8412 include a serial bit clock, serial data, left-right clock (FSYNC), de-emphasis control and a 256Fs master clock.

During normal operation, the CS8412 operates in the Channel Status mode where the LED's display channel status information for the channel selected by the CSLR/FCK jumper. This allows the CS8412 to decode and supply the de-emphasis bit from the digital audio interface for control of the CS4329/90 de-emphasis filter via pin 3, CC/F0, of the CS8412.

When the Error Information Switch is activated, the CS8412 operates in the Error and Frequency information mode. The information displayed by the LED's can be decoded by consulting the CS8412 data sheet. If the Error Information Switch is activated, the CC/F0 output has no relation to the de-emphasis bit and it is likely that the de-emphasis control for the CS4329/90 will be erroneous and produce an incorrect audio output.

Encoded sample frequency information can be displayed provided a proper clock is being applied to the FCK pin of the CS8412. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8412. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option of CSLR/FCK should be selected if the FCK pin is being driven by a clock signal.

The evaluation board has been designed such that the input can be either optical or coax, Figure 8. It is not necessary to select the active input. However, both inputs can not be driven simultaneously.

Data Format

The CS4329/90 must be configured to be compatible with the incoming data and can be set with DIF0, DIF1, and DIF2. The CS8412 data format can be set with the M0, M1, M2 and M3. There are several data formats which the CS8412 can produce that are compatible with CS4329/90. Refer to Table 2 for one possibility.

Power Supply Circuitry

Power is supplied to the evaluation board by four binding posts, Figure 10. The +5 Volt input supplies power to the CS4329/90 (through VA+), the CS8412 (through VA+ and VD+), and the +5 Volt digital circuitry (through VD+). The ±12 volt input supplies power to the analog filter circuitry.

Input/Output for Clocks and Data

The evaluation board has been designed to allow the interface to external systems via the 10-pin header, J1. This header allows the evaluation board to accept externally generated clocks and data. The schematic for the clock/data I/O is shown in Figure 7. The 74HC243 transceiver functions as an I/O buffer where the CLK SOURCE jumper determines if the transceiver operates as a transmitter or receiver.

The transceiver operates as a transmitter with the CLK SOURCE jumper in the 8412 position. LRCK, SDATA, and SCLK from the CS8412 will be available on J1. J22 must be in the 0 position and J23 must be in the 1 position for MCLK to be an output and to avoid bus contention on MCLK.

The transceiver operates as a receiver with the CLK SOURCE jumper in the EXTERNAL position. LRCK, SDATA and SCLK on J1 become inputs. The CS8412 must be removed from the evaluation board for operation in this mode.

There are 2 options for the source of MCLK in the EXT CLK source mode. MCLK can be an input with J23 in the 1 position and J22 in the 0 position. However, the recommended mode of operation is to generate MCLK on the evaluation board. MCLK becomes an output with LRCK, SCLK and SDATA inputs. This technique insures that the CS4329/90 receives a jitter free clock to maximize performance. This can be accomplished by installing a crystal oscillator into U4, see Figure 9 (the socket for U4 is located within the footprint for the CS8412) and placing J22 in the 1 position and J23 in the 0 position.

Analog Filter

The design of the second-order Butterworth lowpass filter, Figure 6, is discussed in the CS4329 and CS4390 data sheets and the applications note "Design Notes for a 2-pole Filter with Differential Input."

Grounding and Power Supply Decoupling

The CS4329/90 requires careful attention to power supply and grounding arrangements to optimize performance. The recommended power arrangements would be VA+ connected to a clean +5 Volt supply. The voltage VD+ (pin 6 of the CS4329/90) should be derived from VA+ through a 2 ohm resistor and should not used for any additional digital circuitry. Ideally, mode pins which require this voltage should be connected directly to VD+ (pin 6 of the CS4329/90) and mode pins which require DGND should be connected directly to pin 5 of the CS4329/90. AGND and DGND, Pins 4 and 5, are connected together at the CS4329/90. However, it was not possible to connect VD+ (pin 6 of the CS4329/90) and DGND to the mode pins on the CDB4329/90 due to layout complications resulting from the hardware selected to exercise the features of the CS4329/90.

Figure 2 shows the CS4329/90 and connections. The evaluation board has separate analog and digital regions with individual ground planes. DGND for the CS4329/90 should not be confused with the ground for the digital section of the system (GND). The CS4329/90 is positioned over the analog ground plane near the digital/analog ground plane split. These ground planes are connected elsewhere on the board. This layout technique is used to minimize digital noise and to insure proper power supply matching/sequencing. The decoupling capacitors are located as close to the CS4329/90 as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yield large reductions in radiated noise effects.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5V	input	+5 Volts for the CS4329/90, CS8412 and digital section
±12V	input	±12 volts for analog filter section
GND	input	ground connection from power supply
Digital input	input	digital audio interface input via coax
Optical input	input	digital audio interface input via optical
J1	input/output	I/O for system clocks and digital audio data
AOUTL	output	left channel analog output
AOUTR	output	right channel analog output

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8412 channel status information	L R	See CS8412 data sheet for details
Clock Select	Selects source of system clocks and data	*8412 EXT	CS8412 clock/data source External clock/data source
J22 J23	Selects MCLK as input or output	0 1	See *Input/Output for Clocks and Data* section of text
M0 M1 M2 M3	CS8412 mode select	*Low *Low *Low *Low	See CS8412 data sheet for details
auto_mute	CS4329/90 Auto Mute	*Low High	On Off
DEM0 DEM1	De-emphasis select	*High *Low	See CS4329 and CS4390 data sheets for details set for 44.1 kHz
DIF0 DIF1 DIF2	CS4329/90 digital input format	*High *High *Low	See CS4329 and CS4390 data sheets for details
SCLK	CS4329/90 SCLK Mode	*INT EXT	Internal SCLK Mode External SCLK Mode
DEM_8412	Selects source of de-emphasis control	*Low High	CS8412 de-emphasis De-emphasis input static high

Notes: 1. * Default setting from factory

Table 2. CDB4329/90 Jumper Selectable Options

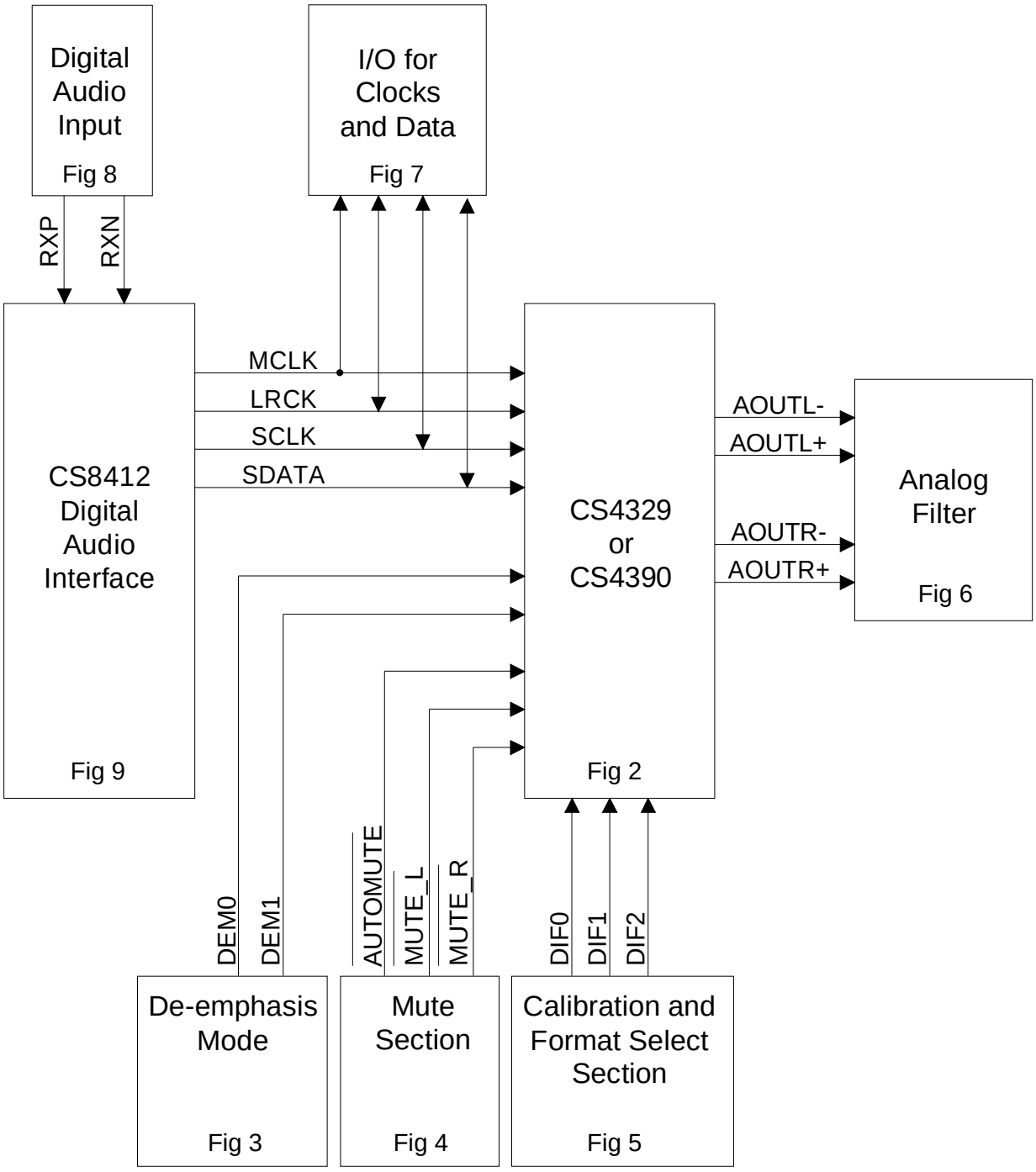


Figure 1. System Block Diagram and Signal Flow

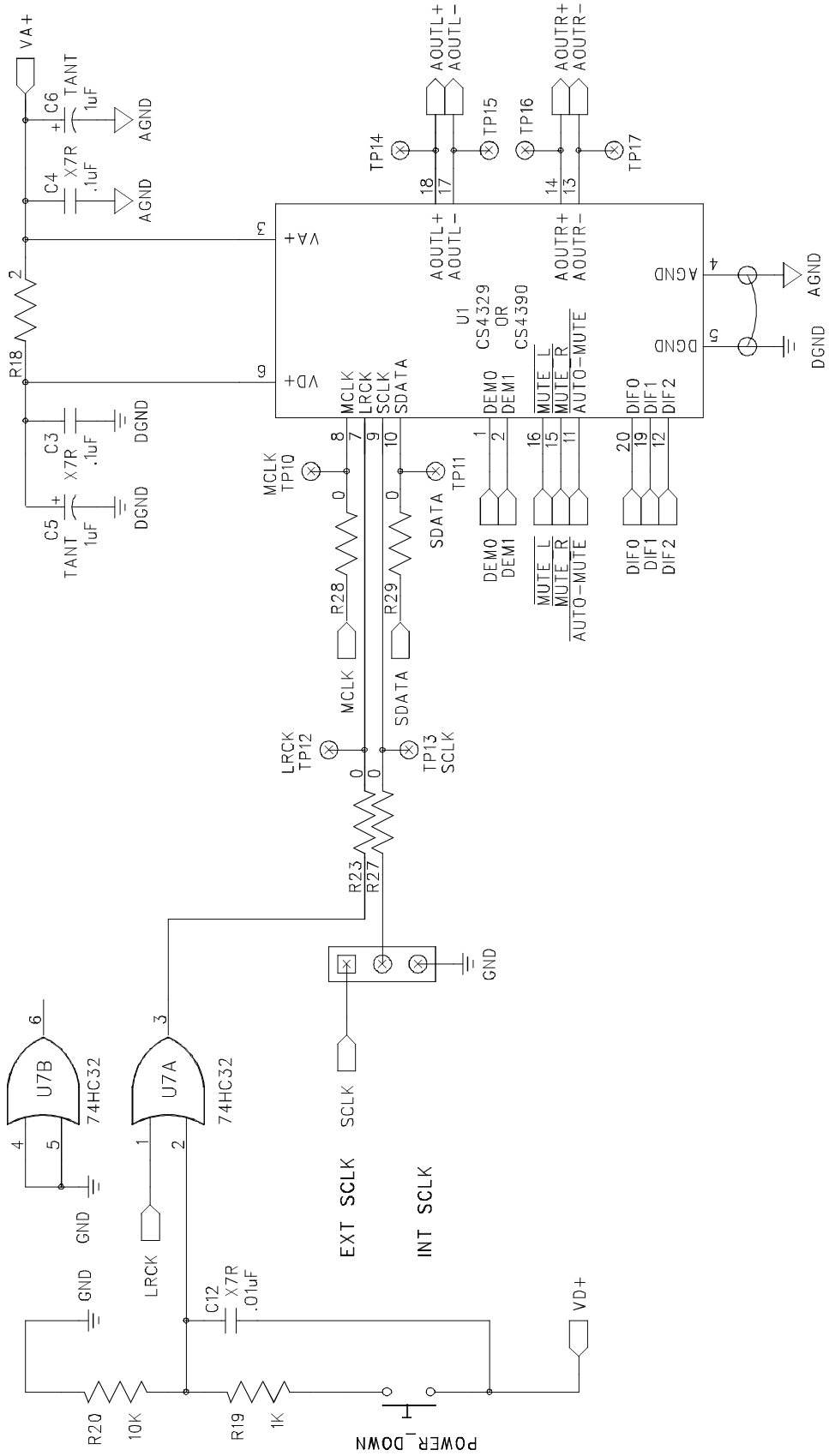


Figure 2. CS4329/90 and Connections

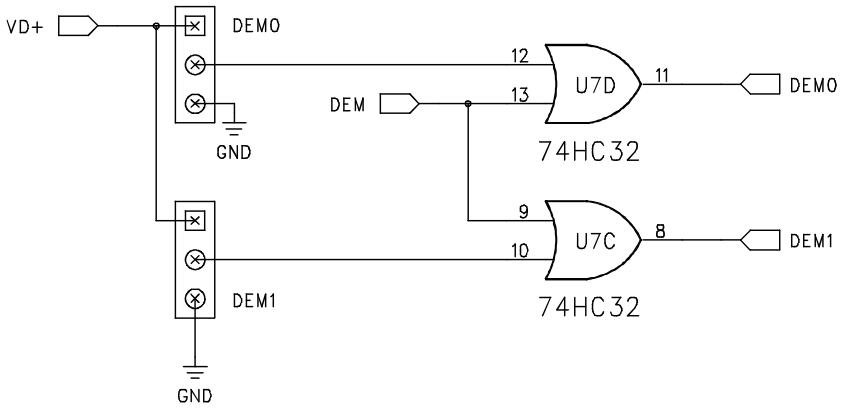


Figure 3. De-emphasis Circuitry

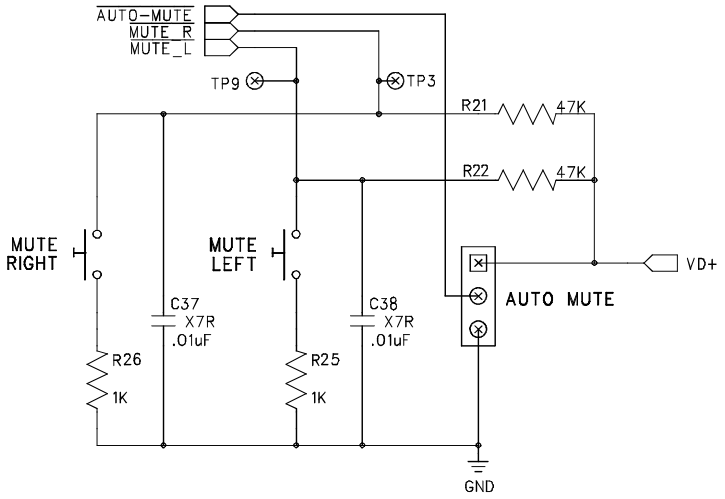


Figure 4. Mute Circuitry

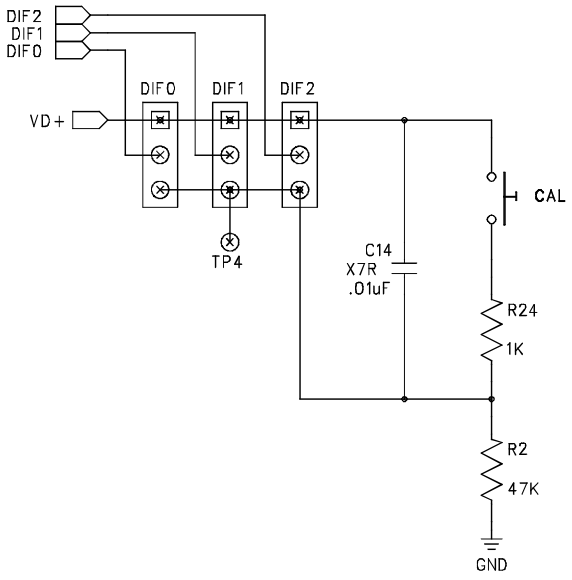
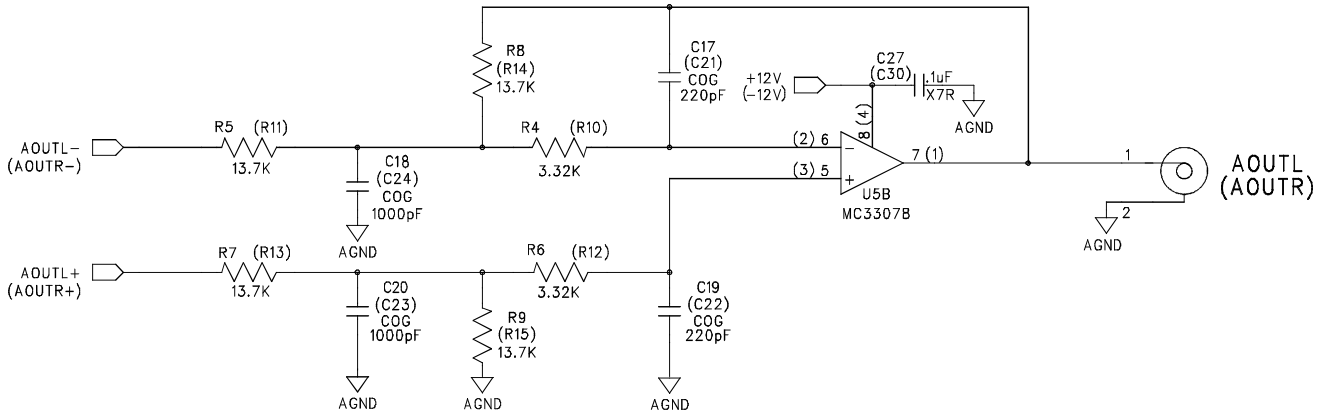


Figure 5. Calibration and Format Select Circuitry



NOTE: Rigth channel components in parentheses.

Figure 6. 2-pole Analog Filter

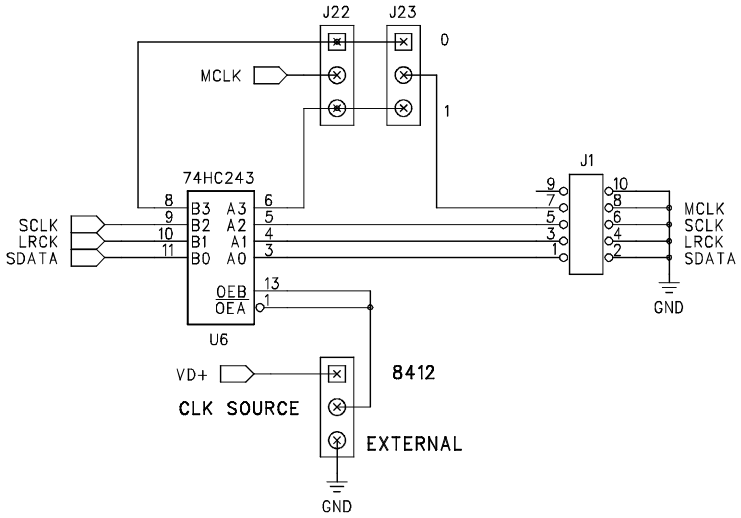
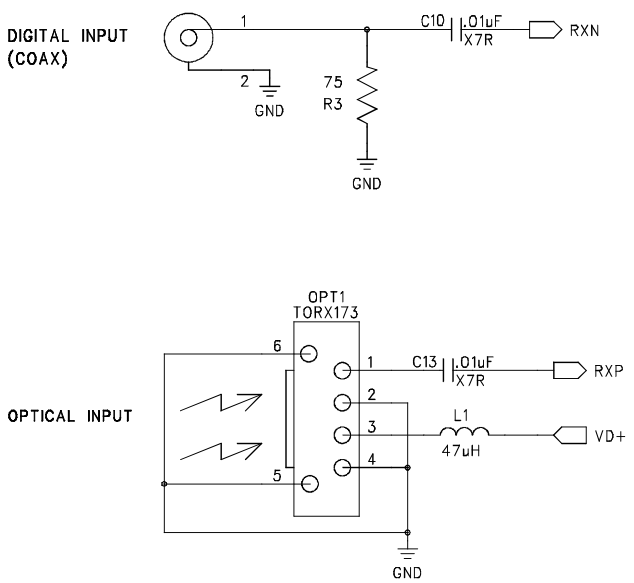
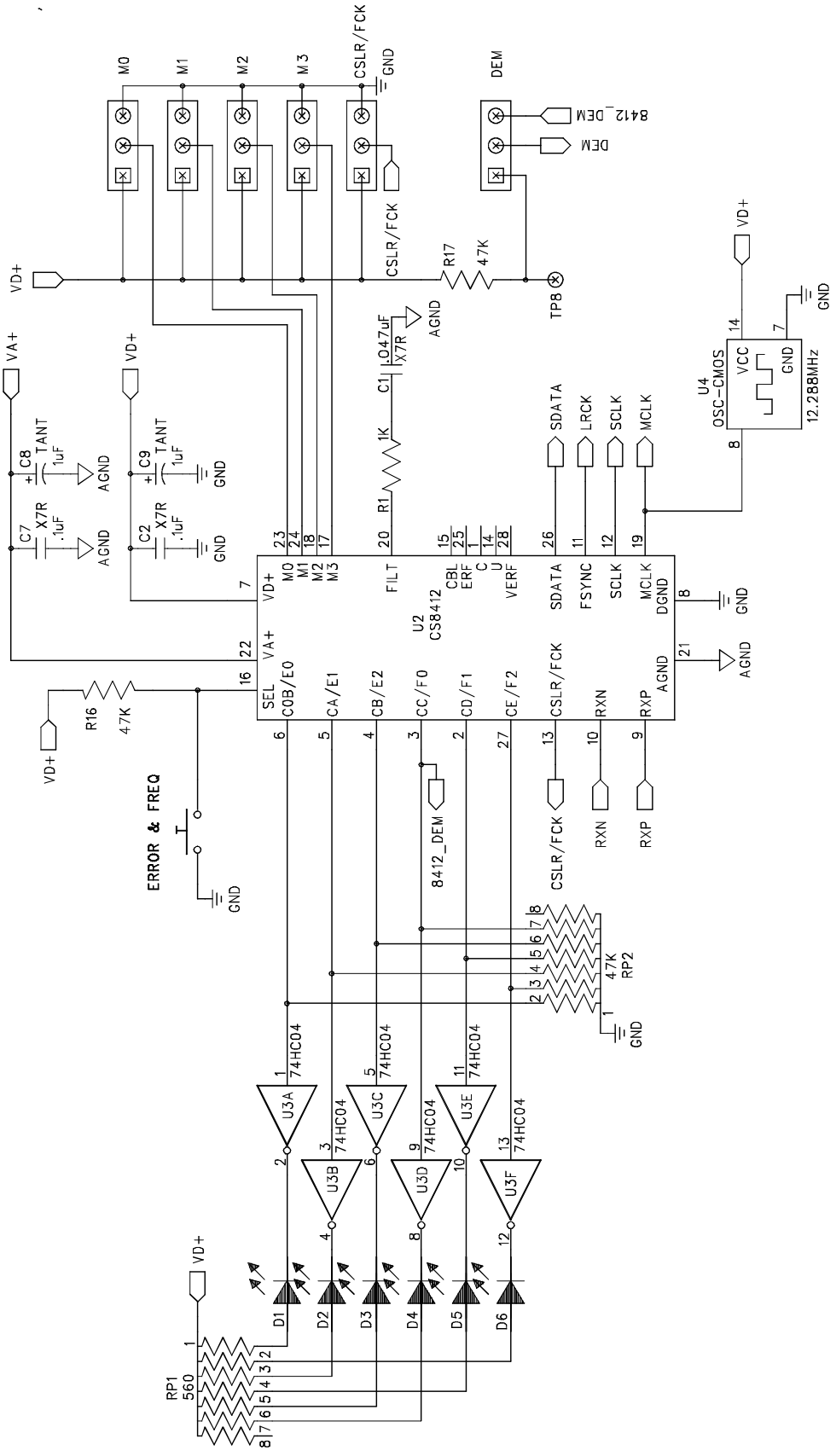


Figure 7. I/O Interface for Clocks and DATA



OPTI Toshiba TORX173 optical receiver available from Insight Electronics

Figure 8. Digital Audio Input Circuit



Note: U2 and U4 can not be installed simultaneously.

Figure 9. CS8412 and Connections

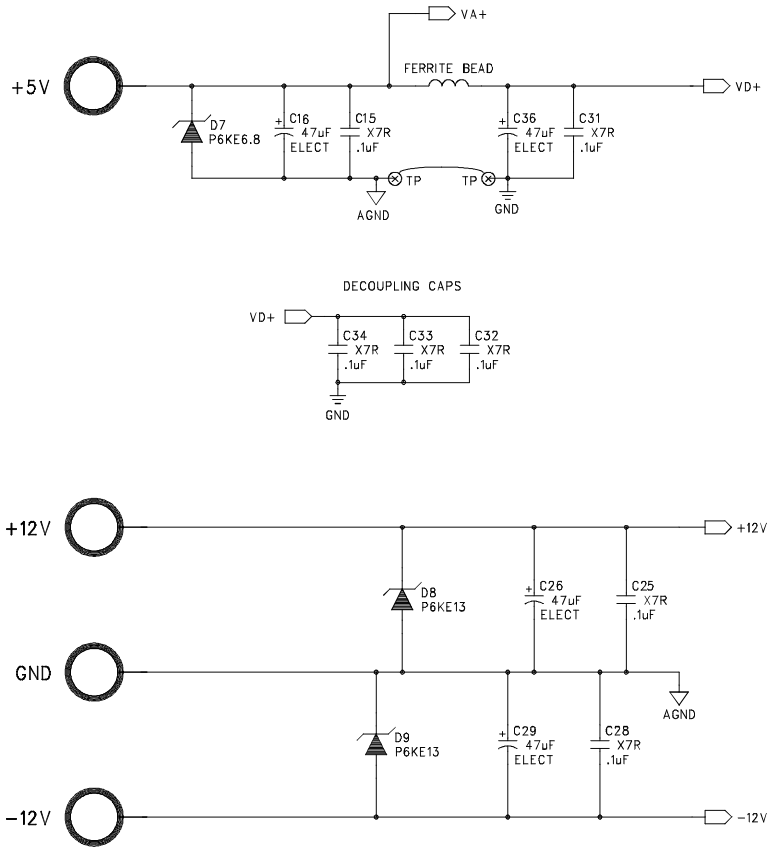


Figure 10. Power Supply Connections

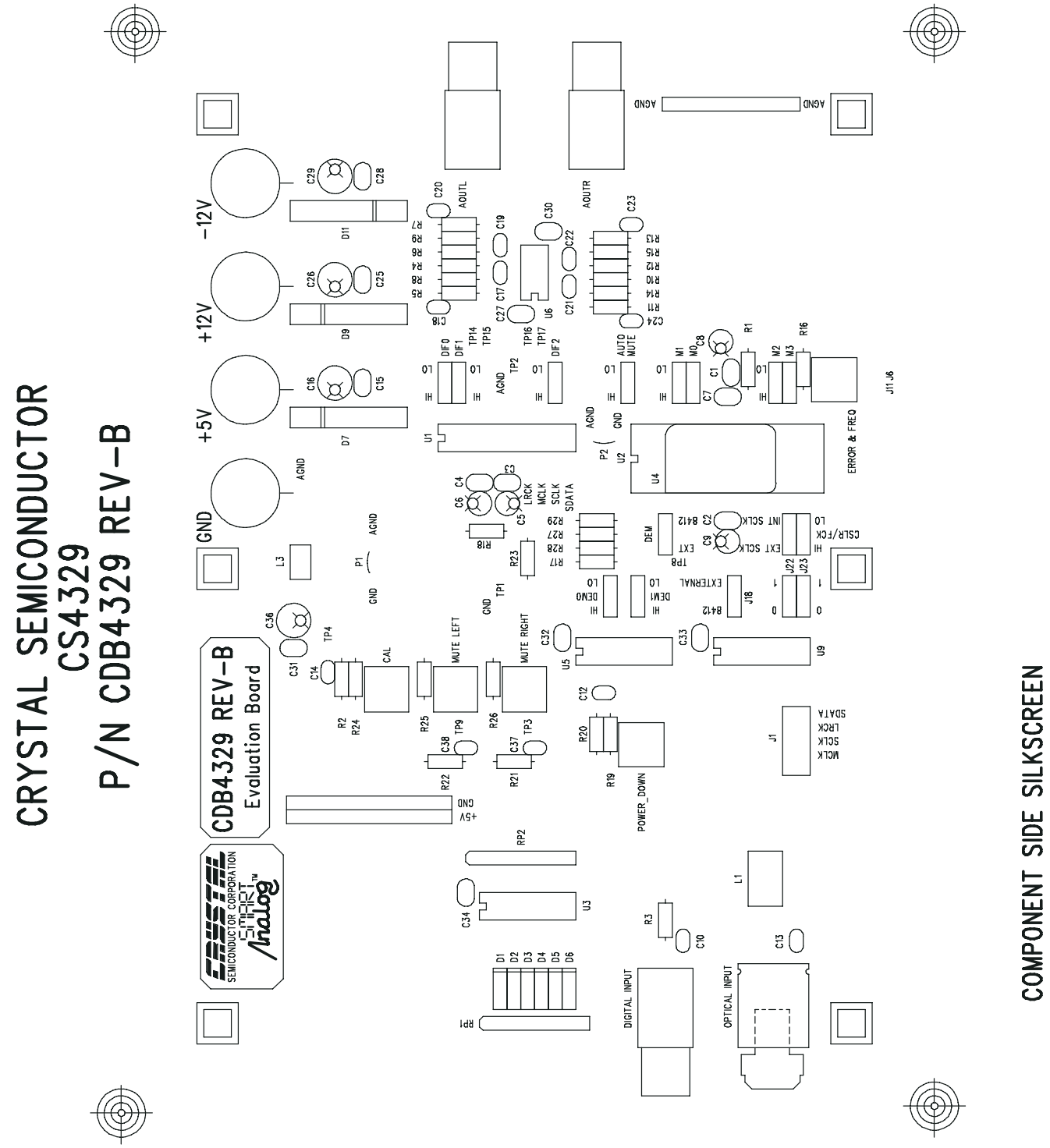


Figure 11. CDB4329/90 Component Side Silkscreen

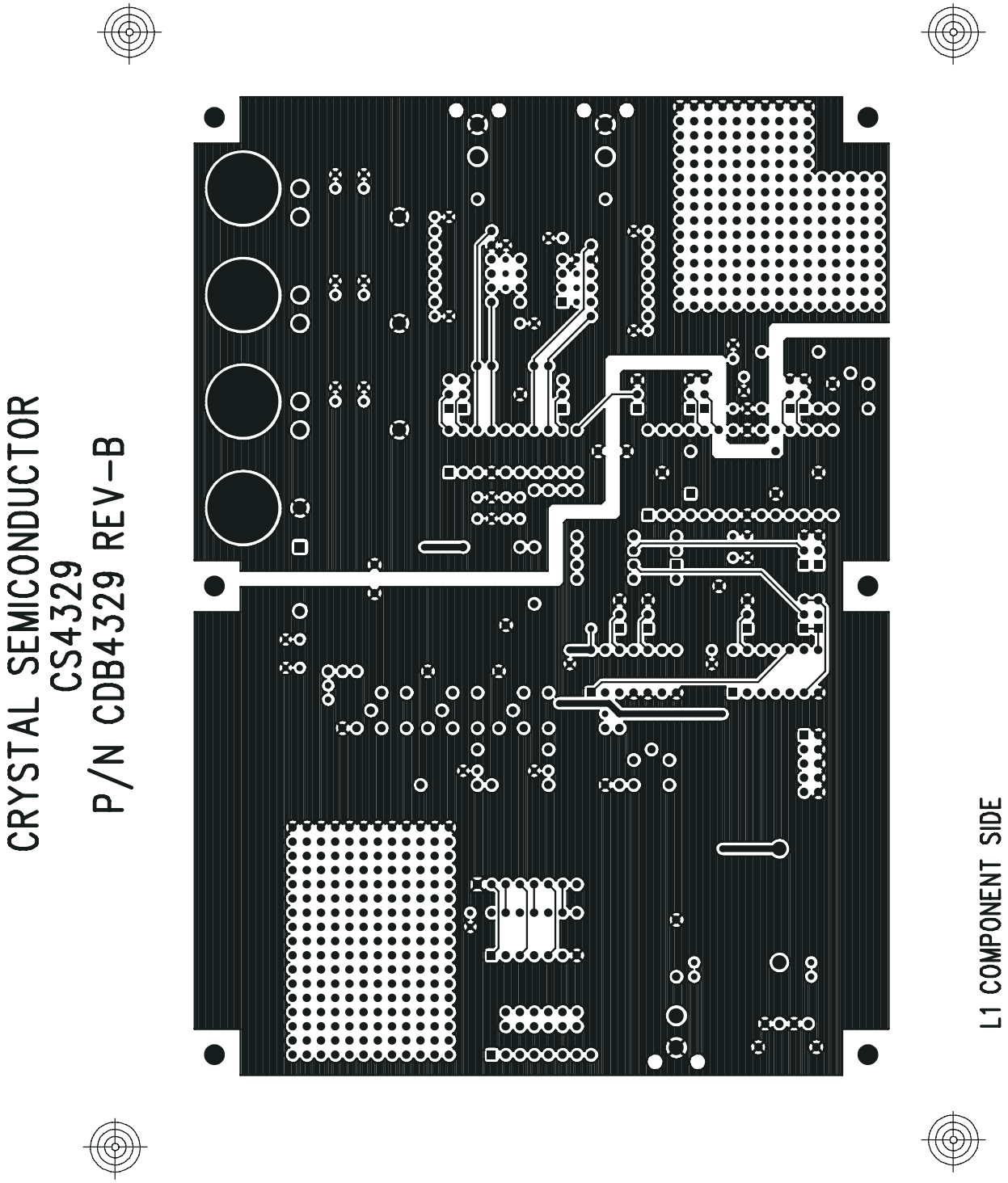


Figure 12. CDB4329/90 Component Side (top)

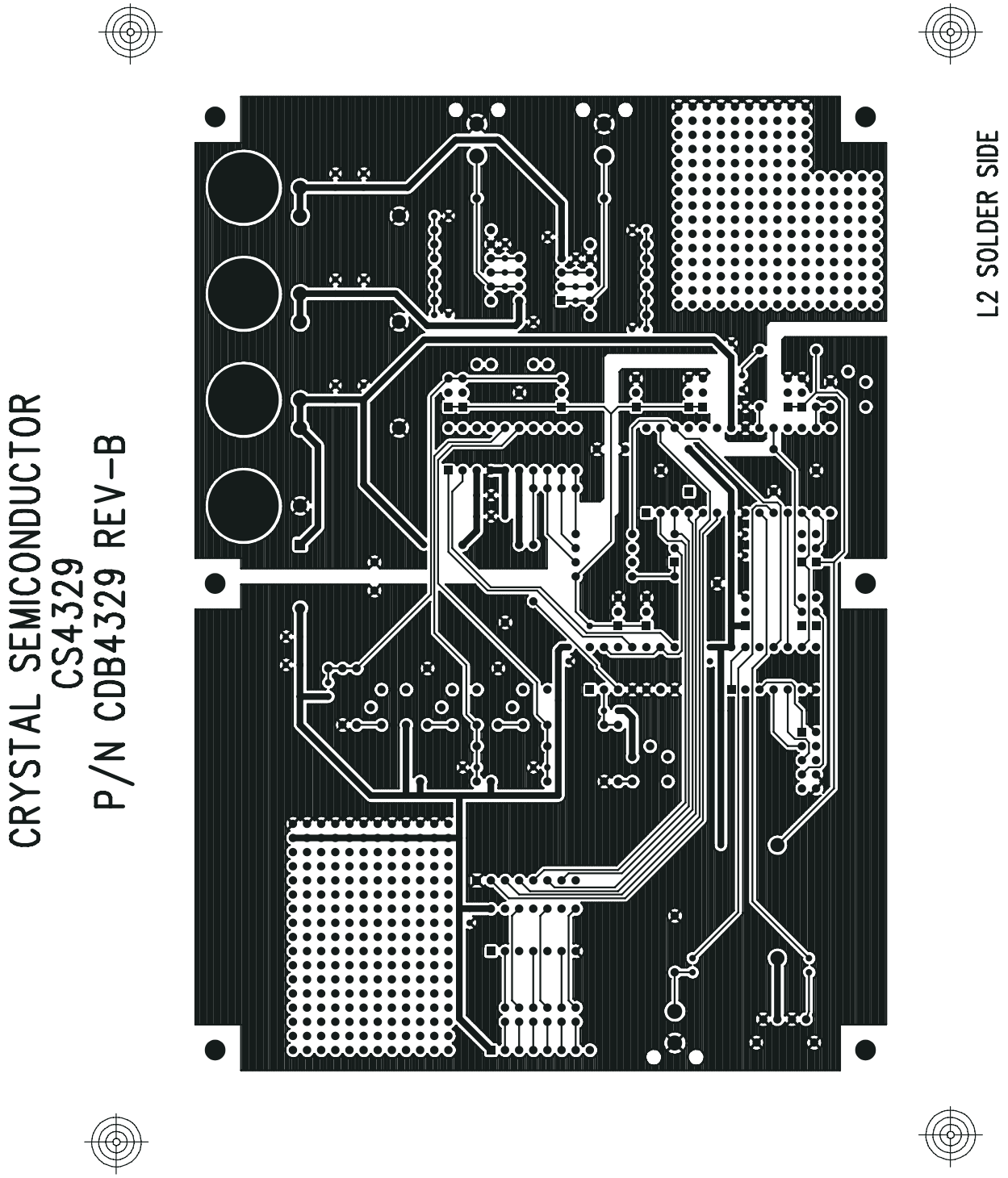


Figure 13. CDB4329/90 Solder Side (bottom)

• Notes •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