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SP8790

60MHz÷4 (2-MODULUS EXTENDER)

The SP8790 is a divide-by-four counter designed for use with 2-modulus dividers. It increases the minimum division ratio of the 2-modulus divider while retaining the same difference in division ratio. The device is suitable for use in low power frequency synthesis interfacing to CMOS or TTL.

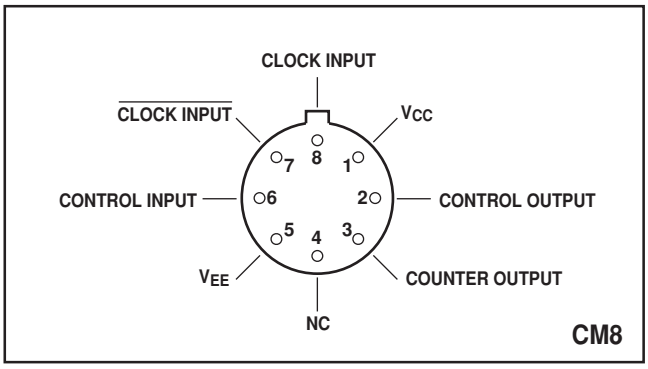


Fig. 1 Pin connections - bottom view

FEATURES

- Very Low Power
- Control Input and Counter Output will Interface Directly to TTL or CMOS
- Interfaces to GPS SP8000 Series Programmable 2-Modulus Dividers

QUICK REFERENCE DATA

- Supply Voltage: 5·0V
- Power Consumption: 40mW
- Temperature Range: −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p
Output sink current	10mA

ORDERING INFORMATION

SP8790 A CM
SP8790 B CM

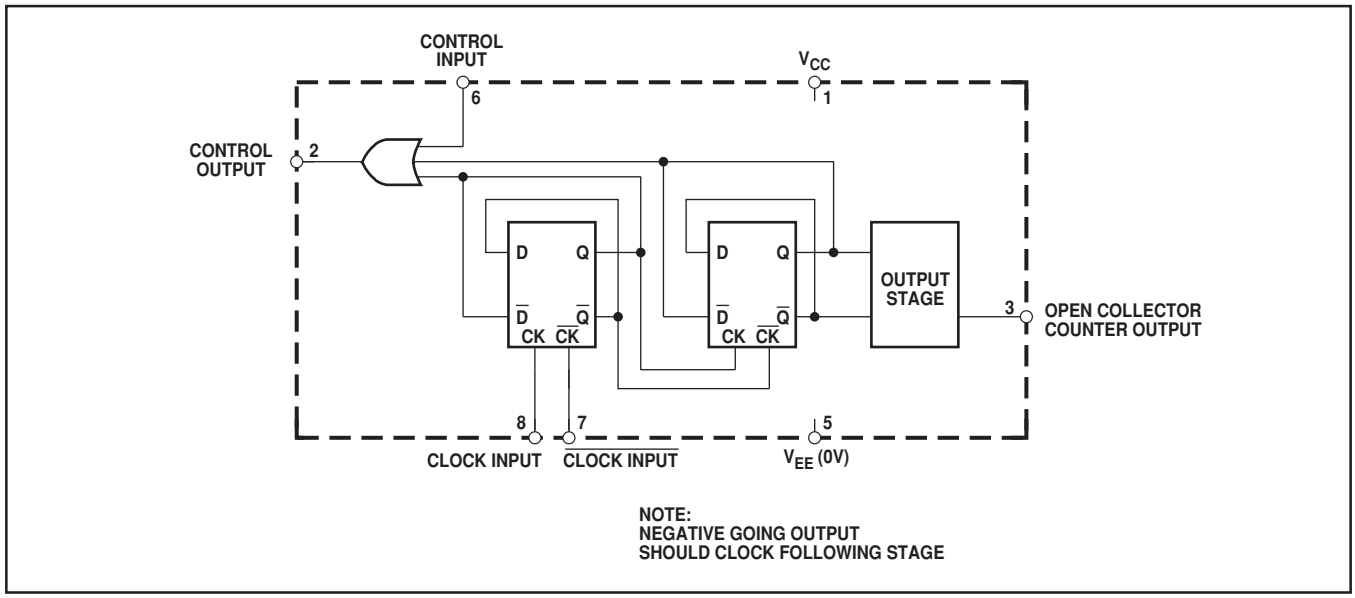


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

Supply voltage, V_{CC} = 5V ±0·25V, V_{EE} = 0V

Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	60		MHz	Tested as a controller, see Fig. 4	2
Power supply current	I_{CC}		11	mA		2
Control input high voltage	V_{INH}	3·5	10	V		2
Control input low voltage	V_{INL}	0	1·5	V		2
Output high voltage (pin 3)	V_{OH}	9		V	Pin 3 via 1·6kΩ to+10V	2
Output low voltage (pins 3)	V_{OL}		0·4	V	Pin 3 via 1·6kΩ to+10V	2
Output high voltage (pin 2)	V_{OH}	4·27	4·5	V	V_{CC} = 5·2V (25°C)	
Output low voltage (pin 2)	V_{OL}	3·28	3·7	V	V_{CC} = 5·2V (25°C)	
Clock to counter output −ve going delay	t_{pHL}		25	ns		3
Clock to counter output +ve going delay	t_{pLH}		40	ns		3
Clock to control output −ve going delay	t_{pHL}		15	ns	10kΩ pull-down on control output	3, 4
Clock to control output +ve going delay	t_{pLH}		26	ns	10kΩ pull-down on control output	3, 4
Control input to control output −ve going delay	t_{pHL}		12	ns	10kΩ pull-down on control output	3, 4
Control input to control output +ve going delay	t_{pLH}		16	ns	10kΩ pull-down on control output	3, 4

NOTES

1. The test configuration for dynamic testing is shown in Fig.4.
2. Tested at low and high temperatures only.
3. Guaranteed but not tested.
4. The propagation delays stated are with the device controlling the SP8695, which has internal 10kΩ pull-down resistors on its PE inputs. These propagation delays will be reduced when the device is used with the SP8643/47 and SP8740 series of 2-modulus dividers, which have internal 4·3kΩ pull-downs. Refer to relevant data sheet/s.

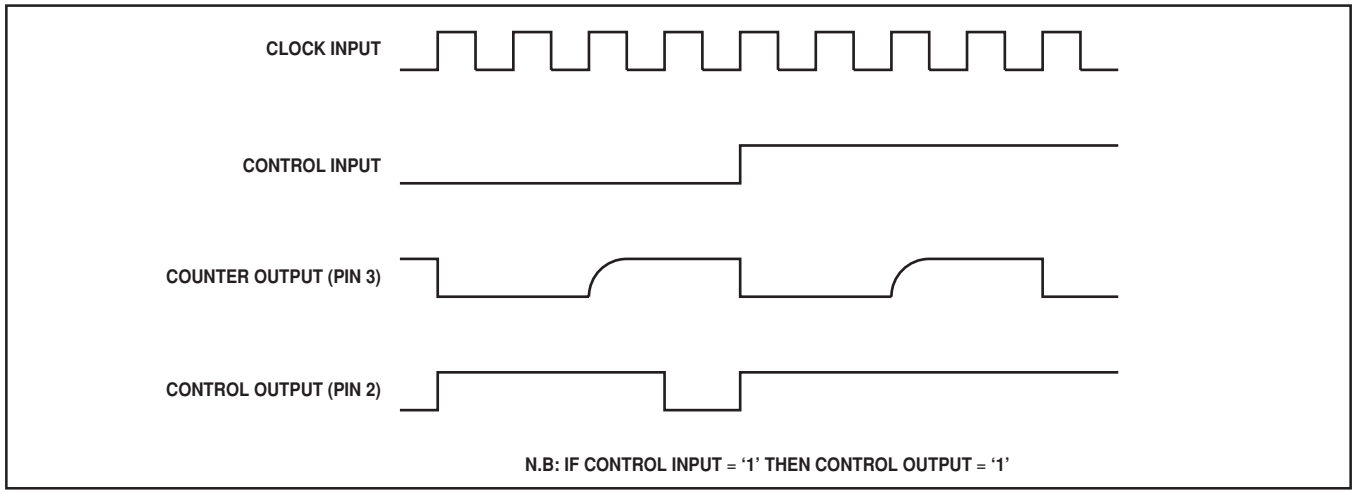


Fig. 3 Timing diagram

OPERATING NOTES

1. The device will normally be driven by capacitively coupling the inputs to the outputs of a 2-modulus divider, as shown in Figs. 4 and 5. The maximum frequency of the device when used as a controller is limited by the internal delays to 60MHz. However, when used as a ÷4 prescaler, it will operate at frequencies in excess of 80MHz, the maximum frequency being limited by saturation of the output stage.
2. The device is normally driven from very fast edges of a 2-modulus divider, in which case there is no input slew rate problem.
3. The control input is TTL/CMOS compatible.
4. The counter output (pin 3) interfaces to TTL/CMOS by the addition of a pull-up resistor. For interfacing to CMOS, the output can be connected with a pull-up resistor to a supply which must not exceed 12V.
5. When used as a controller the device will self-oscillate in the absence of an input signal; this can be prevented by connecting a 47kΩ resistor from pin 7 to ground, as shown in Fig. 5.
6. The control output, which includes an internal 16kΩ pull-down resistor, is ECL compatible and will interface directly to ECL 2-modulus dividers such as the GPS SP8600 and SP8700 series as shown in Figs. 4 and 5.

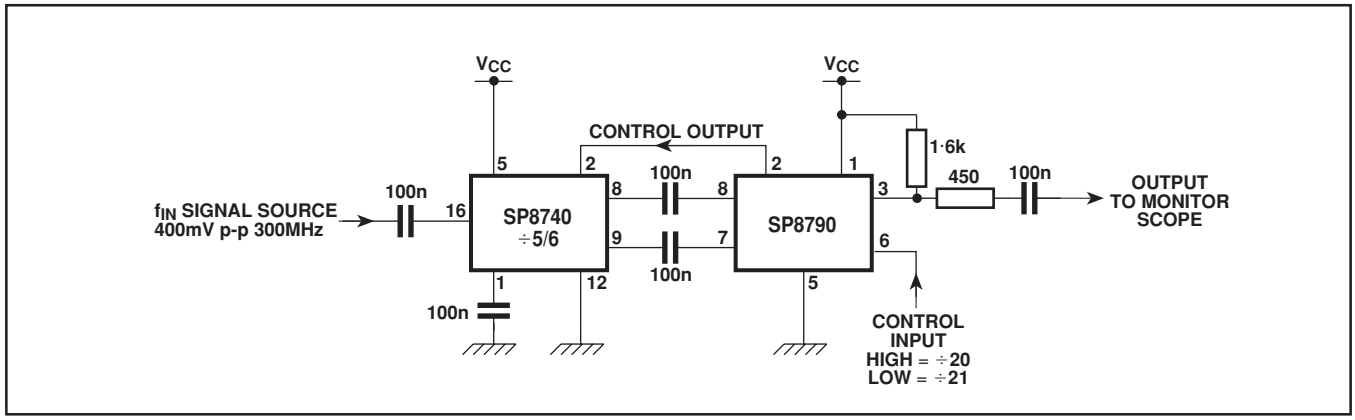


Fig. 4 Test circuit

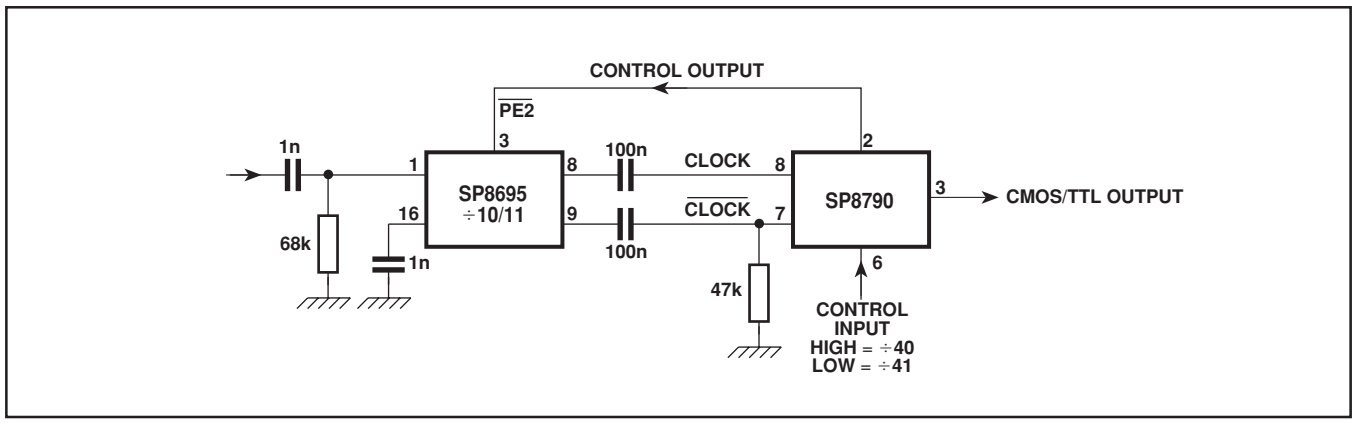
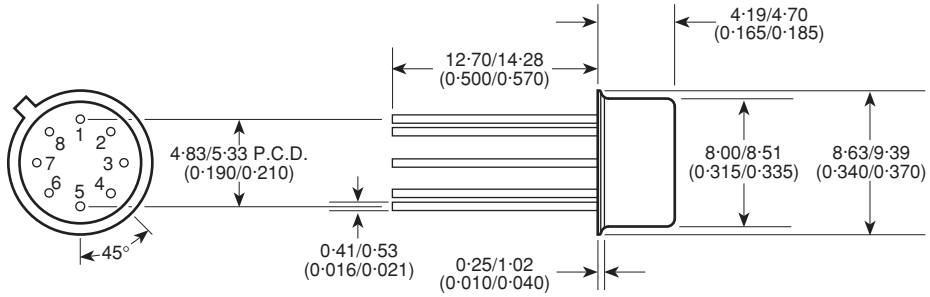


Fig. 5 Typical interfacing to suppress oscillation with no input signal

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

8-LEAD METAL CAN - CM8

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