Preliminary Specifications

SST 28LP040
3.0V-only 4 Megabit
PCMCIA Interface EEPROM

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Features:

Single 3.0-Volt Read and Write Operations

CMOS SuperFlash EEPROM Technology
- Endurance: 250,000 Cycles (typical)
- Greater than 100 years Data Retention

Memory Organization:
- 512K x 8/1M x 4 PCMCIA common memory
- 1K x 8/2K x 4 attribute memory for user alterable PCMCIA attribute memory

Low Power Consumption:

Active Current:	10 mA	(typical)
Standby Current:	5 µA	(typical)

Fast Sector Erase and Byte Program Operation

Byte Program Time:	30 µs	(typical)
Sector Erase Time:	60 µs	(typical)
Complete Memory Rewrite:	15 sec	(typical)

Fast Access Time: 250 ns

Sector Erase Capability:
- 256 bytes/512 nibbles per Sector

Selectable single Nibble & dual Nibble Access

PCMCIA Byte-wide or Word wide selection

Latched Address and Data

Hardware and Software Data Protection
- WP pin Hardware Write Protection
- 7-read-cycle-sequence Software Data Protection

End of Write Detection
- Toggle Bit
- Data# Polling

TTL I/O Compatibility

Packages Available
- 40-Pin TSOP (10 mm x 14 mm)

Product Description

The 28LP040 is organized as a 512K x 8 (bits) common memory array plus a 1K x 8 attribute memory array. The attribute memory can be accessed by asserting REG# or issuing an Enable_Attribute command. Either one nibble or two nibbles in a byte can be read in one cycle with internal decoding of CEL#, CEH#, and HB. The 28LP040 must be configured as a pair per 1Mbyte of PCMCIA application memory. Each byte in the PCMCIA memory map consists of two nibbles, one from each 28LP040 in the pair.

Each 28LP040 has 4M bits of common memory and 8K bits of attribute memory and is manufactured using SST's proprietary, high performance CMOS SuperFlash EEPROM Technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternative approaches. The 28LP040 erases and programs with a 3.0 volt only power supply. (V_{CC}: 3.0V to 3.6V)

Figure 1 shows the functional blocks of the 28LP040, and shows the memory map consisting of common memory array and the attribute memory array. Figure 2 shows the pin assignments for the TSOP package. Pin description and operation modes are described in Tables 1 through 6.

Device Operation

Commands are used to initiate the memory operations functions of the device. Commands are written to the device using standard microprocessor write sequences. The device is selected by applying the proper input levels to CS_0 and CS_1 (see Table 2A). A command is written by asserting WE# low while keeping CEL# or CEH# low. The address bus is latched on the falling edge of WE#, CEL#, or CEH#, whichever occurs last. The data bus is latched on the rising edge of WE# or CEL#, whichever occurs first. Note, during the software data protection sequence the address are latched on the rising edge of OE# or CEL#, whichever occurs first.

Memory Map

The 28LP040 consists of two memory arrays: the common memory and the attribute memory. The common memory consists of 1M-nibbles and is used for storing data, program codes and other user files. The total available attribute memory is 2K nibbles. The selection between the common and attribute memory maps is controlled by the REG# pin. When REG# is high, the common memory is active. Alternatively, the attribute memory can be accessed through an Enable_Attribute command, which enables the attribute memory access independent of REG#.

Two sectors of the attribute memory are used to store the map of nonconforming sectors. Refer to Table 9 for details. A maximum of zero nonconforming attribute memory sectors and five nonconforming common memory sectors are allowed when the 28LP040 is shipped.

Command Definitions

Table 7 contains a command list and a brief summary of the commands. The following is a detailed description of the operations initiated by each command.

Sector_Erase Operation

The Sector_Erase operation erases all byte within a sector and is initiated by a setup command and an execute command. A sector contains 512 nibbles. This sector erasability enhances the flexibility and usefulness of the 28LP040, since most applications only need to change a small number of bytes or sectors, not the entire chip.

The setup command is performed by writing 22H to the device. To execute the Sector_Erase operation, the execute command (DDH) must be written to the device. The erase operation begins with the rising edge of the WE# pulse and terminates with the Reset command. The device has an internal timer that will terminate the erase (into the read mode) after T_{SE} if no Reset command has been sent. The end of Erase can be determined using either Data# Polling, Toggle Bit or Successive Reads detection methods. See Figure 9 for timing waveforms.

The two-step sequence of setup command followed by an execute command ensures that only memory contents within the addressed sector are erased and other sectors are not inadvertently erased.

Erase_Verify

The Erase_Verify operation is initiated by writing a single command (AAH). The address bus is latched on the falling edge of WE#, CEL#, or CEH#, whichever occurs last. The Erase_Verify is used only to verify that the device has erased prior to programming. The Erase_Verify uses an internal reference level to provide extra margin com-pared to normal read levels for “FF” data. This operation automatically resets after reading the byte.

Sector_Erase Flowchart Description

Fast and reliable erasing of the memory contents within a sector is accomplished by following the algorithmic sector erase flowchart as shown in Figure 20. The Sector_Erase operation will terminate after a maximum of 2 ms, if not interrupted. After the initial 40 µs of erase time, a Reset command can be executed to terminate the erase operation followed by an Erase_Verify operation to assure complete erasure. The algorithmic Sector_Erase operation allows for up to seven erase iterations to complete the Sector_Erase. A sector erase iteration is perform by doubling the algorithmic sector erase sector time (T_{ASE} = 40 µs , 80 µs, 160 µs, 320 µs, 640 µs, 1.28 ms and 2.56 ms). The purpose of the successive erase attempts is to optimize the total time required to erase the sector. An additional 150 erase retries at maximum T_{ASE} is allowed to ensure erasure.

Byte_Program Operation

The Byte_Program operation is initiated by writing the setup command (11H). Once the program setup is performed, programming is executed by the next WE# pulse. See Figures 5 and 6 for timing waveforms. The address bus is latched on the falling edge of WE#, CEL# or CEH#, which ever occurs last. The data bus is latched on the rising edge of WE#, CEL# or CEH#, which ever occurs first. The rising edge of WE#, CEL# or CEH#, which ever occurs first, begins the program operation. The program operation is terminated automatically by an internal timer. See Figure 18 for the programming flowchart.

The two-step sequence of a setup command followed command ensures that only the addressed byte is programmed and other bytes are not inadvertently programmed.

The Byte_Program Flowchart Description

Programming data into the 28LP040 is accomplished by following the Byte_Program flowchart shown in Figure 18. The Byte_Program command sets up the byte for programming. The address bus is latched on the falling edge of WE#, CEL# or CEH#, which ever occurs last. The data bus is latched on the rising edge of WE#, CEL# or CEH#, which ever occurs first and begins the po

gram operation. The end of program can be detected using either the Data# Polling or Toggle bit.

Reset Operation

The Reset command is provided as a means to safely abort the erase or program command sequences. Follow either setup commands (erase or program) with a write of FFH will safely abort the operation. Memory contents will not be altered. After the Reset command, the device returns to the read mode. The Reset command does not enable software data protection. See Figure 7 for timing waveforms.

Read

The Read operation is initiated by setting CEL#, CEH#, and OE# to logic low and setting WE# to logic high (See Table 3). See Figure 4 for read memory timing diagram. The read operation from the host retrieves data from the array. The device remains enabled for read until another operation mode is accessed. During initial power-up, the device is in the read mode and is software data protected. The device must be unprotected to execute a write command.

The read operation of the 28LP040 is controlled by OE# at logic low and either CEL# and/or CEH# at logic low. When CEL# and CEH# are high, the chip is deselected and only standby power will be consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when both CEL# and CEH# are high or OE# is high.

Enable_Attribute Operation

Attribute memory is access by initiating the Enable_Attribute operation with a single command (88H). Read, Sector_Erase, and Byte Program operations can be performed in the attribute memory. The 1K byte of memory includes the PCMCIA attribute memory information. The REG# pin status has no effect on the operation. To return to common memory operations, a Reset command must be issued. The Reset command enables access to the common memory. (See Figure 8)

Read_ID operation

The Read_ID operation is initiated by writing a single command (99H). A read of address 0000H will output the manufacturer's code (BFH). A read of address 0001H will output the device code (11H). Any other valid command will terminate this operation.

Data Protection

In order to protect the integrity of nonvolatile data storage, the 28LP040 provides both hardware and software features to prevent inadvertent writes to the device, for example, during system power-up or power-down. Such provisions are described below.

Hardware Data Protection

The 28LP040 is designed with hardware features to prevent inadvertent writes. This is done in the following ways:

1. Write Inhibit Mode: OE# low, CEL# high, CEH# high, or WE# high will inhibit the write operation.
2. Noise/Glitch Protection: A WE# pulse width of less than 15 ns will not initiate a write cycle.
3. V_{CC} Power Up/Down Detection: The write operation is inhibited when V_{CC} is less than 2.5 V.
4. After power-down the device is in the read mode and the device is in the software data protect state.
5. The WP pin at V_{IH} will put the device in the Write Protect mode.

Software Data Protection (SDP)

The 28LP040 has software methods to further prevent inadvertent writes. In order to perform an erase or program operation, a two-step command sequence consisting of a set-up command followed by an execute command avoid inadvertent erasing and programming of the device.

The 28LP040 will default to software data protection after power up. A sequence of seven consecutive reads at specific addresses will unprotect the device The address sequence is 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 041AH. The address bus is latched on the rising

edge of OE# or CEL#, whichever occurs first. A similar seven read sequence of 1823H, 1820H, 1822H, 0418H, 041BH, 0419H, 040AH will protect the device. Also refer to Figures 10 and 11 for the 7 read cycle sequence Software Data Protection. The I/O pins can be in any state (i.e., high, low, or tristate).

Write Operation Status Detection

The 28LP040 provides three software means to detect the completion of a write cycle, in order to optimize the system write cycle time. The end of a write cycle (erase or program) can be detected by three means: 1) monitoring the Data# Polling bit; 2) monitoring the Toggle bit; or by two successive read of the same data. These three detection mechanisms are described below.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with the DQ used. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the rejection is valid.

Data# Polling (DQ_3, DQ_7)

The 28LP040 features Data# Polling to indicate the write operation status. During a write operation, any attempt to read the last byte loaded will receive the complement of the true data on DQ_3 and DQ_7. Once the write cycle is completed, DQ_3 for the low nibble and DQ_7 for the high nibble will show true data. The device is then ready for the next operation. See Figure 14 for Data Polling timing waveforms. In order for Data# Polling to function correctly, the byte being polled must be erased prior to programming.

Toggle Bit (DQ_2, DQ_6)

An alternative means for determining the write operation status is by monitoring the Toggle Bit, DQ_2 for the low nibble and DQ_6 for the high nibble. During a write operation, consecutive attempts to read data from the device will result in DQ_2 and DQ_6 toggling between logic 0 (low) and logic 1 (high). When the write cycle is completed, the toggling will stop. The device is then ready for the next operation. See Figure 15 for Toggle Bit timing waveforms.

Successive Reads

An alternative means for determining an end of a write cycle is by reading the same address for two consecutive data matches.

Chip select (CS0, CS1)

The 28PC040 provides two user selectable chip select pins, CS0 and CS1. By ordering different part number suffix of a device, the device response only to one of the combinations of CS0 and CS1. See Table 2A. Therefore, there is no need of external decoder for up to 4 pairs of devices. Typically, the CS0 and CS1 are connected to address line A20 and A21. See application note "PCMCIA Memory Cards Made Easy with SST28PC040".

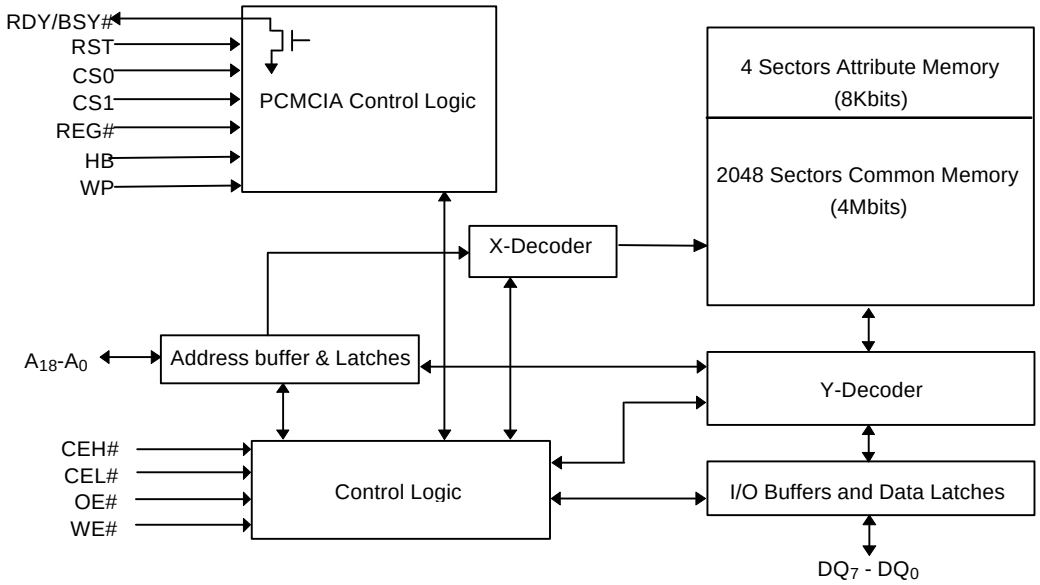


Figure 1: Functional Block Diagram of SST 28LP040

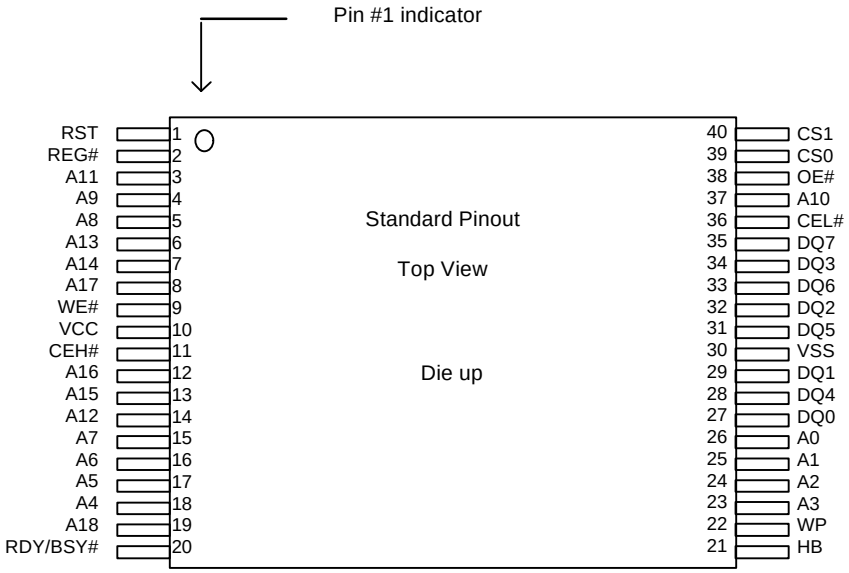


Figure 2: Standard Pin Assignments for 40-pin TSOP Pac kages.

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{18}-A_8	Row Address Inputs	To provide memory addresses. Row addresses define a sector.
A_7-A_0	Column Address Inputs	Selects the byte within the sector.
DQ_7-DQ_0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE#, CEL# or CEH# is high.
CEL#, CEH#	Chip Enable	To activate the device when CEL# or CEH# is low.(1) CEL# to enable the low nibble of DQ_0 to DQ_3 CEH# to enable the high nibble of DQ_4 to DQ_7
OE#	Output Enable	To gate the data output buffers.(1)
WE#	Write Enable	To control the write operations.(1)
Vcc	Power Supply	To provide 3.3-volt supply (± 0.3V)
Vss	Ground	
CS_0 - CS_1	Chip Selects	Preset chip selects used for memory pair select.(1) See Table 2A
HB	Half-Byte	Selects Odd/Even nibble for chip.(1)
WP	Write Protect	To activate write protect state.(1) When WP is high, the device becomes a ROM, acknowledging all read operation, and will ignore all operations attempting to alter memory array data. See Table 7.
RDY/BSY#	Read/Busy	This open-drain output requires a 1K pull-up resistor (minimum).(2) This pin is low to indicate the chip is busy internally. Any new instruction must be performed only when RDY/BSY# is high.
REG#	Attribute Memory	To switch from common memory to attribute memory.(1) There are 1Kbits of attribute memory in the 28LP040 decoded by A_9 to A_0. REG# can be overridden by the Enable_Attribute command.
RST	Reset	To reset the device after power-on.(1) RST must be asserted after power-up. After the falling edge of the RST pulse, the 28LP040 will be ready (RDY/BSY#) in ~ 10ms.

Note: (1) This pin is considered as an input for the purposes of the DC Operation Characteristics Table.
(2) This pin is considered as an output for the purposes of the DC Operation Characteristics Table.

Table 2: Operation Modes Selection

Mode	CEL#, CEH#	OE#	WE#	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Byte Program	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Sector Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Standby	V_{IH}	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	High Z/ D_{OUT}	X
Write Inhibit	X	X	V_{IH}	High Z/ D_{OUT}	X
Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	D_{IN}	See Table 7
Product Identification					
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	Manufacturer Code (BF)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IL}
				Device Code (11)	A_{18}-A_1=V_{IL}, A_9=V_H, A_0=V_{IH}
Software Mode	V_{IL}	V_{IH}	V_{IL}		See Table 7
SDP Enable & Disable Mode	V_{IL}	V_{IH}	V_{IL}		See Table 7
Enable_Attribute	V_{IL}	V_{IH}	V_{IL}		See Table 7
Reset	V_{IL}	V_{IH}	V_{IL}		See Table 7

Table 2A: Card Decode Table

Device Part# Suffix	CS_1	CS_0
S00A	0	0
S01B	0	1
S10C	1	0
S11D	1	1

Note: The chip is selected by applying the listed logic levels to CS_0 and CS_1. The device part # suffix indcates the preset state.

Table 3: Main Memory Read Functions

Function Mode	REG #	CEH #	CEL #	HB	OE#	WE#	DQ_{7-4} (1)	DQ_{3-0} (2)	A_{18}-A_0
Standby Mode	X	H	H	X	X	X	High Z	High Z	X
Nibble Access (x4) (3)	H	H	L	L	L	H	High Z	Even Nibble	A_{IN}
Nibble Access (x4) (3)	H	H	L	H	L	H	High Z	Odd Nibble	A_{IN}
Byte Access (x8) (3)	H	L	L	X	L	H	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access (3)	H	L	H	X	L	H	Odd Nibble	High Z	A_{IN}

Note: (1) D_{15}-D_8 in Figure 3

(2) D_7-D_0 in Figure 3

(3) CS1 and CS0 at active state.

Table 4: Main Memory Write Functions

Function Mode	REG #	CEH #	CEL #	HB	OE#	WE#	DQ_{7-4}[1]	DQ_{3-0}[2]	A_{18}-A_0
Standby Mode	X	H	H	X	X	X	X	X	X
Nibble Access (x4)[3]	H	H	L	L	H	L	X	Even Nibble	A_{IN}
Nibble Access (x4)[3]	H	H	L	H	H	L	X	Odd Nibble	A_{IN}
Byte Access (x8)[3]	H	L	L	X	H	L	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access[3]	H	L	H	X	H	L	Odd Nibble	X	A_{IN}
Write Inhibit	X	X	X	X	L	X	X	X	X

Note: [1]D_{15}-D_8 in Figure 3

[2]D_7-D_0 in Figure 3

[3]CS1 and CS0 at active state.

Table 5: Attribute Memory Read Functions

Function Mode	REG #	CEH #	CEL #	HB	OE#	WE#	DQ_{7-4}[1]	DQ_{3-0}[2]	A_9-A_0[3]
Standby Mode	X	H	H	X	X	X	High Z	High Z	X
Nibble Access (x4)[4]	L	H	L	L	L	H	High Z	Even Nibble	A_{IN}
Nibble Access (x4)[4]	L	H	L	H	L	H	High Z	Odd Nibble	A_{IN}
Byte Access (x8)[4]	L	L	L	X	L	H	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access[4]	L	L	H	X	L	H	Odd Nibble	High Z	A_{IN}

Note: ([1])D_{15}-D_8 in Figure 3

[2]D_7-D_0 in Figure 3

[3]Other addresses are “don’t care”

Table 6: Attribute Memory Write Functions

Function Mode	REG #	CEH #	CEL #	HB	OE#	WE#	DQ_{7-4} (1)	DQ_{3-0} (2)	A_9-A_0 (3)
Standby Mode	X	H	H	X	X	X	X	X	X
Nibble Access (x4) (4)	L	H	L	L	H	L	X	Even Nibble	A_{IN}
Nibble Access (x4) (4)	L	H	L	H	H	L	X	Odd Nibble	A_{IN}
Byte Access (x8) (4)	L	L	L	X	H	L	Odd Nibble	Even Nibble	A_{IN}
Odd Nibble Access (4)	L	L	H	X	H	L	Odd Nibble	X	A_{IN}
Write Inhibit	X	X	X	X	L	X	X	X	X

Note: (1) D_{15}-D_8 in Figure 3

(2) D_7-D_0 in Figure 3

(3) Other addresses are “don’t care”

Table 7: Software Command Summary

Command Summary	Required Cycle(s)	Setup Command Cycle			Execute Command Cycle			WP[6]	SDP[6]
		Type[1]	Addr[2, 3]	Data[4]	Type[1]	Addr[2, 3]	Data[4]		
Sector_Erase[10]	2	W	X	22H	W	SA	DDH	N	N
Byte_Program[10]	2	W	X	11H	W	PA	PD	N	N
Erase_Verify[10]	2	W	VA[5]	AAH	R	X	D_{OUT}	Y	Y
Reset[10]	1	W	X	FFH				Y	Y
Enable_Attribute[10]	1	W	X	88H				Y	Y
Read_ID[10]	3	W	X	99H	R	(9)	(9)	Y	Y
Software_Data_Protect[10]	7	R	(7)						
Software_Data_Unprotect[10]	7	R	(8)						

Notes:

1. Type definition: W = Write, R = Read, X= don't care
2. Addr (Address) definition: SA = Sector Address = A_{18} - A_8, sector size = 512 nibbles; A_7- A_0 = X for this command.
3. Addr (Address) definition: PA = Program Address = A_{18} - A_0.
4. Data definition: PD = Program Data, H = number in hex.
5. Addr (Address) definition: VA = Verify Address = A_{18} - A_0.
6. WP = Hardware Write Protect mode using WP pin, SDP = Software Data Protect mode using 7 Read Cycle Sequence.
   a) Y = the operation can be executed with protection enabled
   b) N = the operation cannot be executed with protection enabled
7. Refer to Figure 13 for the 7 Read Cycle sequence for Software_Data_Protect.
8. Refer to Figure 12 for the 7 Read Cycle sequence for Software_Data_Unprotect.
9. Address 0000H retrieves the manufacturer' code of BFH and address 0001H retrieves the device code of 11H.
10. CS1 and CS0 at active state

Table 8: Memory Array Detail

Memory Array	Sector Select	Byte Select	Nibble Select
Common Memory	A_{18} - A_8	A_7 - A_0	HB
Attribute Memory	A_9 - A_8	A_7 - A_0	HB

Table 9: Nonconforming Sector Map

Attribute Byte Address	D7	D6	D5	D4	D3	D2	D1	D0	Attribute Byte Address	D7	D6	D5	D4	D3	D2	D1	D0
200	X	X	X	X	SNS SUM [3:0]				**300**	X	X	X	X	SNS SUM [3:0]			
201	X	X	X	X	SNS SUM [7:4]				**301**	X	X	X	X	SNS SUM [7:4]			
202	X	X	X	X	16	14	12	10	**302**	X	X	X	X	17	15	13	11
203	X	X	X	X	1E	1C	1A	18	**303**	X	X	X	X	1F	1D	1B	19
.	X	X	X	X					**.**	X	X	X	X				
.	X	X	X	X					**.**	X	X	X	X				
.	X	X	X	X					**.**	X	X	X	X				
.	X	X	X	X					**.**	X	X	X	X				
2FE	X	X	X	X	7F6	7F4	7F2	7F0	**3FE**	X	X	X	X	7F7	7F5	7F3	7F1
2FF	X	X	X	X	7FE	7FC	7FA	7F8	**3FF**	X	X	X	X	7FF	7FD	7FB	7F9

Notes: The Attribute memory bit is “0” when the corresponding Common memory sector is nonconforming. The first 8 sectors of Common memory are always conforming.

Definitions:

1. The SNS sum is the sum of the number of nonconforming sectors and is calculated by summing the “0”s in the remaining bytes of the nonconforming sector map.
2. SNS Sum = Sum of Nonconforming Sector sum. The byte data from these addresses are not included in the sum.
   a) [3:0] = The lower nibble of the SNS sum.
   b) [7:4] = The higher nibble of the SNS sum.
3. Only the lower nibble is used in the attribute memory to map the location of the nonconforming sector(s).

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{CC} + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{CC} + 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 14.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) .....240°C
Output Short Circuit Current[1] ..... 100 mA

Note: [1] Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 10: Operating Range

Range	Ambient Temp	V_{CC}
Commercial	0 °C to +70 °C	3.0V to 3.6V

Table 11: AC Conditions of Test

Input Rise/Fall Time.....10 ns
Output Load.....1 TTL Gate and C_L = 100 pF
See Figures 16 and 17

Table 12: DC Operating Characteristics

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
I_{CC}	Power Supply Current				CE# (L or H) = OE# = V_{IL}, WE# = V_{IH}, all I/Os open
	Read		10	mA	Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min. V_{CC} = V_{CC} Max
	Program and Erase		25	mA	CE# (L or H) = WE# = V_{IL}, OE# = V_{IH} V_{CC} = V_{CC} Max.
I_{SB1}	Standby V_{CC} Current (TTL input)		1	mA	CE# = OE# = WE# = V_{IH}, V_{CC}=V_{CC} Max all Input pins at V_{IL} or V_{IH}
I_{SB2}	Standby V_{CC} Current (CMOS input)		20	µA	CE# = OE# = WE# = V_{CC} -0.3V, V_{CC}=V_{CC} Max, all Input pins at V_{IL2} or V_{IH2}
I_{LI}	Input Leakage Current		1	µA	V_{IN} = GND to V_{CC}, V_{CC} = V_{CC} Max.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}, V_{CC} = V_{CC} Max.
V_{IL}	Input Low Voltage, TTL		0.8	V	V_{CC} = V_{CC} Max.
V_{IH}	Input High Voltage, TTL	2.0		V	V_{CC} = V_{CC} Max.
V_{IL2}	Input Low Voltage, CMOS		0.2	V	V_{CC} = V_{CC} Max.
V_{IH2}	Input High Voltage, CMOS	$V_{CC-0.2}$		V	V_{CC} = V_{CC} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3.2 mA, V_{CC} = V_{CC} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2.0 mA, V_{CC} = V_{CC} Min.
V_H	Supervoltage for A_9	11.6	12.4	V	CE#=OE#=V_{IL}, WE#=V_{IH}
I_H	Supervoltage Current for A_9		200	µA	CE#=OE#=V_{IL}, WE#=V_{IH}, A_9 = V_H Max.

Table 13: Power-up Timings

Symbol	Parameter	Maximum	Units
$T_{PU-READ}$ (1)	Power-up to Read Operation	10	ms
$T_{PU-WRITE}$ (1)	Power-up to Write Operation	10	ms

Table 14: Capacitance (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$ (1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN} (1)	Input Capacitance	V_{IN} = 0v	6 pF

Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 15: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}	Endurance	100,000	Cycles	MIL-STD-883, Method 1033
T_{DR} (1)	Data Retention	100	Years	MIL-STD-883, Method 1008
V_{ZAP_HBM} (1)	ESD Susceptibility Human Body Model	1000	Volts	MIL-STD-883, Method 3015
V_{ZAP_MM} (1)	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH} (1)	Latch Up	100	mA	JEDEC Standard 17

Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC Characteristics

Table 16: Read Cycle Timing Parameters

PCMCIA Symbol	IEEE Symbol	Industry Symbol	Parameter	28LP040-250 Min	28LP040-250 Max	Units
tCR	tAVAV	T_{RC}	Read Cycle time	250		ns
ta(A)	tAVQV	T_{AA}	Address Access Time		250	ns
ta(CE)	tELQV	T_{CE}	Chip Enable Access Time		250	ns
ta(OE)	tGLQV	T_{OE}	Output Enable Access Time		100	ns
tdis(CE)	tEHQZ	T_{CLZ} (1)	CE# Low to Active Output	0		ns
tdis(OE)	tGHQZ	T_{OLZ} (1)	OE# Low to Active Output	0		ns
ten(CE)	tELQX	T_{CHZ} (1)	OE# High to High-Z Output		75	ns
ten(OE)	tGLQX	T_{OHZ} (1)	OE# High to High-Z Output		75	ns
tv(A)	tAXQX	T_{OH} (1)	Output Hold from Address Change	0		ns

Table 17: Erase/Program Cycle Timing Parameters

PCMCIA Symbol	IEEE Symbol	Industrial Symbol	Parameter	28LP040-250 Min	28LP040-250 Max	Units
tCW	tAVA	T_{BP}	Byte Program Cycle Time		35	µs
tw(WE)	tWLWH	T_{WP}	Write Pulse Width (WE#)	160		ns
tsu(A)	tAVWL	T_{AS}	Address Setup Time	20		ns
th(a)	tWLAX	T_{AH}	Address Hold Time	0		ns
tsu(CE)	tELWL	T_{CS}	CE# Setup Time	0		ns
th(CE)	tWHEX	T_{CH}	CE# Hold Time	0		ns
tsu(OE-WE)	tGHWL	T_{OES}	OE# High Setup Time	20		ns
th(OE-WE)	tWGL	T_{OEH}	OE# High Hold Time	20		ns
tw(CE)	tWLEH	T_{CP}	Write Pulse Width (CE#)	160		ns
tsu(D-WEH)	tDVWH	T_{DS}	Data Setup Time	120		ns
th(D)	tWHDX	T_{DH}	Data Hold Time	20		ns
	tWHWL2	T_{SE}	Sector Erase Cycle Time		2	ms
		T_{RST} (1)	Reset Command Recovery Time		4	µs
		T_{EVD}	Erase Verify Timing Delay	.025		µs
		T_{ERD}	Erase Reset Timing Delay	4		µs
		T_{ASE}	Algorithmic Sector Erase Cycle Time	0.04	2.56	ms
	tEHEL	T_{CPH}	CE# High Pulse Width	50		ns
	tWHWL1	T_{WPH}	WE# High Pulse Width	50		ns
	tRHRL	T_{HR} (1)	Hardware Reset Pulse Width	10		µs
	tRHBL	T_{RBS} (1)	Hardware Reset High to RDY/BSY# Active	10		µs
		T_{PCP} (1)	Protect Chip Enable Pulse Width	20		ns
		T_{PCH} (1)	Protect Chip Enable High Time	20		ns
		T_{PAS} (1)	Protect Address Setup Time	0		ns
		T_{PAH} (1)	Protect Address Hold Time	100		ns

Note: (1)This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

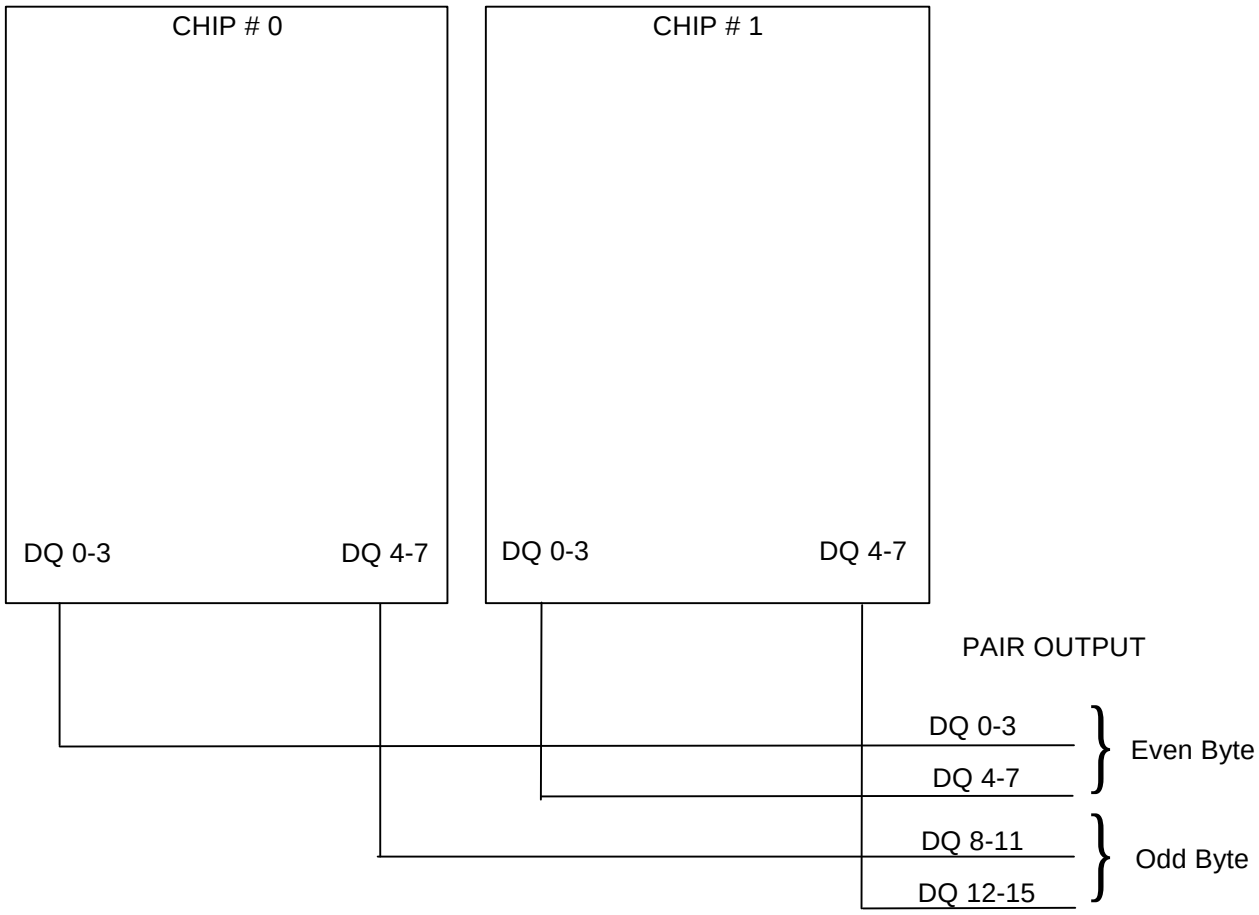


Figure 3: Chip Pair Mapping (Nibble Access)

Table 18: Nibble Access Table

Byte	Nibble	Outputs	CEL#	CEH#	HB
Even	Even Nibble	0-3	L	H	L
Even	Odd Nibble	4-7	L	H	H
Odd	Even Nibble	8-11	H	L	L
Odd	Odd Nibble	12-15	H	L	H

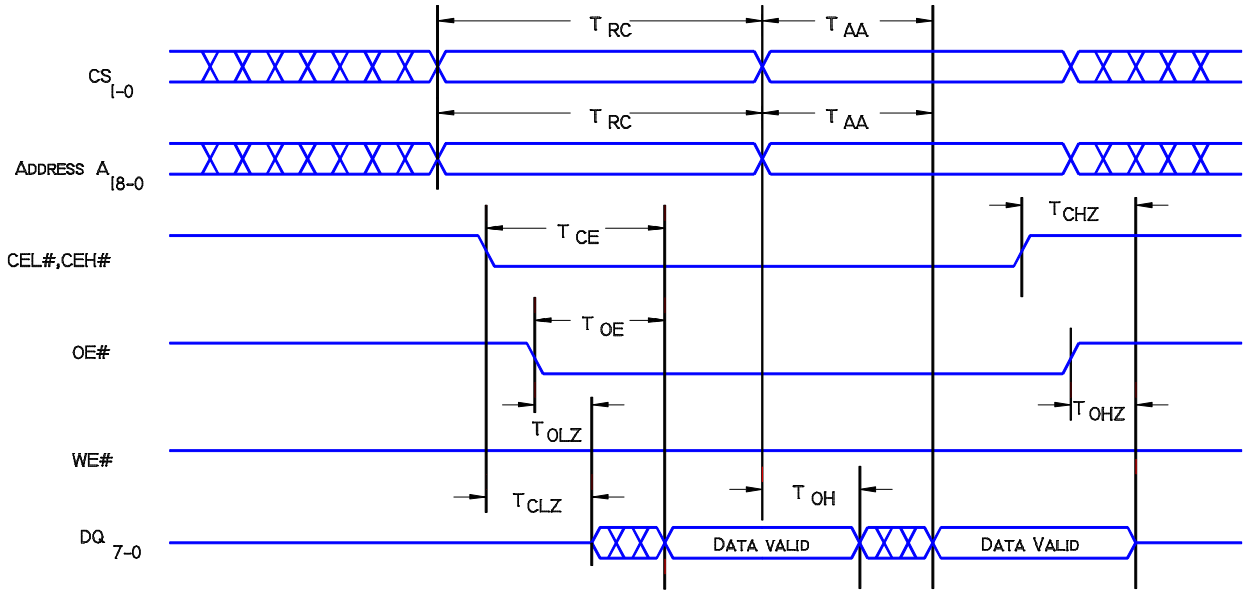


Figure 4: Read Cycle Timing Diagram

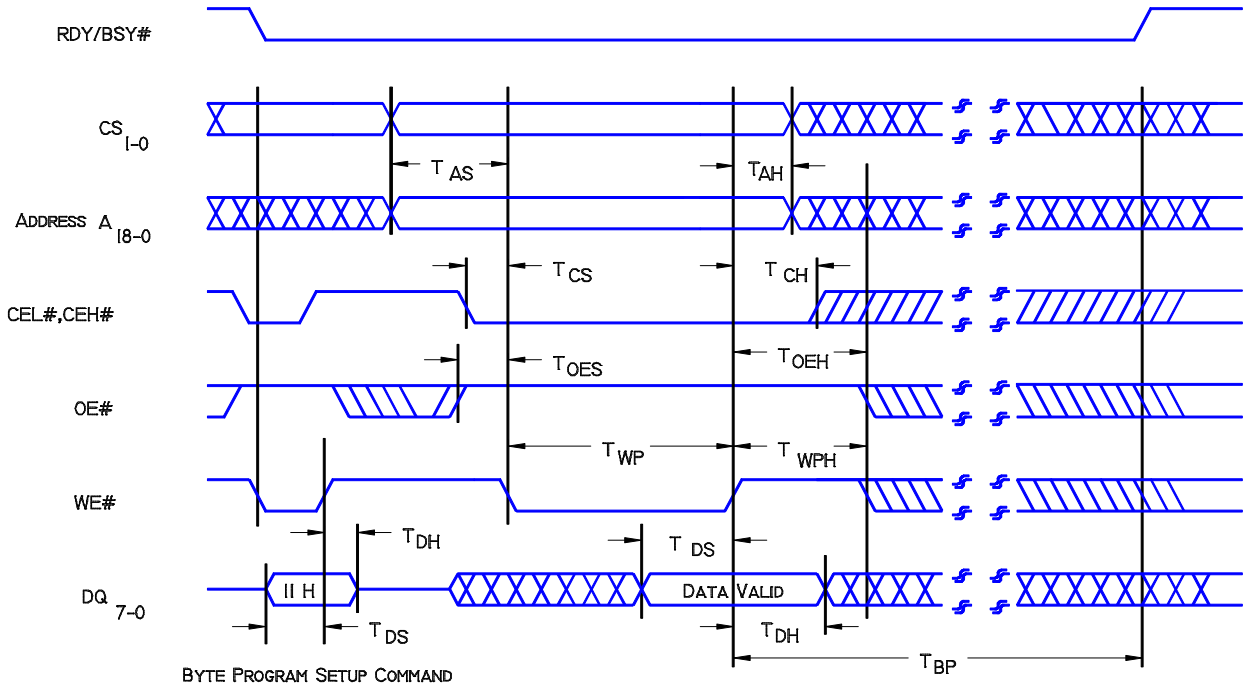


Figure 5: WE# Controlled Byte Program Timing Diagram

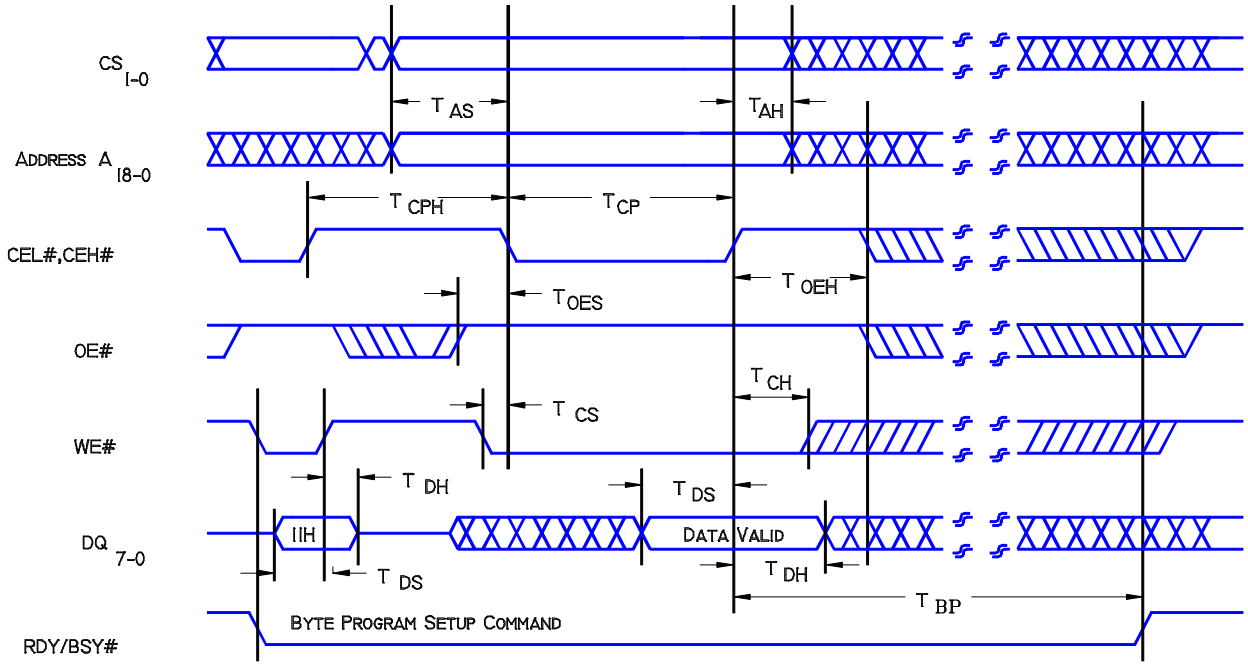


Figure 6: CE# Controlled Byte Program Timing Diagram

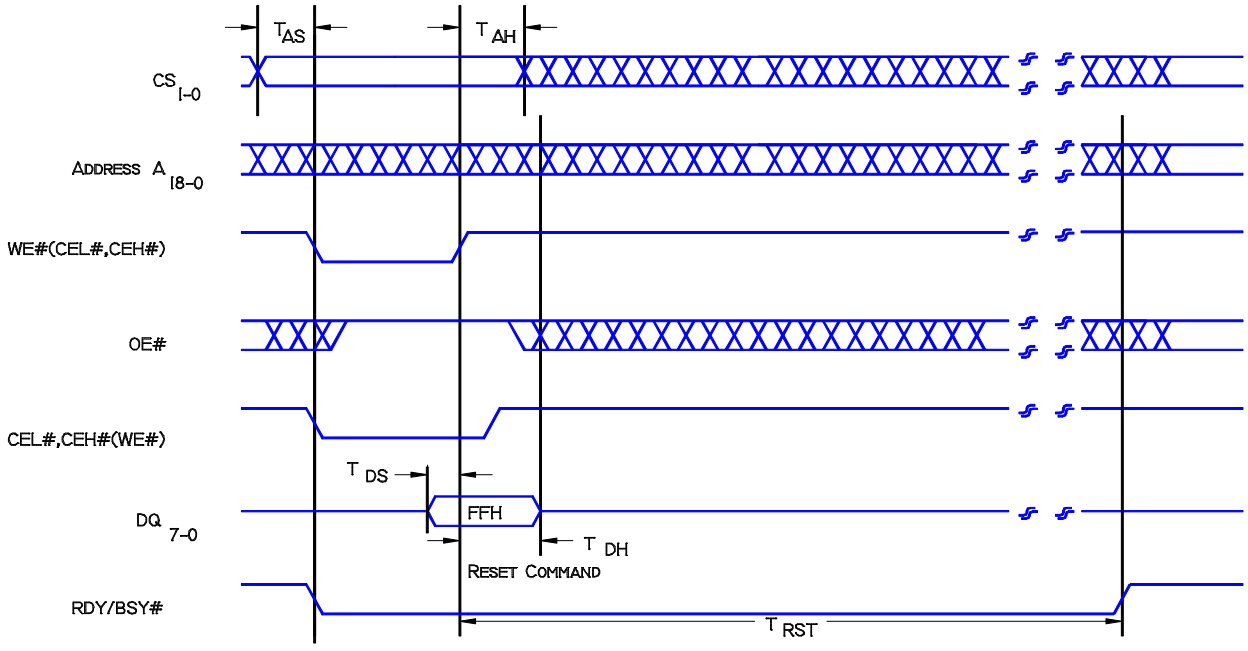


Figure 7: Reset Command Timing Diagram

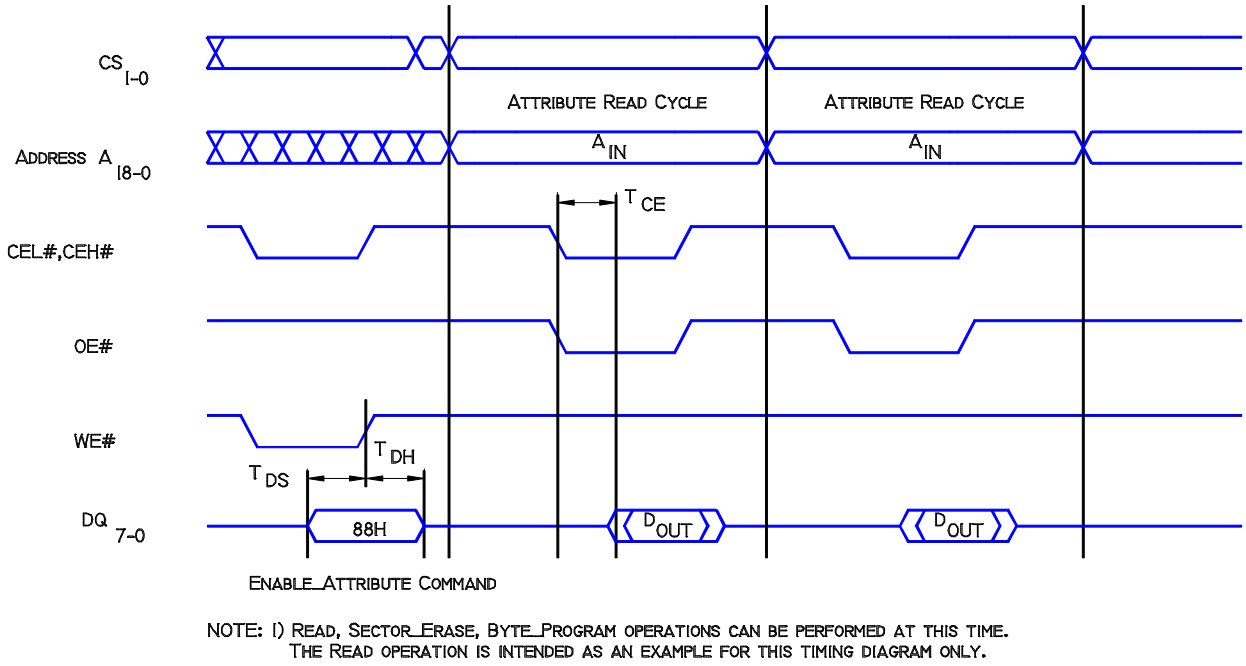


Figure 8: Enable_Attribute Timing Diagram

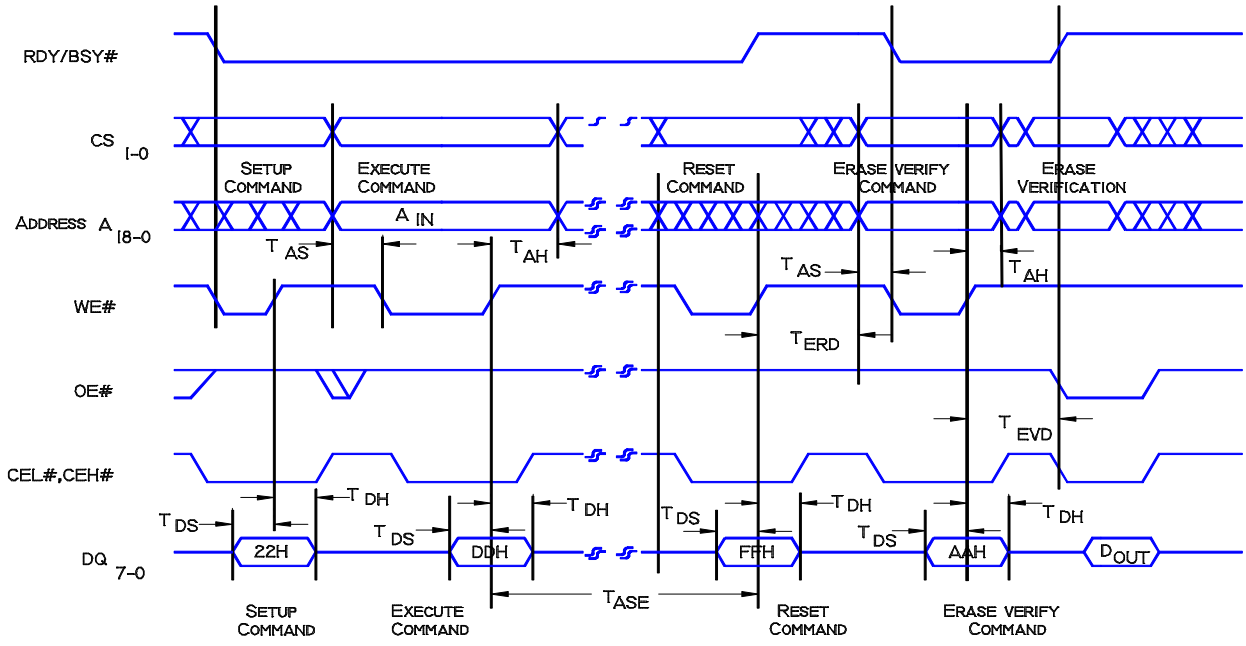
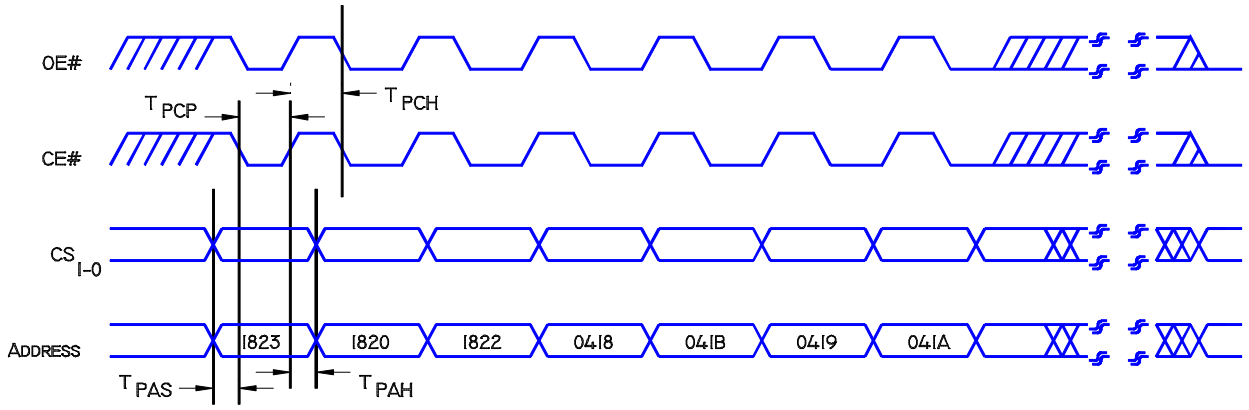


Figure 9: Sector Erase Timing Diagram



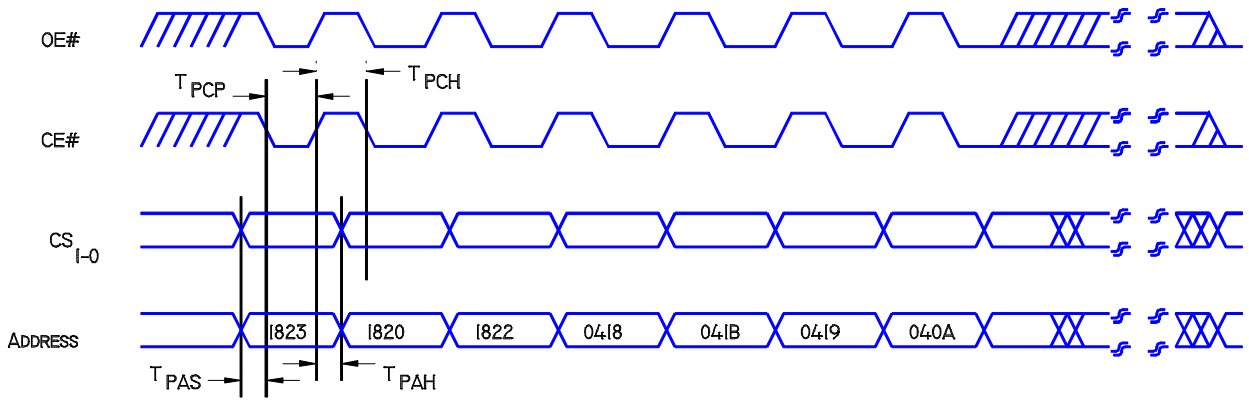
NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 10: Software Data Unprotect Timing Diagram



NOTE : A. ADDRESSES ARE LATCHED INTERNALLY ON THE RISING EDGE OF:

1. OE# IF CE# IS KEPT AT LOW ALL TIME.
2. CE# IF OE# IS KEPT AT LOW ALL TIME.
3. THE FIRST PIN TO GO HIGH IF BOTH ARE TOGGLED.

B. ABOVE ADDRESS VALUES ARE IN HEX.

C. ADDRESSES > A_{12} ARE "DON'T CARE"

Figure 11: Software Data Protect Timing Diagram

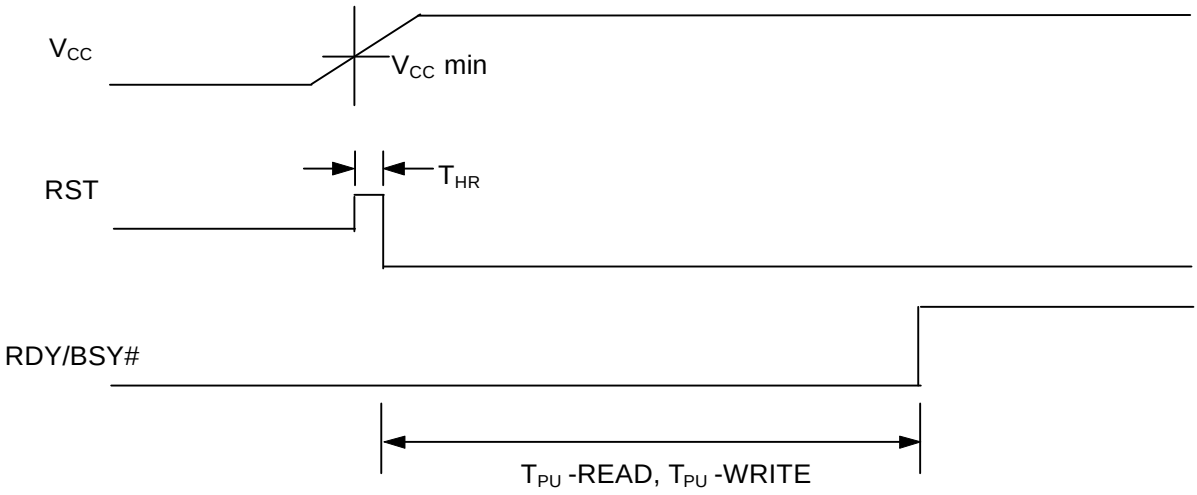


Figure 12: RST and RDY/BSY# waveforms - Power up to Read and Write

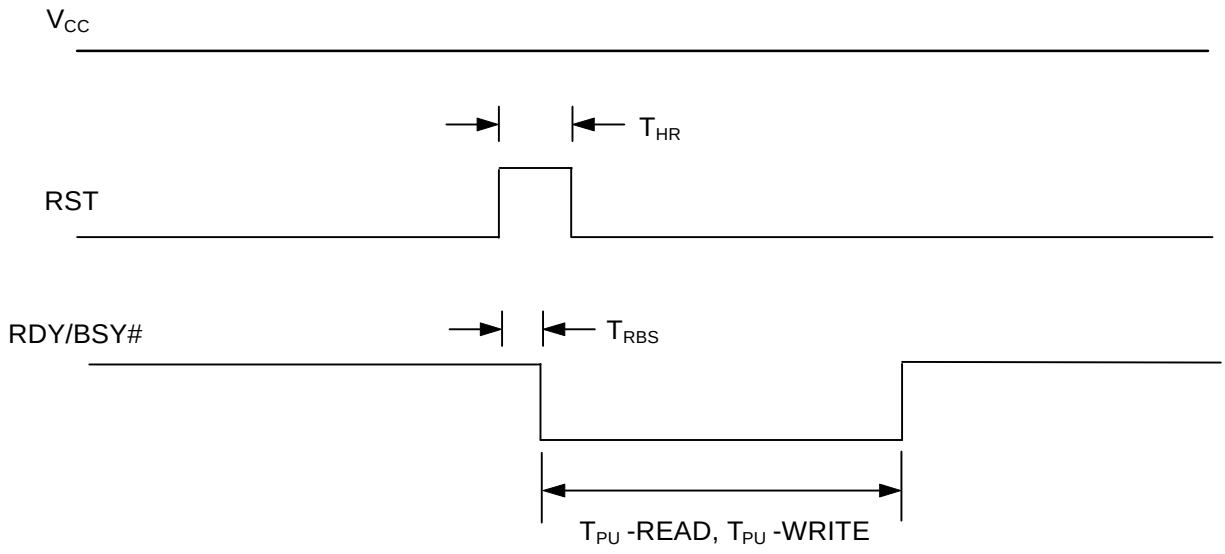


Figure 13: RST and RDY/BSY# waveforms - Hardware Reset

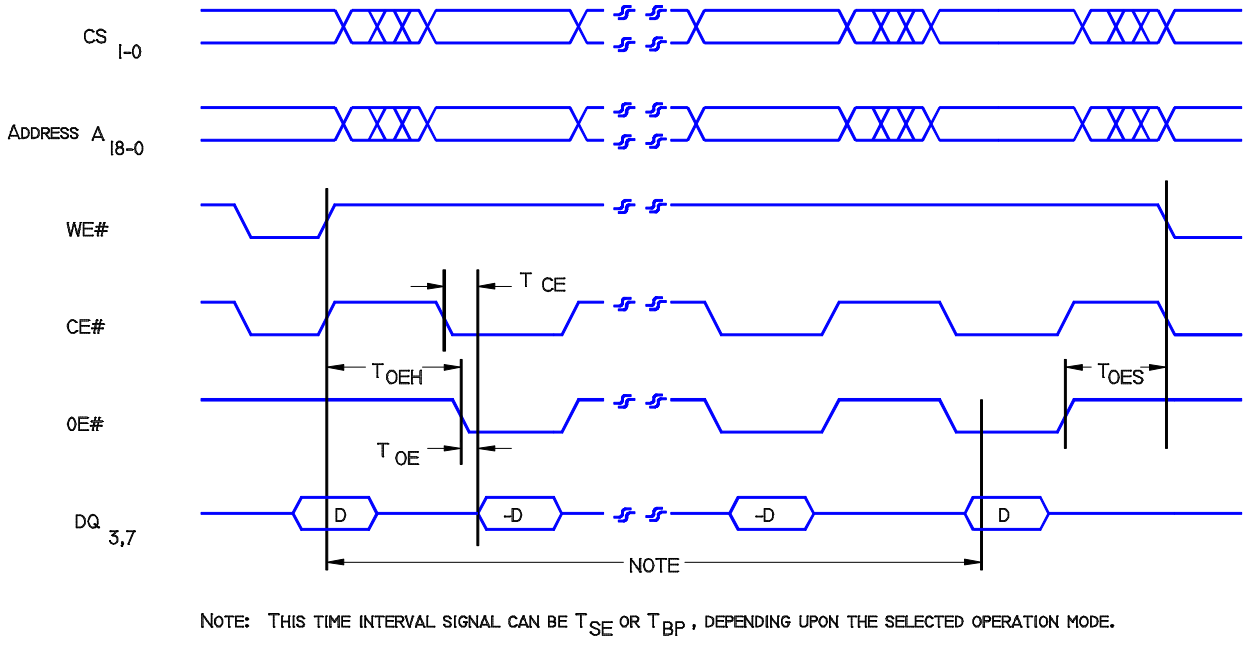


Figure 14: Data# Polling Timing Diagram

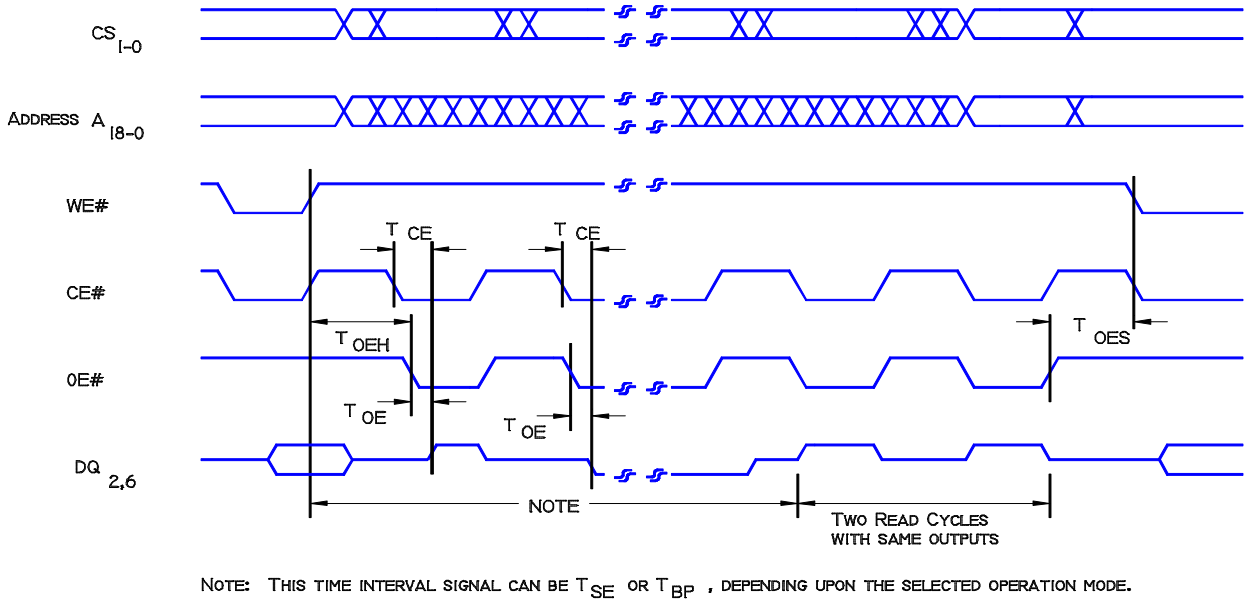
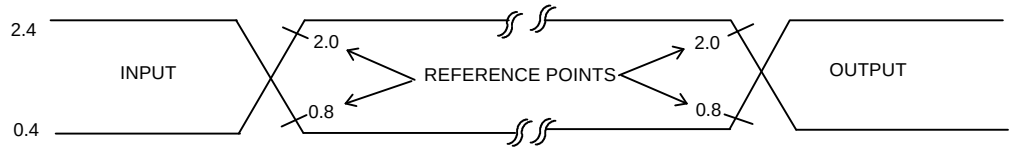


Figure 15: Toggle Bit Timing Diagram



AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.4 V_{TTL}) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Inputs rise and fall times (10% ↔ 90%) are <10 ns.

Figure 16: AC Input/Output Reference Waveform

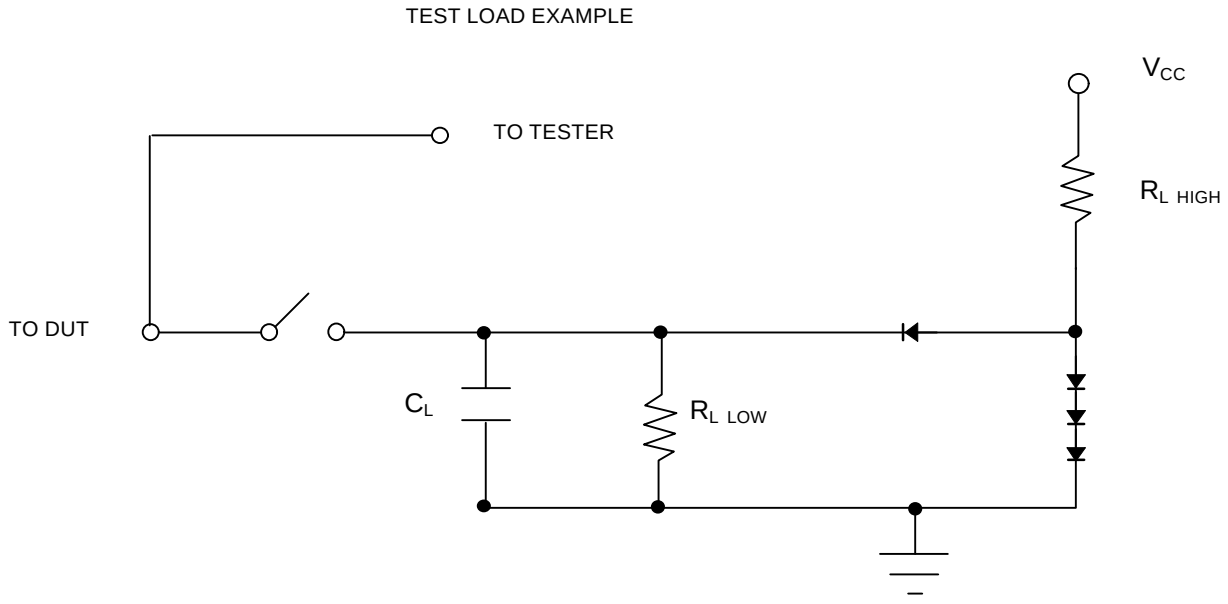


Figure 17: Test Load Example

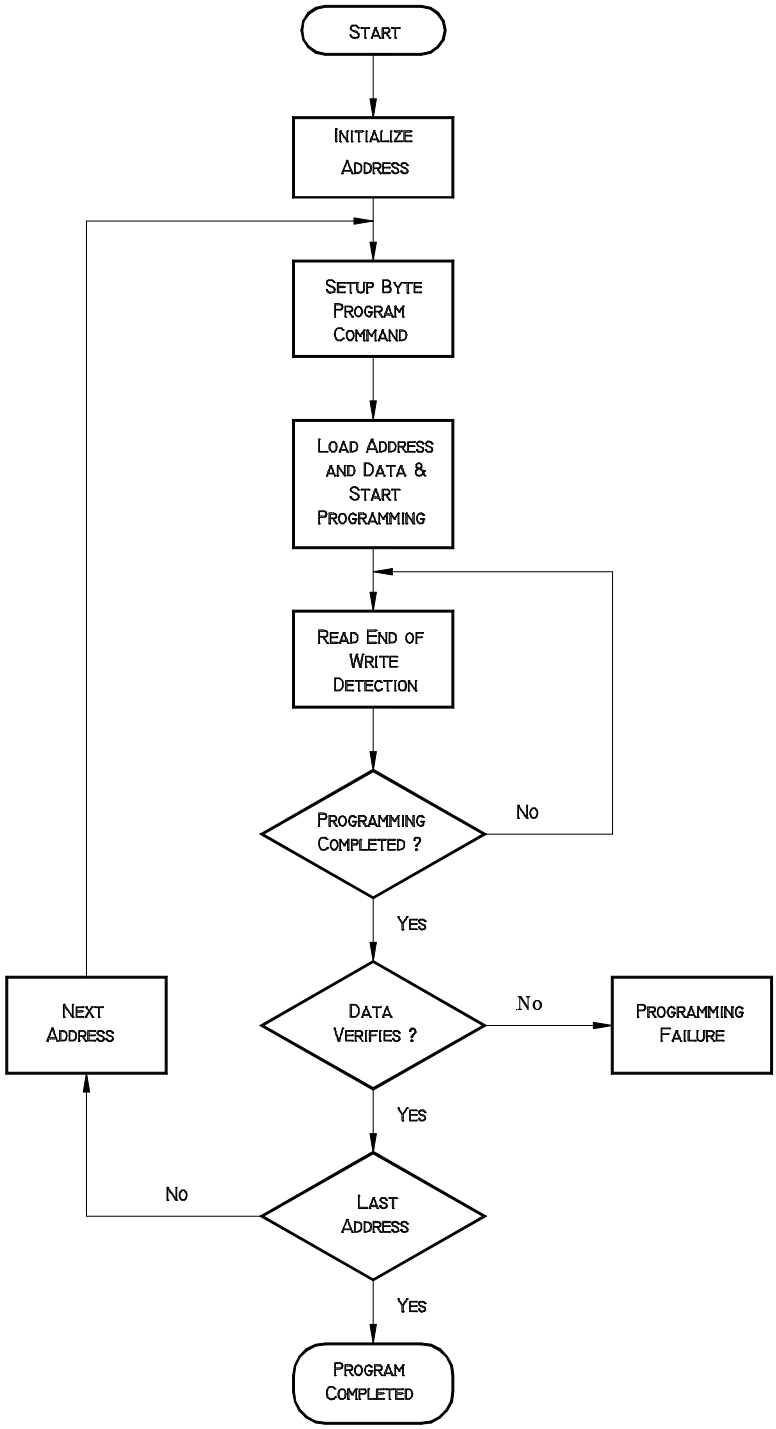


Figure 18: Byte Program Flowchart

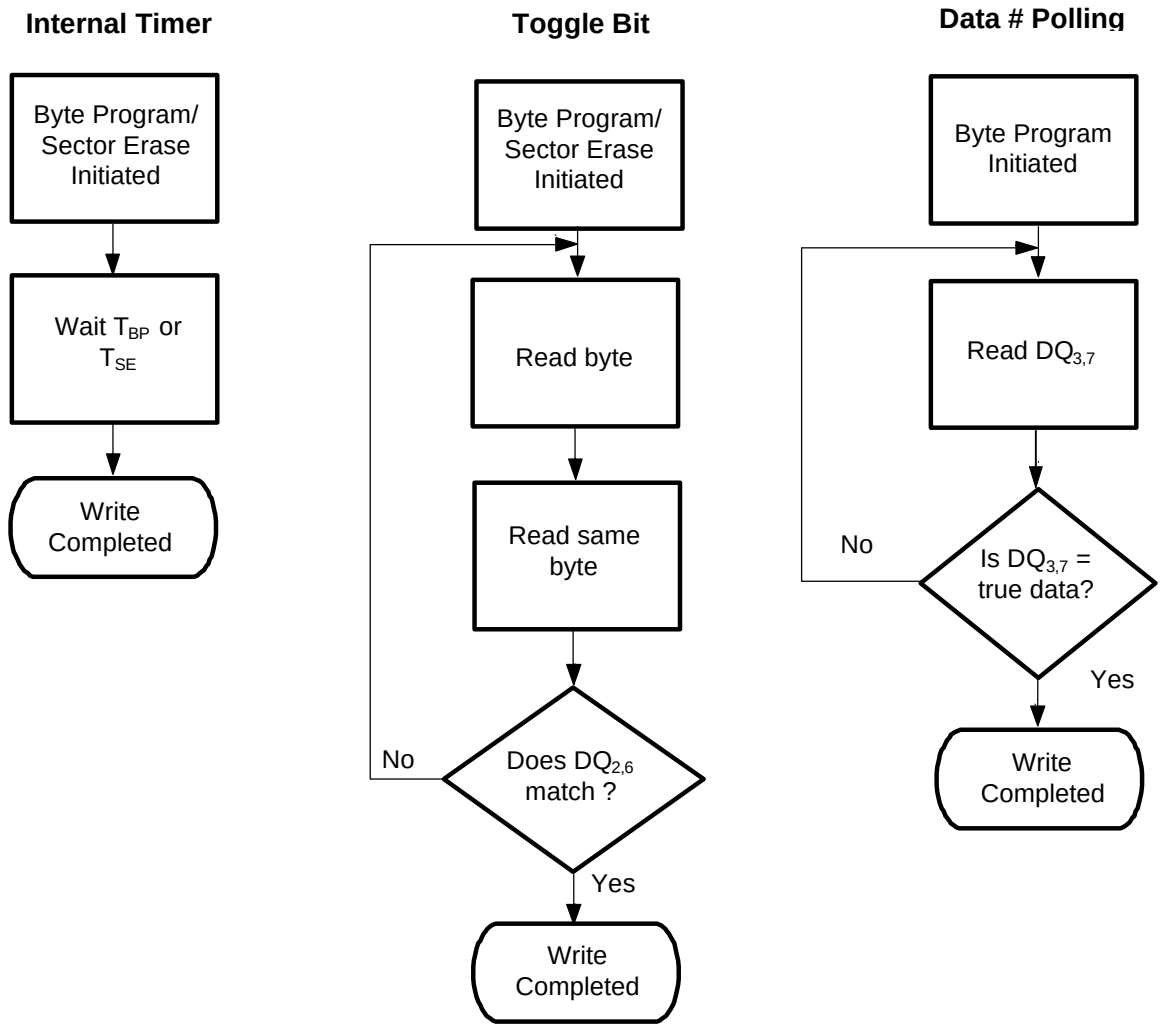


Figure 19: Write Wait Options

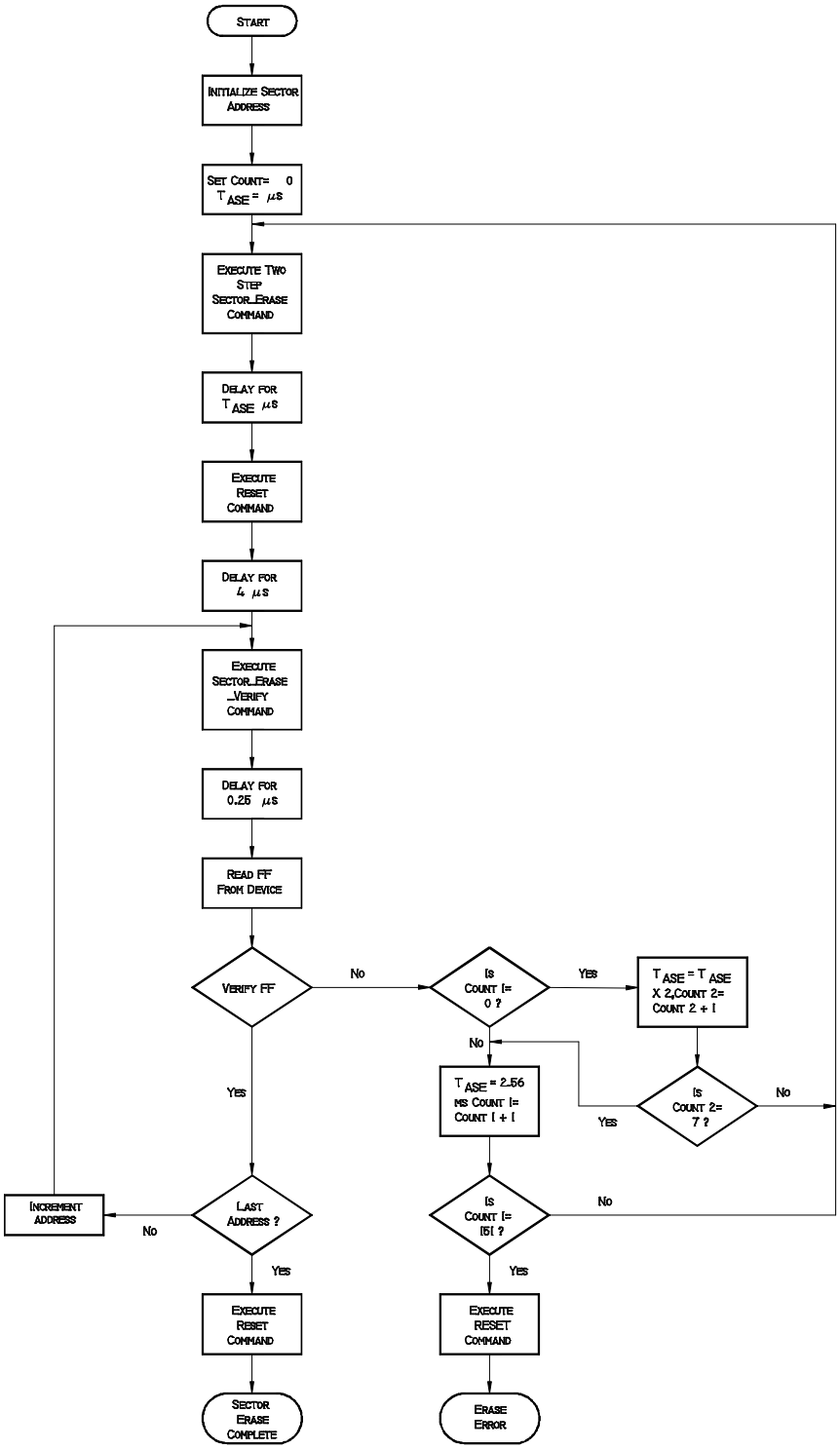


Figure 20: Sector_Erase Flowchart

Product Ordering Information

Device **Speed** **Suffix1** **Suffix2** **Suffix3**

SST28LP040 - XXX - XX - XX XXXX

Card Decode
S00A = CS1 low active
CS0 low active
S01B = CS1 low active
CS0 high active
S10C = CS1 high active
CS0 low active
S11D = CS1 high active
CS0 high active

Package Modifier
I = 40 leads

Package Type
W = TSOP (die up)

Operating Temperature
C = Commercial = 0° to 70°C

Minimum Endurance
5 = 100,000 cycles

Read Access Speed
250 = 250 ns
150 = 150 ns

Valid combinations

SST28LP040-250-5C-WI-S00A SST28LP040-250-5C-WI-S01B

SST28LP040-250-5C-WI-S10C SST28LP040-250-5C-WI-S11D

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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