

ST730C..L SERIES

PHASE CONTROL THYRISTORS

Hockey Puk Version

Features

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AC (B-PUK)

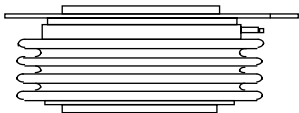
Typical Applications

- DC motor controls
- Controlled DC power supplies
- AC controllers

Major Ratings and Characteristics

Parameters	ST730C..L	Units
$I_{T(AV)}$	990	A
@ T_{hs}	55	°C
$I_{T(RMS)}$	2000	A
@ T_{hs}	25	°C
I_{TSM}	@ 50Hz	17800 A
	@ 60Hz	18700 A
I^2t	@ 50Hz	1591 KA ² s
	@ 60Hz	1452 KA ² s
V_{DRM}/V_{RRM}	800 to 1800	V
t_q typical	150	μs
T_J	- 40 to 125	°C

990A



case style TO-200AC (B-PUK)

ST730C..L Series

Bulletin I25191 rev. C 04/00

International
IR Rectifier**ELECTRICAL SPECIFICATIONS****Voltage Ratings**

Type number	Voltage Code	V_{DRM}/V_{RRM} , max. repetitive peak and off-state voltage V	V_{RSM} , maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = T_J \text{ max}$ mA
ST730C..L	08	800	900	80
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	
	18	1800	1900	

On-state Conduction

Parameter	ST730C..L	Units	Conditions
$I_{T(AV)}$ Max. average on-state current @ Heatsink temperature	990 (375) 55 (85)	A °C	180° conduction, half sine wave double side (single side) cooled
$I_{T(RMS)}$ Max. RMS on-state current	2000	A	DC @ 25°C heatsink temperature double side cooled
I_{TSM} Max. peak, one-cycle non-repetitive surge current	17800		t = 10ms No voltage
	18700		t = 8.3ms reapplied
	15000		t = 10ms 100% V_{RRM}
	15700		t = 8.3ms reapplied
I^2t Maximum I^2t for fusing	1591	KA ² s	t = 10ms No voltage
	1452		t = 8.3ms reapplied
	1125		t = 10ms 100% V_{RRM}
	1027		t = 8.3ms reapplied
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	15910	KA ² √s	t = 0.1 to 10ms, no voltage reapplied
$V_{T(TO)1}$ Low level value of threshold voltage	0.98	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}), T_J = T_J \text{ max.}$
$V_{T(TO)2}$ High level value of threshold voltage	1.12		$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ max.}$
r_{t1} Low level value of on-state slope resistance	0.32	mΩ	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)}), T_J = T_J \text{ max.}$
r_{t2} High level value of on-state slope resistance	0.27		$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ max.}$
V_{TM} Max. on-state voltage	1.62	V	$I_{pk} = 2000A, T_J = T_J \text{ max, } t_p = 10ms \text{ sine pulse}$
I_H Maximum holding current	600	mA	$T_J = 25^\circ C$, anode supply 12V resistive load
I_L Typical latching current	1000		

Switching

Parameter	ST730C..L	Units	Conditions
di/dt Max. non-repetitive rate of rise of turned-on current	1000	A/μs	Gate drive 20V, 20Ω, $t_i \leq 1\mu s$ $T_J = T_J \text{ max, anode voltage} \leq 80\% V_{DRM}$
t_d Typical delay time	1.0	μs	Gate current 1A, $di_g/dt = 1A/\mu s$ $V_d = 0.67\% V_{DRM}, T_J = 25^\circ C$
t_q Typical turn-off time	150		$I_{TM} = 750A, T_J = T_J \text{ max, } di/dt = 60A/\mu s, V_R = 50V$ $dv/dt = 20V/\mu s, \text{ Gate } 0V \text{ } 100\Omega, t_p = 500\mu s$

Blocking

Parameter	ST730C..L	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	500	V/ μ s	$T_J = T_J \text{ max. linear to } 80\% \text{ rated } V_{\text{DRM}}$
I_{DRM} I_{RRM} Max. peak reverse and off-state leakage current	80	mA	$T_J = T_J \text{ max, rated } V_{\text{DRM}}/V_{\text{RRM}} \text{ applied}$

Triggering

Parameter	ST730C..L		Units	Conditions
P_{GM} Maximum peak gate power	10.0		W	$T_J = T_J \text{ max, } t_p \leq 5\text{ms}$
$P_{\text{G(AV)}}$ Maximum average gate power	2.0			$T_J = T_J \text{ max, } f = 50\text{Hz, } d\% = 50$
I_{GM} Max. peak positive gate current	3.0		A	$T_J = T_J \text{ max, } t_p \leq 5\text{ms}$
$+V_{\text{GM}}$ Maximum peak positive gate voltage	20		V	$T_J = T_J \text{ max, } t_p \leq 5\text{ms}$
$-V_{\text{GM}}$ Maximum peak negative gate voltage	5.0			
I_{GT} DC gate current required to trigger	TYP.	MAX.	mA	$T_J = -40^\circ\text{C}$ $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ Max. required gate trigger/ current/ voltage are the lowest value which will trigger all units 12V anode-to-cathode applied
	200	-		
	100	200		
	50	-		
V_{GT} DC gate voltage required to trigger	2.5	-	V	$T_J = -40^\circ\text{C}$ $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
	1.8	3.0		
	1.1	-		
I_{GD} DC gate current not to trigger	10		mA	$T_J = T_J \text{ max}$ Max. gate current/voltage not to trigger is the max. value which will not trigger any unit with rated V_{DRM} anode-to-cathode applied
V_{GD} DC gate voltage not to trigger	0.25		V	

Thermal and Mechanical Specification

Parameter	ST730C..L	Units	Conditions
T_J Max. operating temperature range	-40 to 125	$^\circ\text{C}$	
T_{stg} Max. storage temperature range	-40 to 150		
$R_{\text{thJ-hs}}$ Max. thermal resistance, junction to heatsink	0.073 0.031	K/W	DC operation single side cooled DC operation double side cooled
$R_{\text{thC-hs}}$ Max. thermal resistance, case to heatsink	0.011 0.006	K/W	DC operation single side cooled DC operation double side cooled
F Mounting force, $\pm 10\%$	14700 (1500)	N (Kg)	
wt Approximate weight	255	g	
Case style	TO - 200AC (B-PUK)		See Outline Table

ST730C..L Series

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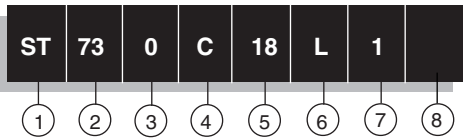
ΔR_{thJ-hs} Conduction

(The following table shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction		Rectangular conduction		Units	Conditions
	Single Side	Double Side	Single Side	Double Side		
180°	0.009	0.009	0.006	0.006	K/W	$T_J = T_{J \text{ max.}}$
120°	0.011	0.011	0.010	0.011		
90°	0.014	0.014	0.015	0.015		
60°	0.020	0.020	0.021	0.021		
30°	0.036	0.036	0.036	0.036		

Ordering Information Table

Device Code



- 1** - Thyristor
- 2** - Essential part number
- 3** - 0 = Converter grade
- 4** - C = Ceramic Puk
- 5** - Voltage code: Code x 100 = V_{RRM} (See Voltage Rating Table)
- 6** - L = Puk Case TO-200AC (B-PUK)
- 7** - 0 = Eyelet terminals (Gate and Auxiliary Cathode Unsoldered Leads)
1 = Fast-on terminals (Gate and Auxiliary Cathode Unsoldered Leads)
2 = Eyelet terminals (Gate and Auxiliary Cathode Soldered Leads)
3 = Fast-on terminals (Gate and Auxiliary Cathode Soldered Leads)
- 8** - Critical dv/dt: None = 500V/ μ sec (Standard selection)
L = 1000V/ μ sec (Special selection)

Outline Table

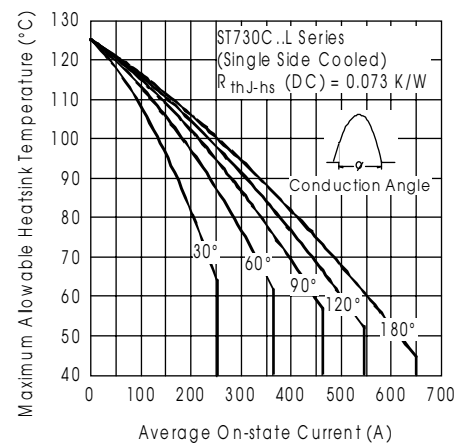
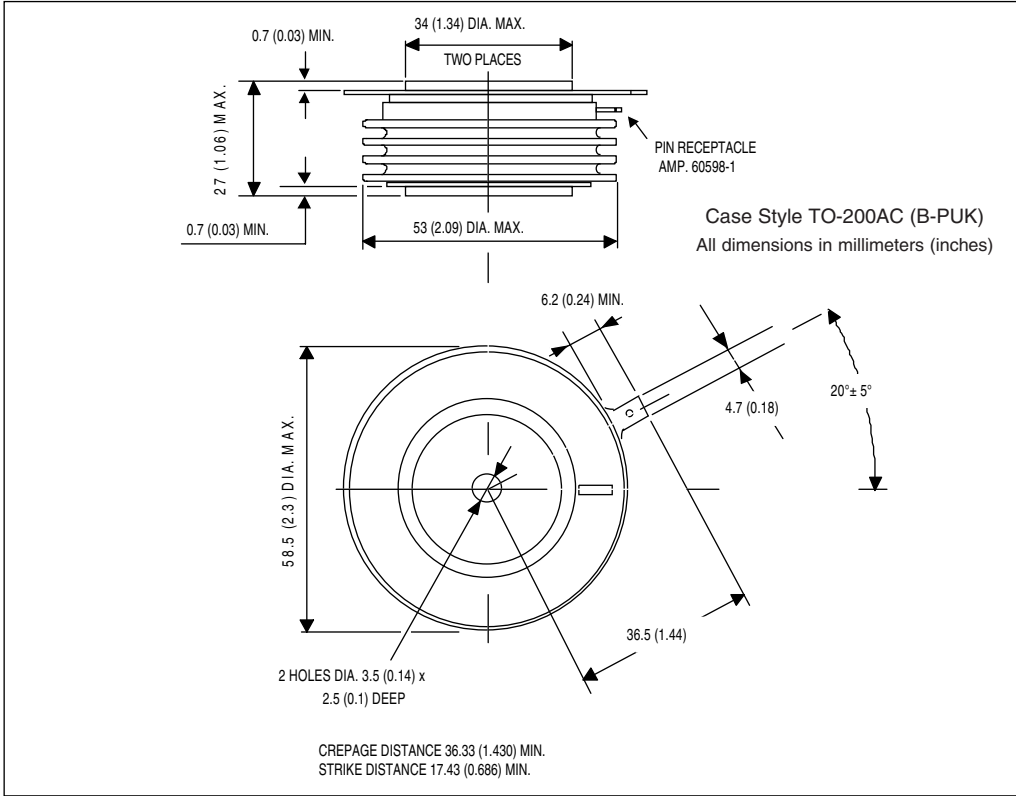


Fig. 1 - Current Ratings Characteristics

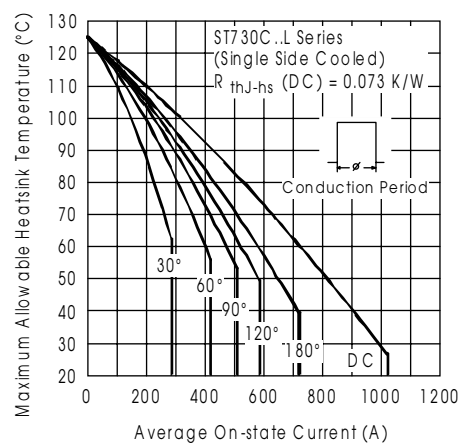


Fig. 2 - Current Ratings Characteristics

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International
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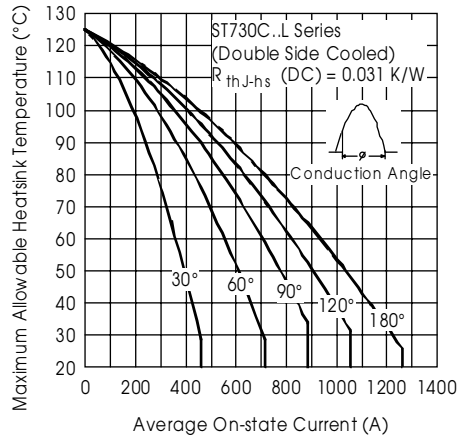


Fig. 3 - Current Ratings Characteristics

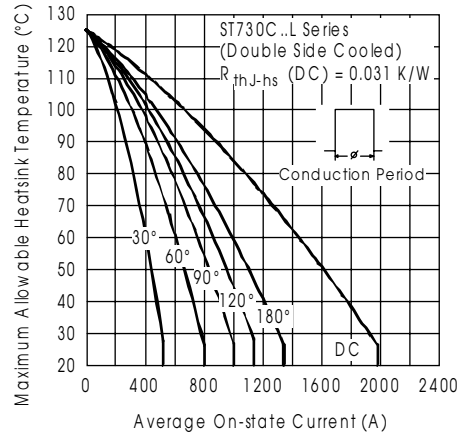


Fig. 4 - Current Ratings Characteristics

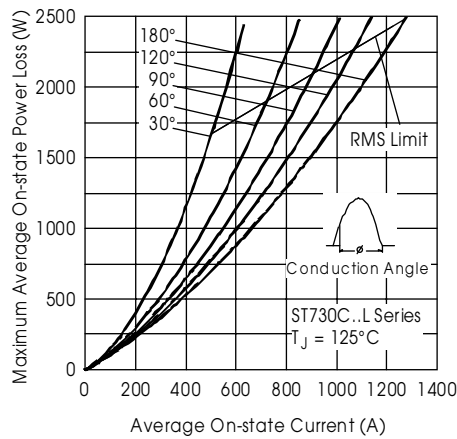


Fig. 5 - On-state Power Loss Characteristics

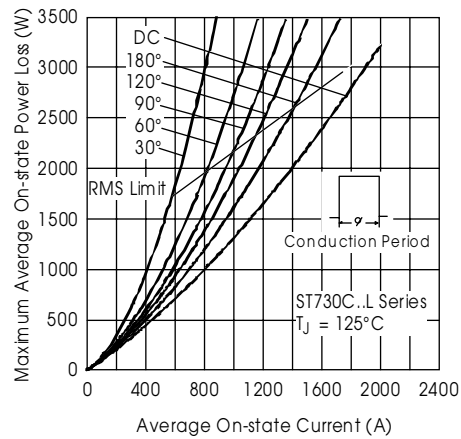


Fig. 6 - On-state Power Loss Characteristics

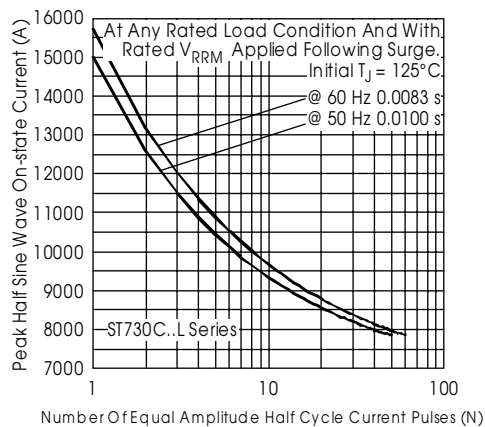


Fig. 7 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

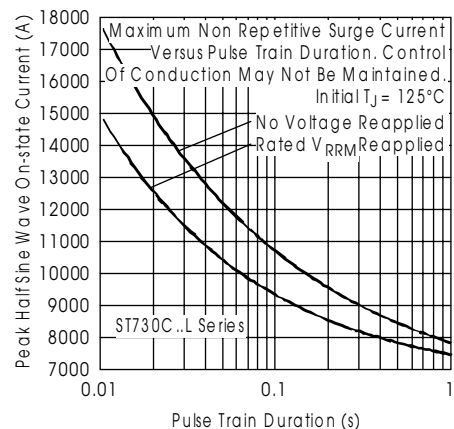


Fig. 8 - Maximum Non-Repetitive Surge Current
Single and Double Side Cooled

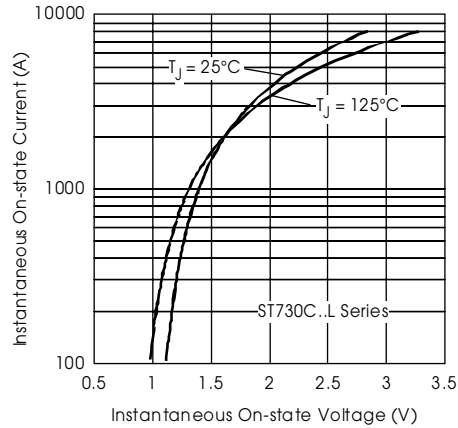


Fig. 9 - On-state Voltage Drop Characteristics

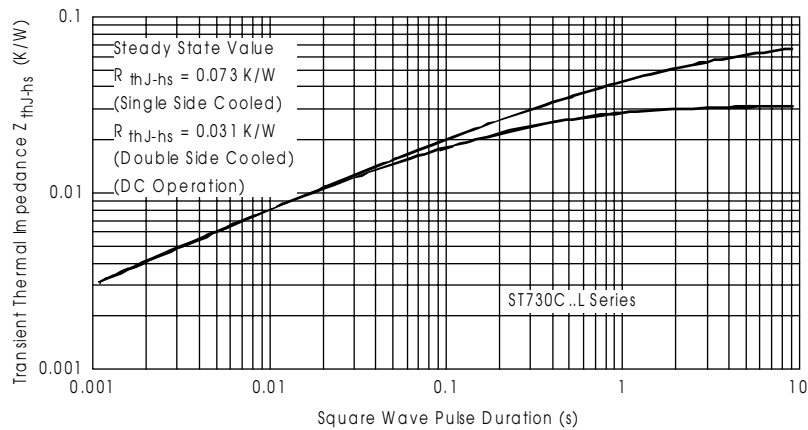


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

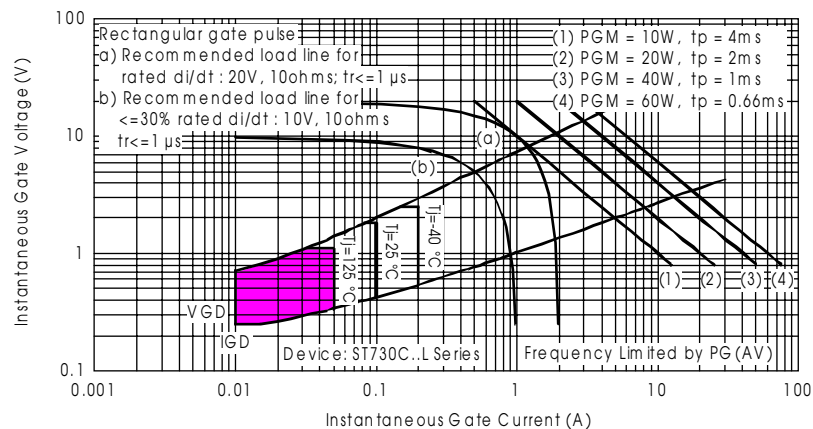


Fig. 11 - Gate Characteristics