

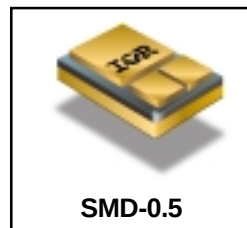
RADIATION HARDENED POWER MOSFET

SURFACE MOUNT (SMD-0.5) RAD Hard™ HEXFET® TECHNOLOGY

**IRHNJ7330SE
JANSR2N7465U3
400V, N-CHANNEL
REF: MIL-PRF-19500/676**

Product Summary

Part Number	Radiation Level	RDS(on)	ID	QPL Part Number
IRHNJ7330SE	100K Rads (Si)	1.2Ω	5.3A	JANSR2N7465U3



SMD-0.5

International Rectifier's RADHard™ HEXFET® MOSFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
ID @ VGS = 12V, TC = 25°C	Continuous Drain Current	5.3	A
ID @ VGS = 12V, TC = 100°C	Continuous Drain Current	3.4	
IDM	Pulsed Drain Current ①	21	
PD @ TC = 25°C	Max. Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	150	mJ
IAR	Avalanche Current ①	5.3	A
EAR	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.8	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	1.0(Typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	400	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _j	Temperature Coefficient of Breakdown Voltage	—	0.48	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	1.2	Ω	V _{GS} = 12V, I _D = 3.4A ④
V _{GS(th)}	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
g _{fs}	Forward Transconductance	1.3	—	—	S (r)	V _{DS} > 15V, I _{DS} = 3.4A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	50	μA	V _{DS} = 320V, V _{GS} = 0V
		—	—	250		V _{DS} = 320V, V _{GS} = 0V, T _j = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	41	nC	V _{GS} = 12V, I _D = 5.3A V _{DS} = 200V
Q _{gs}	Gate-to-Source Charge	—	—	7.0		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	20		
t _{d(on)}	Turn-On Delay Time	—	—	25	ns	V _{DD} = 200V, I _D = 5.3A, V _{GS} = 12V, V _{RG} = 7.5Ω
t _r	Rise Time	—	—	75		
t _{d(off)}	Turn-Off Delay Time	—	—	58		
t _f	Fall Time	—	—	58		
L _S + L _D	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	600	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	165	—		
C _{rss}	Reverse Transfer Capacitance	—	60	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	5.3	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	21		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 5.2A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	516	nS	T _J = 25°C, I _F = 5.2A, di/dt ≤ 100A/μs V _{DD} ≤ 50V ④
Q _{RR}	Reverse Recovery Charge	—	—	3.8	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	1.67	°C/W	
R _{thJ-PCB}	Junction-to-PC board	—	6.9	—		soldered to a 2" square copper-clad board

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads (Si)		Units	Test Conditions ⑧
		Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	400	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.5		V _{GS} = V _{DS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100		V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	50	μA	V _{DS} =320V, V _{GS} =0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	1.22	Ω	V _{GS} = 12V, I _D = 3.4A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (SMD-0.5)	—	1.2	Ω	V _{GS} = 12V, I _D = 3.4A
V _{SD}	Diode Forward Voltage ④	—	1.2	V	V _{GS} = 0V, I _D = 5.3A

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V _{DS} (V)			
				@V _{GS} =0V	@V _{GS} =-5V	@V _{GS} =-10V	@V _{GS} =-15V
Cu	28	285	43	325	325	325	325
Br	36.8	305	39	325	325	325	275

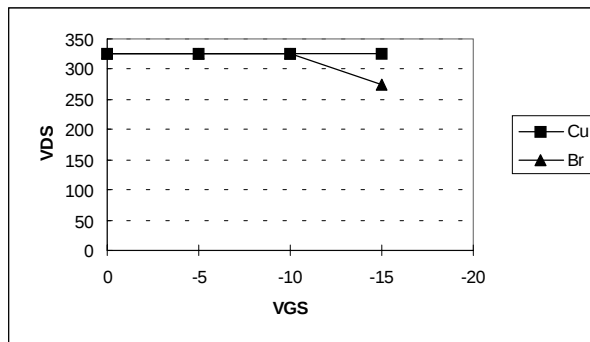


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

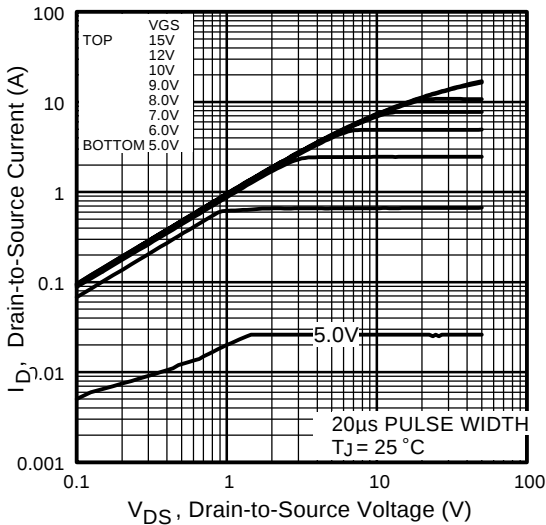


Fig 1. Typical Output Characteristics

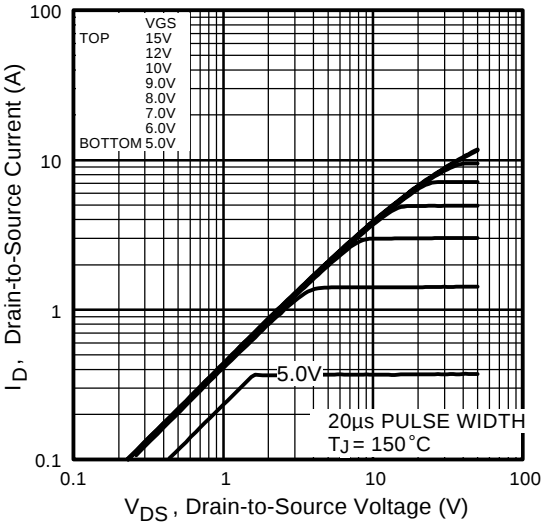


Fig 2. Typical Output Characteristics

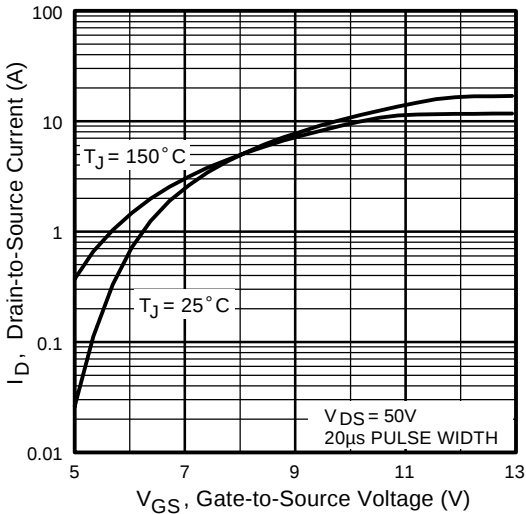


Fig 3. Typical Transfer Characteristics

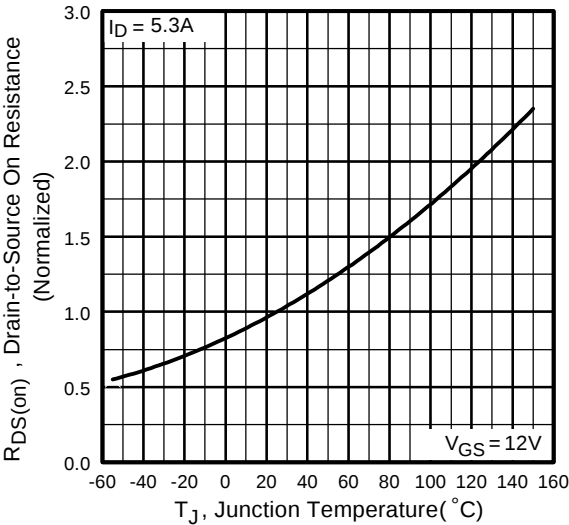


Fig 4. Normalized On-Resistance Vs. Temperature

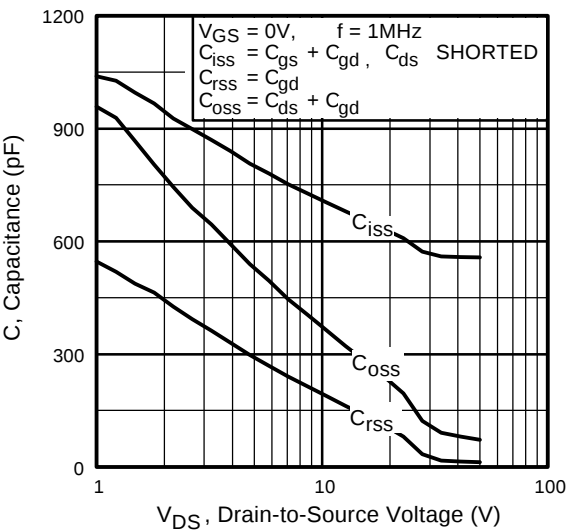


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

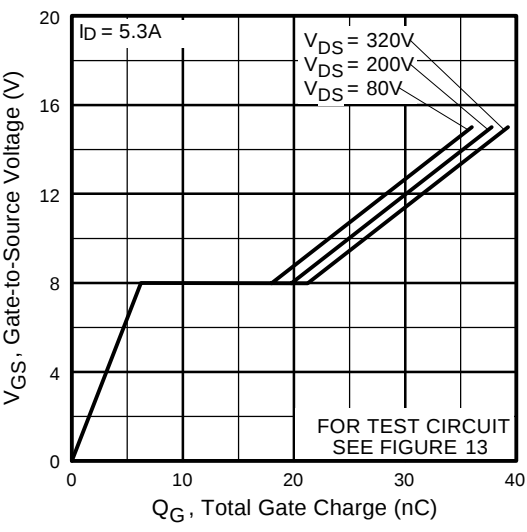


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

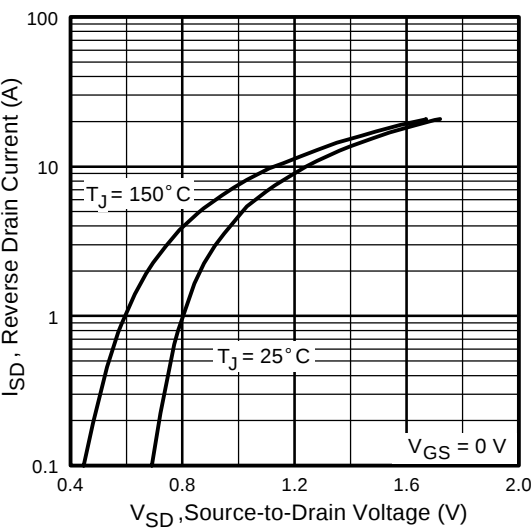


Fig 7. Typical Source-Drain Diode Forward Voltage

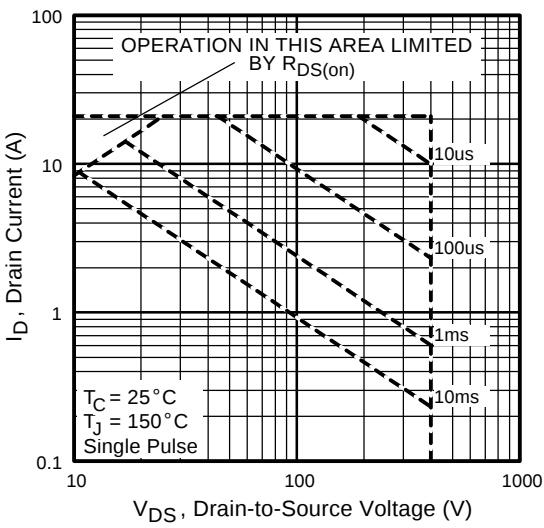


Fig 8. Maximum Safe Operating Area

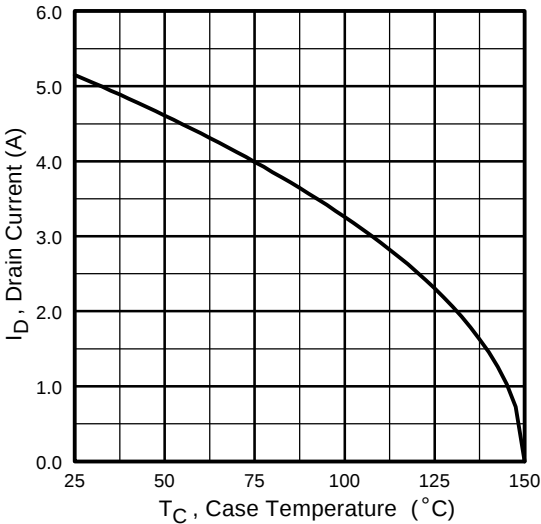


Fig 9. Maximum Drain Current Vs. Case Temperature

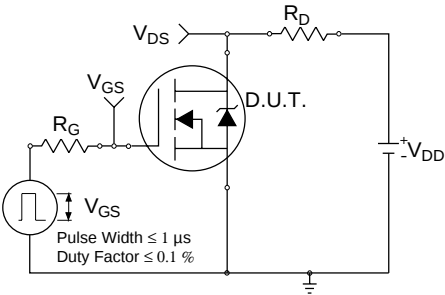


Fig 10a. Switching Time Test Circuit

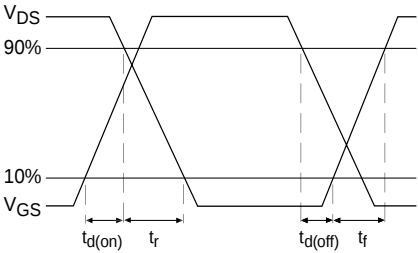


Fig 10b. Switching Time Waveforms

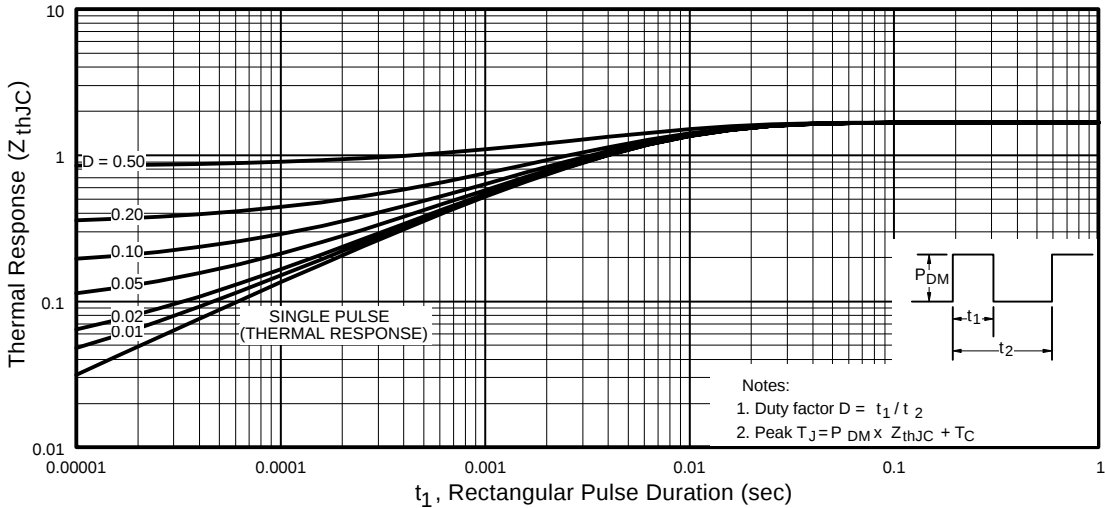


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

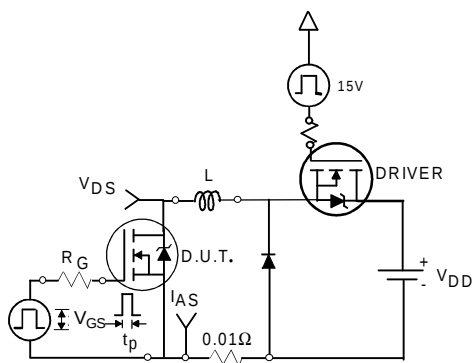


Fig 12a. Unclamped Inductive Test Circuit

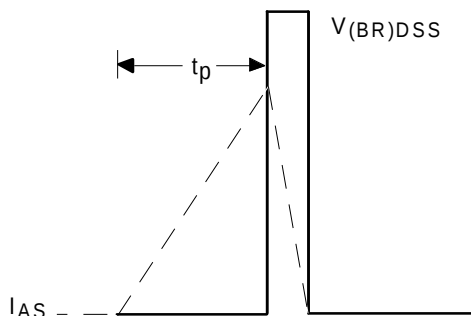


Fig 12b. Unclamped Inductive Waveforms

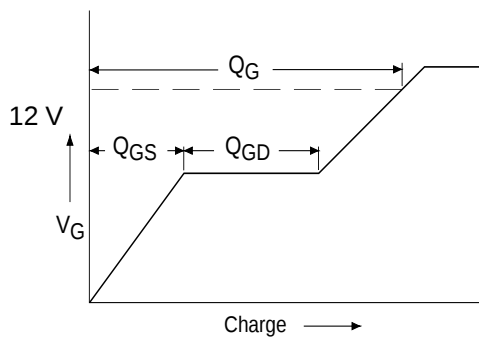


Fig 13a. Basic Gate Charge Waveform

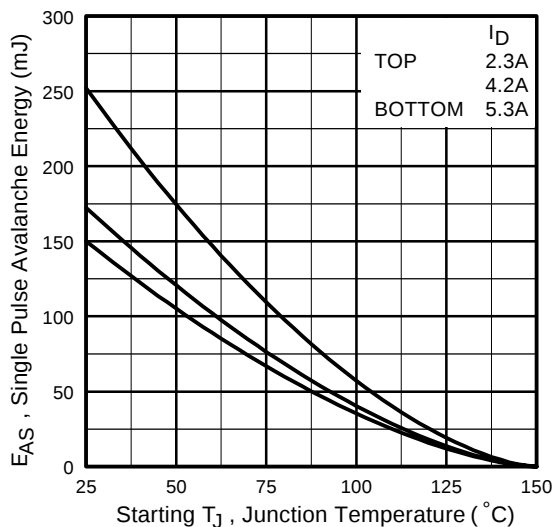


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

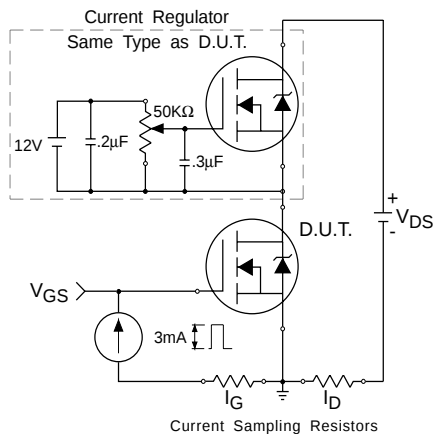
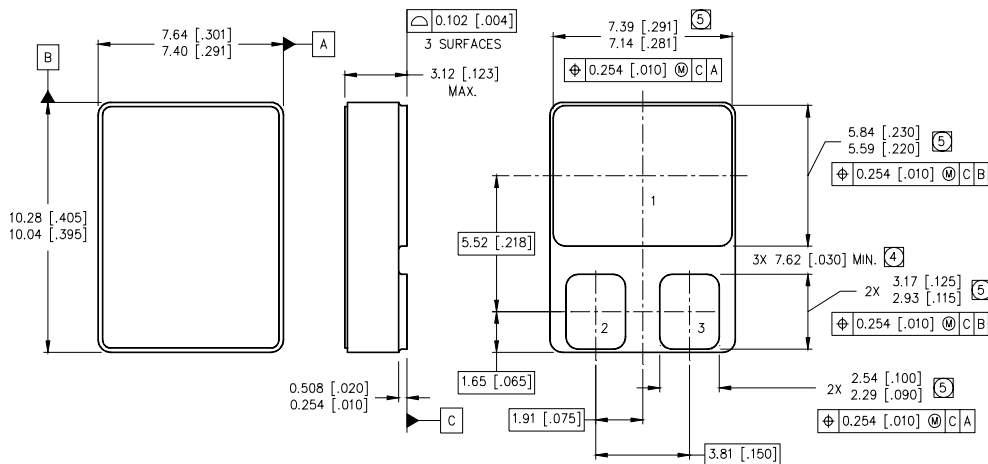


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 50V$, starting $T_J = 25^{\circ}C$, $L = 5.0\text{ mH}$
Peak $I_L = 5.3A$, $V_{GS} = 12V$
- ③ $I_{SD} \leq 5.3A$, $di/dt \leq 240A/\mu s$,
 $V_{DD} \leq 400V$, $T_J \leq 150^{\circ}C$
- ④ Pulse width $\leq 300\text{ }\mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
12 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
320 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — SMD-0.5



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

④ DIMENSION INCLUDES METALLIZATION FLASH.

5 DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

- 1 = DRAIN
2 = GATE
3 = SOURCE

International
IOR Rectifier

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