PM5357

S/UNI-622-POS

SATURN USER NETWORK INTERFACE (622-POS)

ERRATA

ISSUE 7: APRIL 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
7	April, 2000	This document contains errata information corresponding to the issue 4 datasheet and device revision E.
6	February, 2000	This document contains errata information corresponding to the issue 4 datasheet and device revision D.
5	December 1999	This document contains errata information corresponding to the issue 3 datasheet and device revision D.
4	September 1999	This document contains errata information corresponding to the issue 3 datasheet and device revision B.
3	June 1999	This document contains errata information corresponding to the issue 3 datasheet and device revision B.
2	Mar 1999	This document contains errata information corresponding to the issue 3 datasheet and device revision A.
1	Feb 1999	This document contains errata information corresponding to the issue 3 datasheet and device revision A.

CONTENTS

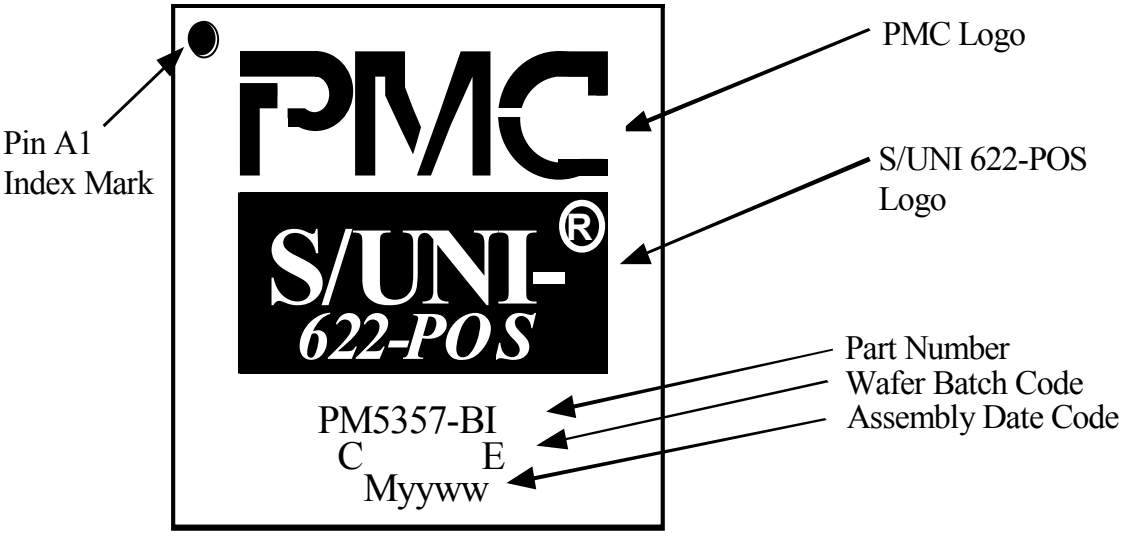
1 ISSUE 7 ERRATA

This issue 7 contains errata applied to the PMC-980911 S/UNI-622-POS Issue 4 datasheet and to Revision E of the device. The issue 4 datasheet and issue 7 errata supersede all prior editions and versions.

1.1 Device Identification

The information contains in this document applies to the PM5357 S/UNI-622-POS revision E device only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). PM5357 S/UNI-622-POS revision E is packaged in a 304 pin Super BGA package.

Figure 1: PM5357 S/UNI-622-POS Branding Format



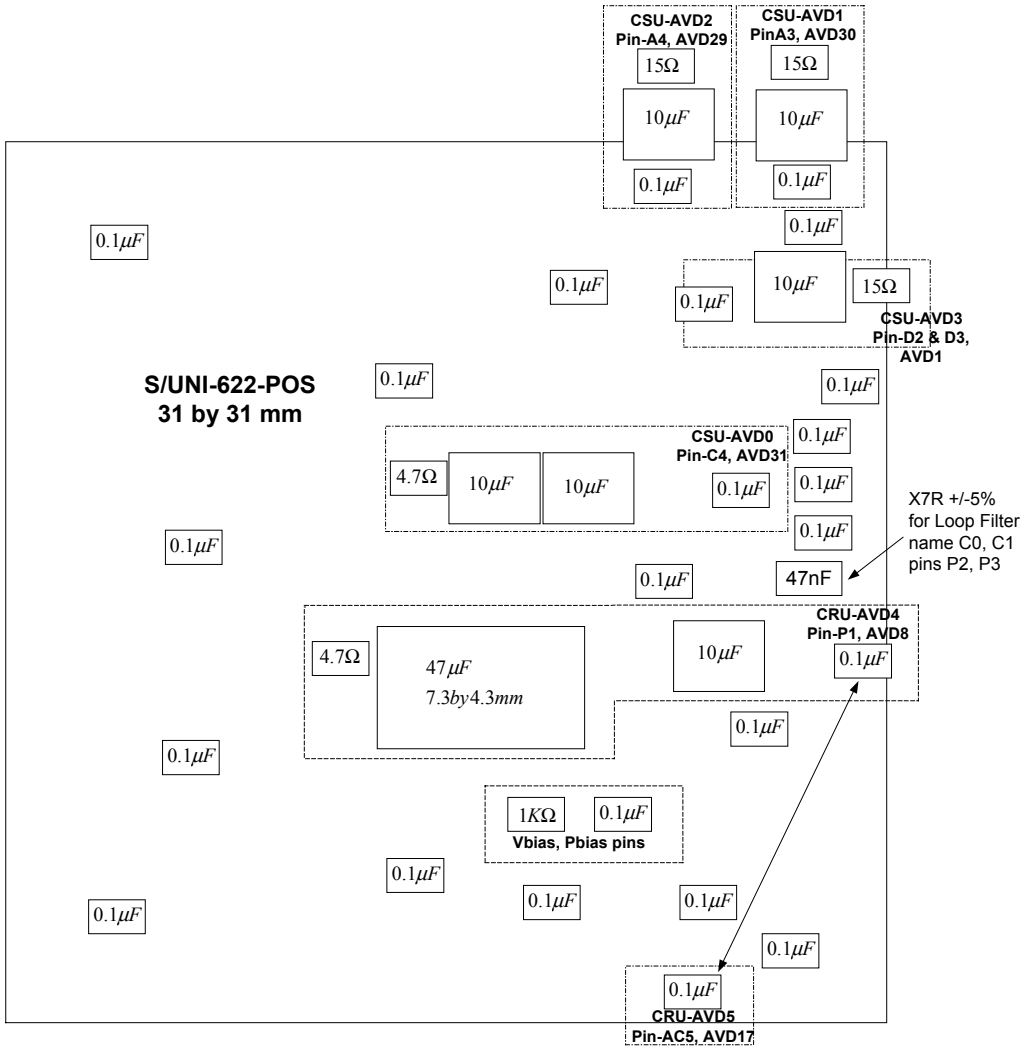
TOP VIEW
SCALE : 2:1
(APPROX.)

2 DATASHEET DOCUMETNATION DISCREPANCIES:

2.1 Power Supply Filtering Mechanical Drawing Incorrect (Pg. 339, Section 13.14)

The loop filter capacitor recommendation specifies a 47nF capacitor not a X7R 47uF capacitor as shown in the datasheet. The correct figure is shown below:

Power Supply Component Layout



2.2 Datasheet Revision History Missing

The datasheet is missing a revision history.

ISSUE	DATE	DETAIL
4	Dec, 1999	#1. Modified section 9.5 (UTOPIA and POS-PHY pin description) and section 14.4 (Functional timing) to reflect operation of the RPA signal (Receive POS-PHY L2 operation requires data be qualified by RVAL). #2 DC characteristics update (Section 16) #3 Registers updated with correct defaults and descriptions: Register 0X01, Bit 4 (TFPEN), Defaults To 1, Not 0 Register 0X08, Description Incorrect Register 0X09 Description Incorrect Register 0XC1, Bit 1 (DSCR), Defaults To 1, Not 0 Register 0XC4, Bit 3 (TPAHWM), Defaults To 0, Not 1 New Register 0XFC: Concatenation Status And Enable New Register 0XFD: Concatenation Interrupt Status New Register Bit Required For OC-3 Operation (Register 0X07) Register 0X5E Bit 5 (RTYPE) To Enable LAN Or WAN Performance Register 0X00 Type Bits Incorrect Loss Of Multi-frame Tributary AIS (LOMTUAIS) Bit 2 Incorrectly Stated In Register 0X0D #4 APS pin description modified #5 Documented overflowing Transmit FIFO #6 Updated TFCLK timing specifications, RFCLK timing specifications

ISSUE	DATE	DETAIL
		#7 Diagnostic Loop-back Clarification #8 Bit Error Rate Monitor Table Update #9 Receive Data Requires 3 RFCLK Cycles Before Becoming Valid (Utopia Level 3 Only) #10 TPAHWM Upper Limit #11 Receive Line AIS Insertion Is Not Gated By ALLONES #12 Large Power Supply Glitch (Beyond Specification) Can Cause Clock Synthesis Unit To Lose Lock To Reference.
3	Jan 13, 1999	Corrected wrong pin number assignments in pin description.
2	Dec 12, 1998	General update in preparation for Issue 2 S/UNI-622-POS
1	Mar 30, 1998	Updated datasheet

2.3 PECL Interface Resistor Value Incorrect (Section 13.14):

The pull down for 3.3V PECL interface is shown as 330 ohm instead of the recommended 150 ohm.

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