Octal Serial Link Multiplexer

FEATURES

- Integrated analog/digital device that interfaces a high speed parallel bus to 8 bidirectional data streams.
- Each stream travels over a high speed Low Voltage Differential Signal (LVDS) serial link.
- Interfaces to 8 S/UNI®-DUPLEX devices (via the LVDS links) to create a point-to-multipoint serial backplane architecture.
- In the LVDS receive direction: accepts cell streams from the 8 LVDS links, multiplexing them into a single cell stream, which is presented to the system bus as a single UTOPIA L2 compatible PHY.
- In the LVDS transmit direction: receives cell streams from the bus master, and routes the cells to the appropriate serial link.
- Cell read/write to the 8 LVDS links is available via the microprocessor port.
- Provides optional hardware assisted CRC32 calculation across cells, which creates an embedded inter-processor communication channel across the LVDS links.
- Optionally routes the embedded control channels from the 8 links to/ from the system bus.
- Under software control, the 8 LVDS links can be individually marked active or standby. This is used by the far end S/UNI-DUPLEX to implement 1:1 protected systems.
- Error monitoring and cell counting on all links.
- Requires no external memories.
- Low power 3.3V CMOS technology.
- Standard 5 pin P1149 JTAG port.
- 304 ball SBGA, 31mm x 31mm.

PARALLEL BUS INTERFACE

- Both directions: 16 bit wide, 52 MHz max clock rate, bus slave.
- Cells transferred to the bus:
  - UTOPIA L2 compatible with optional expanded cell length.
  - Appears as a single PHY, with a cell prepend identifying the source PHY ID of each cell.
  - Alternatively, UTOPIA L2 compliance is supported by placing PHY ID inside the UDF/HEC fields of a standard ATM cell.
- Cells received from the bus:
  - UTOPIA L2 with expanded cell length and addressing capabilities.
  - The S/UNI-VORTEX appears to the bus master as a 264 port multi-PHY device (8 links, each with 32 PHYs & one communication channel).

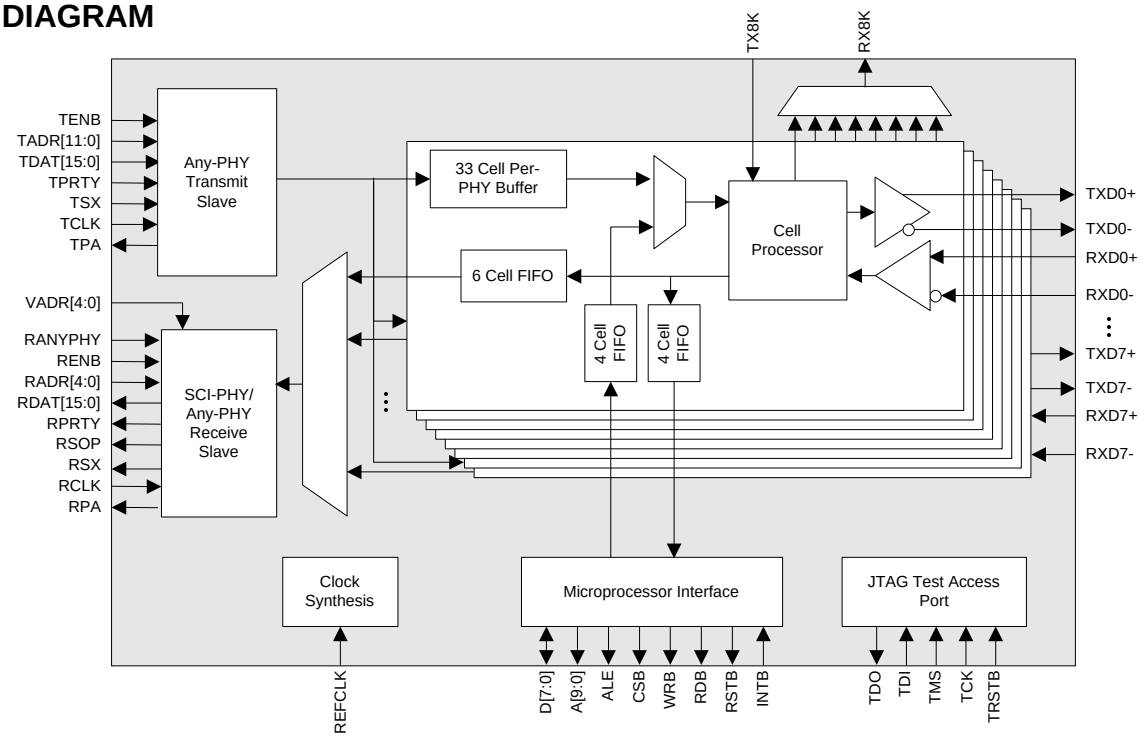
LVDS INTERFACES

- 8 independent 4-wire LVDS serial transceivers, each operating at up to 200 Mb/s.
- Operates across PCB or backplane traces, or across up to 10 meters of 4-wire twisted pair cabling for inter-shelf communications.
- Fully integrated LVDS clock synthesis and recovery. No external analog components are required.
- Usable bandwidth (excludes system overhead) of 186 Mbit/s.

LVDS RECEIVE DIRECTION

- Weighted round-robin multiplex of cell streams from the 8 LVDS links into a single cell stream, which is transferred to the parallel bus under control of the bus master.
- Back-pressure sent to far end to prevent overflow of receiver FIFO.

DIAGRAM



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- LVDS link ID and S/UNI-VORTEX ID is added to each cell (along with the PHY ID already added by S/UNI-DUPLEX) for use by ATM layer to identify cell source.

LVDS TRANSMIT DIRECTION

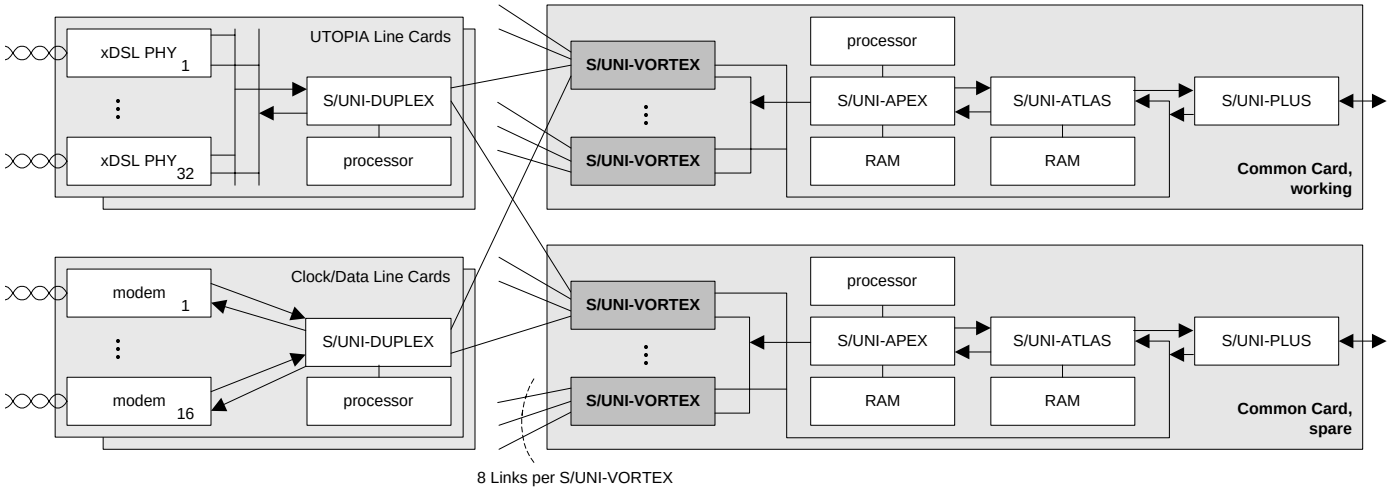
- Per PHY and microprocessor port back-pressure used on each of the 8 links to prevent overflow of downstream buffers.
- Device polling: provides UTOPIA-like TCA status for 264 PHYs based on back-pressure from LVDS links.
- Cell transfer: Bus master adds a PHY address to each cell via a 12 bit ID. S/UNI-VORTEX decodes and accepts cells for its links based on software configured base address.

APPLICATIONS

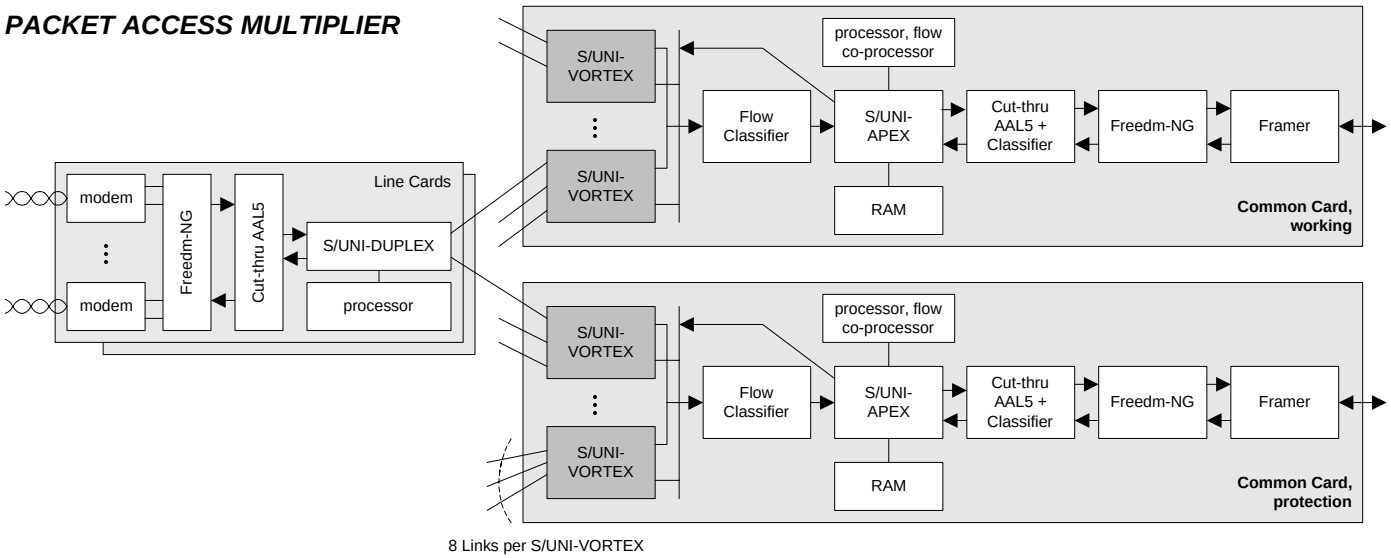
- Single shelf or multi-shelf Digital Subscriber Loop Access Multiplexer (DSLAM)
- ATM, frame relay, IP switch
- Multi-service access multiplexer
- UMTS wireless base stations
- UMTS wireless base station controllers
- Multi-shelf access concentrators

TYPICAL APPLICATIONS

MULTI-SHELF 1024 LINE ATM DSLAM



PACKET ACCESS MULTIPLIER



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