PM73488

QSE

DATA SHEET Errata

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Legal Information

Copyright

PMC-1980616 (P3)

Disclaimer

Trademarks

Patents

The technology discussed is protected by one or more of the following Patents:

U.S. Patent No. 5,557,607; 5,570,348; 5,583,861; 6,151,301; 6,188,690B1

Relevant patent applications and other patents may also exist.

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Revision History

Issue No.	Issue Date	Details of Change
1	Jan. 1999	Creation of document
2	Apr. 1999	Added errata items 1.1, 1.2, 1.4, 1.5
3	June 1999	Aligns with Issue 3 Production Release Data sheet
4	March 2000	Reset timing signal is inverted in Figure 40.
5	Sept. 2001	Added patent award numbers
6	Feb. 2002	Added errata items 2.5, 2.6 ,2.7 and 2.8

Table of Contents

1 Introduction

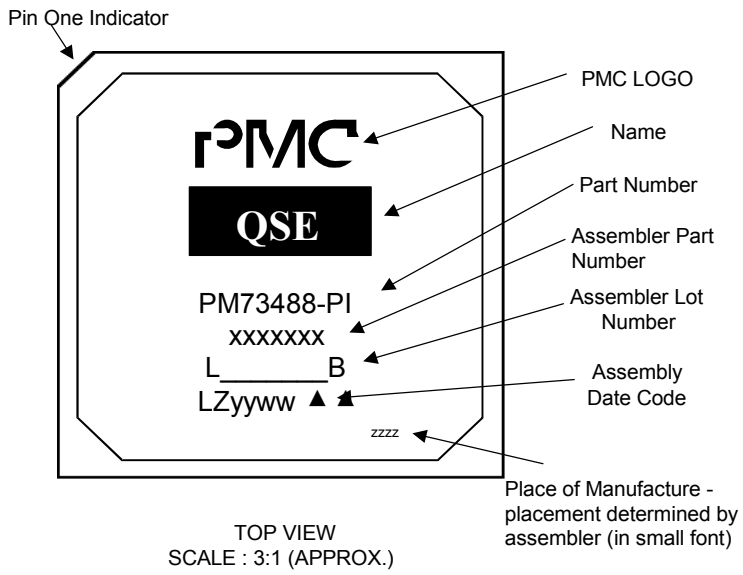
In this document:

- Section 2 lists documentation errors found in Issue 3 of the QSE Data Sheet (PMC-1980616).
- Section3 lists the known functional errata for Revision B of the PM73488 QSE.

1.1 Device Identification

The information contained in Section 2 relates to Revision B of the PM73488 QSE only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device.

Figure 1 PM73488 QSE Branding Format



1.2 References

- Issue 3 of the QSE Data Sheet (PMC-1980616).

2 Documentation Deficiency List

This section lists the known documentation deficiencies for Issue 3 of the QSE Data Sheet (PMC-1980616) as of the publication date of this document.

For each *specific* deficiency, the location of the passage in question, the deficient text, and the replacement text are described. New text is shown in bold. Deleted text is shown as underlined.

For more *general* issues, a description of the nature of the error is given, along with a passage that correctly describes the concept or device function. Please report any documentation deficiencies not covered in this errata to PMC-Sierra.

2.1 Page 92

Add to GANG_DEAD_ACK register description:

For example, if the gang size is 8, and 4 out of the 8 ports are dead/disabled, then a GANG_DEAD_NACK is returned if a cell is sent to any of the 4 dead ports, even though the whole gang (of 8) is not dead/disabled

2.2 Page 109

Add to GANG_DEAD_NACK description:

For example, if the gang size is 8, and 4 out of the 8 ports are dead/disabled, then a GANG_DEAD_NACK is returned if a cell is sent to any of the 4 dead ports, even though the whole gang (of 8) is not dead/disabled.

2.3 Figure 40. Inverted Reset Signal

The RESET signal shown in figure 40 of the data sheet (below) is defined as being asserted during the time period (Tres). Since the RESET pin on the QSE is defined as active high, the RESET signal in figure 40 is incorrect and should be inverted.

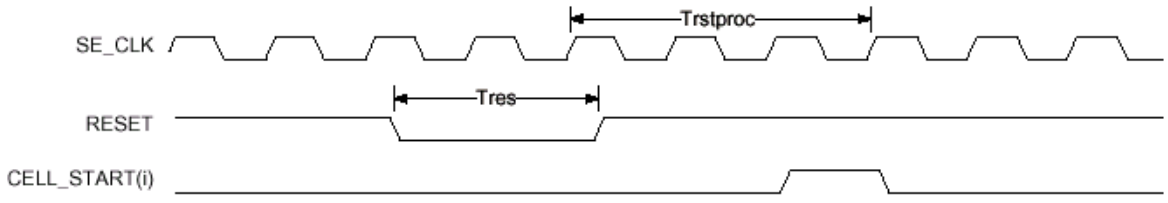


Figure 40 (Data sheet Issue 3). Reset Timing

2.4 Page 2 - US Patents

The PM73488 is protected by the following patents:

US patent 5,557,607

US patent 5,570,348

US patent 5,583,861

US patent 6,151,301

US patent 6,188,690B1

2.5 ESD Specification

There is no ESD specification in Table 22 (Absolute Maximum Ratings) under Section 7, Physical Characteristic, in the current QSE data sheet.

The qualification data indicates that the QSE meets ±500 V ESD.

2.6 Contradictions on Cell Timing/Latency

There are contradictions on cell timing and latency specification between Sections 3.9 and 4.2.2 in the QSE data sheet.

Section 3.9 Cell/Timing Latency mentions that in aggregate mode 1 the latency is 13 clock cycles. Section 4.2.2 Relation Between Local CELL_START and Data Out of the QSE mentions that "The switch latency is 8 clocks from the local CELL_START signal for all unicast gang modes, except for unicast gang mode = 0, in which case the switch latency is 11 clocks."

Section 3.9 is correct, and Section 4.2.2 is in error.

2.7 CHIP_MODE Register

There is a typo in the bit description of the CHIP_MODE register. The bit 1 is shown as Reserved in one place and as SWITCH_MODE in another place. In fact, the bit 1 in this register should be a reserved bit defaulted to ‘0’. Therefore, the SWITCH_MODE description should be ignored.

2.7.1 Location

The bit 1 (SWITCH_MODE) bit description is in the CHIP_MODE register under Section 9.3.2 of the QSE data sheet.

2.7.2 Original Wording

Field (Bits)	Description
ENABLE_STAT_PIN (7)	0 Enable StatOut and CtrlIn pin functionality 1 StatOut behaves like No Data In, and Ctrl In behaves like No Data Out.
PARITY_CHECK (6)	1 Parity checks on cell header disabled. 0 Normal operation.
/NO_DATA_OUT (5)	Current value at the /NO_DATA_OUT pin.
/NO_DATA_IN (4)	Current value at the /NO_DATA_IN pin.
MULTICAST_MODE (3)	1 External RAM present. 0 No external RAM.
CHIP_HARDWARE_RESET (2)	1 Writing a one to this bit will put the chip is in hardware reset (except the processor interface, which remains untouched). 0 Writing a zero to this bit will take the chip out of hardware reset. Upon pin-reset, this bit comes up as a one. A zero must be explicitly written to this bit before the chip can function normally.
SWITCH_MODE (1)	1 Double switch mode. 0 Single switch mode.
Reserved (1:0)	Write with a 0 to maintain future software compatibility.

2.7.3 Replacement Wording

Field (Bits)	Description
ENABLE_STAT_PIN (7)	0 Enable StatOut and CtrlIn pin functionality 1 StatOut behaves like No Data In, and Ctrl In behaves like No Data Out.
PARITY_CHECK (6)	1 Parity checks on cell header disabled. 0 Normal operation.
/NO_DATA_OUT (5)	Current value at the /NO_DATA_OUT pin.
/NO_DATA_IN (4)	Current value at the /NO_DATA_IN pin.
MULTICAST_MODE (3)	1 External RAM present. 0 No external RAM.
CHIP_HARDWARE_RESET (2)	1 Writing a one to this bit will put the chip is in hardware reset (except the processor interface, which remains untouched). 1 Writing a zero to this bit will take the chip out of hardware reset.

	Upon pin-reset, this bit comes up as a one. A zero must be explicitly written to this bit before the chip can function normally.
Reserved (1:0)	Write with a 0 to maintain future software compatibility.

2.8 Typos on Ball Number of RAM_ADD(16) and RAM_PARITY

There are typos on ball number of RAM_ADD(16) and RAM_PARITY pins in Table 17 in the QSE data sheet.

Table 17 in Section 6.4.2 shows that the ball number for the RAM_ADD(16) pin is F18 and for the RAM_PARITY pin is F19. This is not correct.

The correct ball number for RAM_ADD(16) pin is F19 and for the RAM_PARITY pin is F18 as shown in Table 14 in Section 6.2 and in Table 15 in Section 6.3.

3 Device Functional Deficiency List

This section lists the known functional deficiencies for Revision B of the QSE as of the publication date of this document. For each deficiency, the known workaround and the operating constraints, with and without the workaround, are also described.

Please report any functional deficiencies not covered in this errata to PMC-Sierra.

3.1 Short Tag Feature Restriction

This does not apply to cases when the QRT is used in conjunction with the QSE. Short Tags should only be used when the QSE is used with a device other than the QRT.

In the case where the QSE is used with a device other than the QRT, the SHORT_TAG_ENABLE (pg. 97 in 9.3.7 Extended Chip mode) can only be used if Unicast Gang Mode (9.3.25 on pg. 105) is NOT 0.

Notes