

**PM5351**



**S/UNI-TETRA**

**S/UNI-TETRA REFERENCE DESIGN  
ISSUE 2.0**

**ERRATA**

**ISSUE 2: JANUARY 1999**

**REVISION HISTORY**

<b>Issue No.</b>	<b>Issue Date</b>	<b>Details of Change</b>
2	Jan 1999	Added BIAS power supply section
1	Dec 1998	Document created.

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## **1 NEW ISSUE OF THE S/UNI-TETRA REFERENCE DESIGN ERRATA**

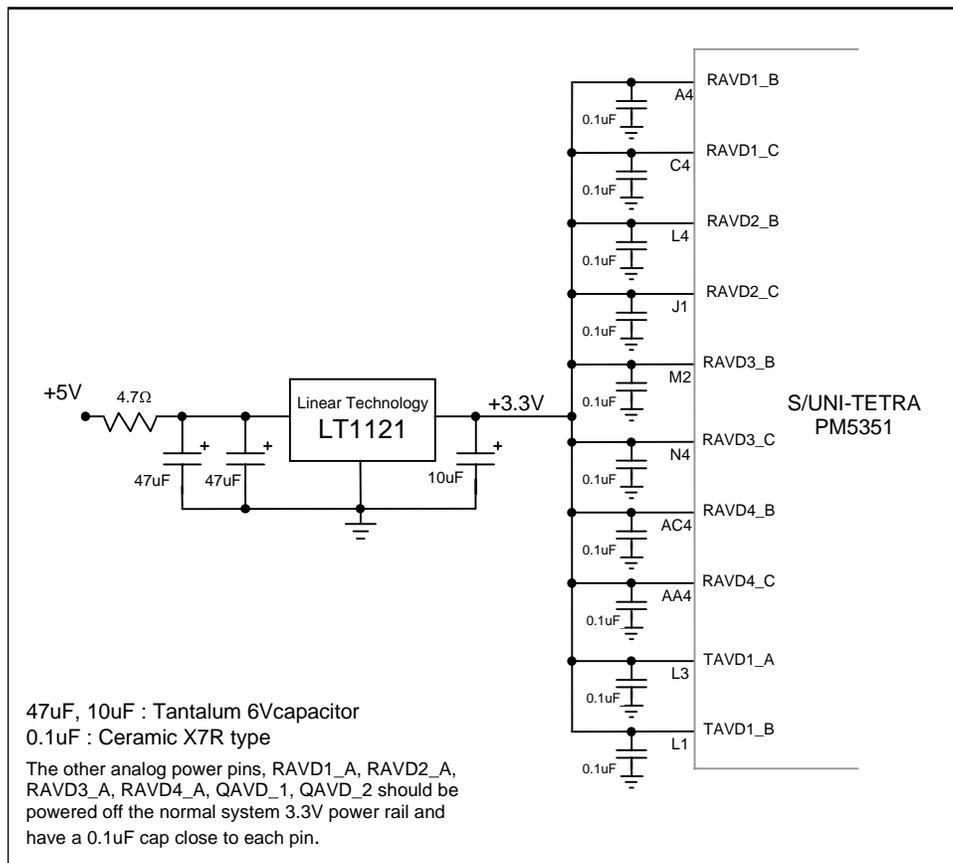
This document is the errata notice for Issue 2.0 of the PMC-980322 S/UNI-TETRA Reference Design.

## 2 CHANGES TO THE ANALOG POWER FILTERING DIAGRAM

Issue: The Analog Power Filtering diagram shows the incorrect pin number (M4) for RAVD3\_B.

Fix: The correct pin number for RAVD3\_B should be M2.

**Figure 1 : Analog Power Filtering Recommendation**

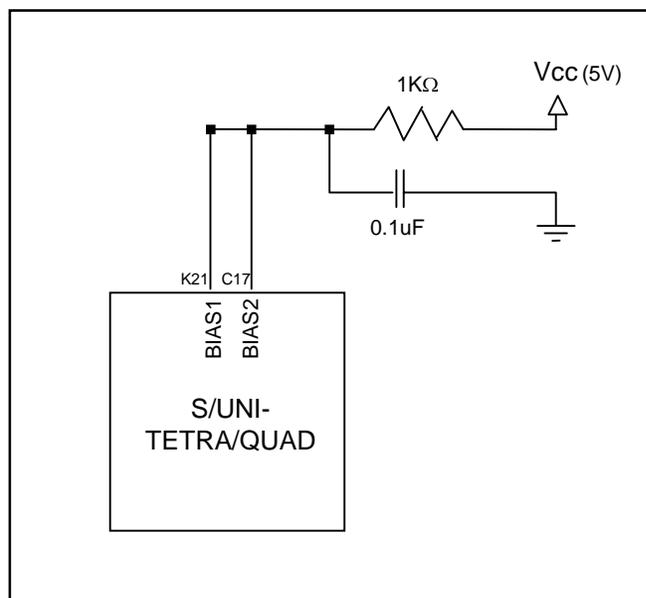


### **3 INCORRECT POWER SUPPLY CONNECTION TO BIAS PINS**

Issue: The schematics shows that 3.3V power supply is connected to the BIAS1, BIAS2 pins.

Fix: BIAS1, BIAS2 pins should be connected only to the Vcc (5V) through a 1K ohm resistor for 5V tolerant operation. The 3.3V should not be connected to the BIAS1, BIAS2 pins.

**Figure 2 : Correct BIAS pin connections for 5V Tolerant Operation**



PRELIMINARY



PM5351 S/UNI-TETRA

ERRATA

PMC-981480

ISSUE 2

S/UNI-TETRA REFERENCE DESIGN ERRATA

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## NOTES

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