PM7364

FREEDM-32

REVISION D AND E DEVICE ERRATA

Issue 6: November, 2001

TABLE OF CONTENTS

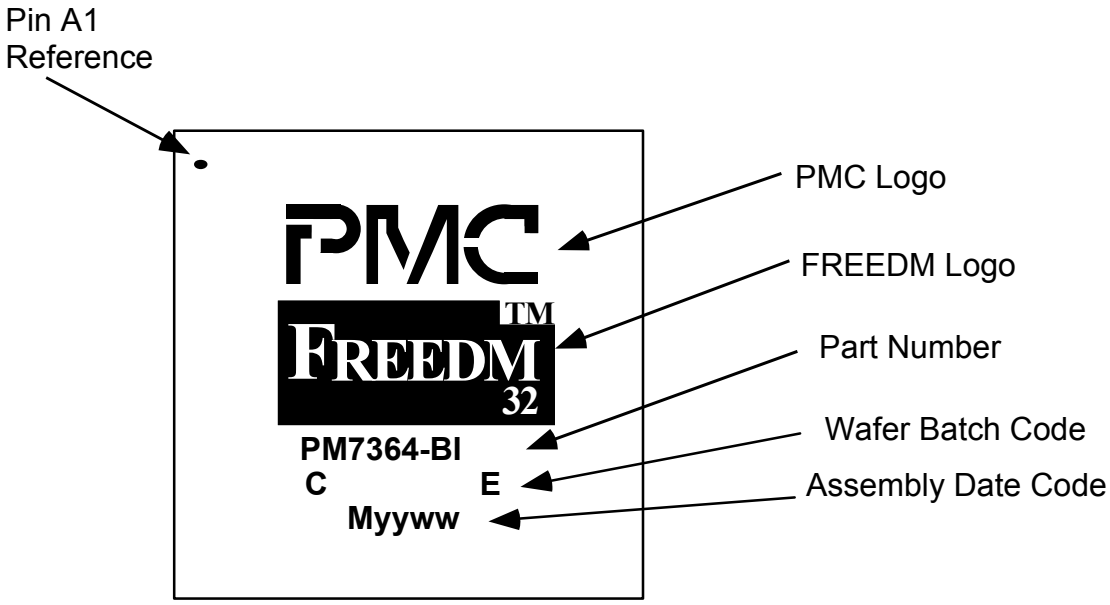
1. INTRODUCTION

In this document, Section 2 lists the known functional errata for Revision D and Revision E of PM7364 FREEDM-32 and Section 3 lists errors found in issue 6 of the FREEDM-32 datasheet (PMC-1960758).

1.1. Device Identification

The information contained in Section 2 relates to Revision D and Revision E of PM7364 FREEDM-32 only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1.1). PM7364 FREEDM-32 is packaged in a 256-pin Ball Grid Array (BGA) package.

Figure 1.1: PM7364 FREEDM-32 Branding Format.



SCALE = 2 : 1 (Approx.)

1.2. Reference:

- PMC-1960758, FREEDM-32 Long Form Data Sheet, Issue 6.

2. FREEDM-32 REVISION D & E FUNCTIONAL DEFICIENCY LIST

This section lists the known functional deficiencies for Revision D and Revision E of FREEDM-32 (as of the publication date of this document). For each deficiency, the known work-around and the operating constraints, with and without the work-around, are also described.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

PMC-Sierra, Inc.
105-8555 Baxter Place
Burnaby, BC
Canada V5A 4V7
Tel: (604) 415-6000
App Support: (604) 415-4533
Fax: (604) 415-6001

Product information: info@pmc-sierra.com
Applications information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

2.1. Offset underflow in Receive Packet Descriptor

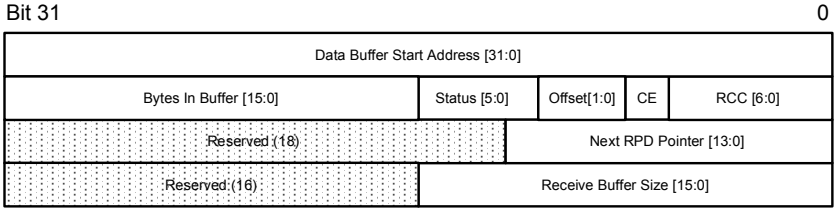
Description:

When ALL of the following conditions are met:

1. The offset[1:0] field of a Receive Packet Descriptor (RPD) is non-zero.
2. The STRIP bit of register "**0x204 RHDL Indirect Channel Data Register #1"** is logic one.
3. The incoming packet payload is smaller than the FCS field (2 bytes for CRC-CCITT or 4 bytes for CRC-32).

The value in the "Bytes in Buffer [15:0]" field of the RPD can be underflowed. That is, this field will contain a negative value. If this field is interpreted as an unsigned integer, the content of the buffer can be erroneously interpreted as a very large number.

Figure 2.1: Receive Packet Descriptor.



Workarounds:

The following are **independent** workarounds for this error:

1. If the Offset[1:0] bits of RPD are set to zero, this problem will not occur.
2. If the STRIP field of "**0x204 RHDL Indirect Channel Data Register #1**" is set to zero, this problem will not occur.
3. If the buffer size is not larger than 32K Bytes, the most significant bit of the "Byte in Buffer" field can be used as a sign bit. The device software should discard RPDs that contain a negative "Bytes in Buffer" value.
4. For every RPD, the driver software can compare the "Bytes in Buffer[15:0]" field to ensure that it is smaller than or equal to "Receive Buffer Size[15:0]".

Performance with workaround:

FREEDM-32 works correctly.

Performance without workaround:

If the "Bytes in Buffer" field is interpreted as a very large number, the driver software may attempt to read data from outside of the allocated buffer space.

2.2. TDR Status Bits Not Reporting All Underflow Events.

Description:

The underflow status bit (Status[2]) of Transmit Descriptor Reference (TDR) indicates whether or not an underflow condition is detected on the transmit packet[1].

In FREEDM-32 Rev D, the underflow status bit does NOT report ALL underflow events. That is, in some cases where underflow did occur, the underflow status bit would incorrectly return a value of zero ("0") to indicate that no underflow event was detected. On the other hand, when underflow did not occur this bit operates normally.

The total underflow count across all channels (register 0x508 PMON Transmit FIFO Underflow Count) is not affected by this and provides an accurate count.

Workarounds:

There is not a known workaround to this problem.

Performance with workaround:

Not applicable.

Performance without workaround:

The system will not be able to keep an accurate underflow count on a per HDLC channel basis.

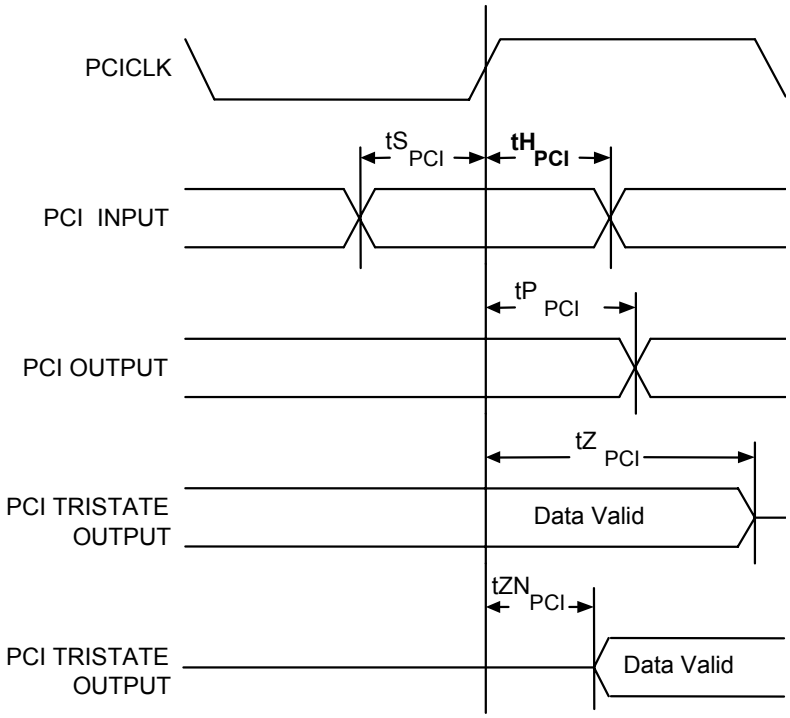
[1] For additional information on the operation of Status[2] in a TDR, please refer to Fig. 9.14, Transmit Descriptor Reference on page 68 of PMC-960758 FREEDM-32 Datasheet.

2.3. PCI Hold Time Increased to 1ns.

Description:

PCI Input and Bi-directional signals require a minimum hold time (tH_{PCI}) of 1 ns with respect to PCICLK.

Figure 2.2: PCI Interface Timing



Workarounds:

The PCI 2.1 specification requires PCI outputs to have a minimum 2 ns propagation delay. The clock skew between FREEDM-32 and other PCI devices in a system must therefore be kept below 1 ns to ensure correct operation.

Performance with workaround:

Operates normally.

Performance without workaround:

If the clock skew is not kept within the above limit, FREEDM-32 may operate incorrectly.

2.4. Misinterpret Octet in the Highest Timeslot as Belonging to Timeslot Zero.

Description:

When a single FREEDM-32 terminates a large number of channelized T1 or E1 links, such as 28 T1 links in an M13 application, the following receive error may be observed: FREEDM-32 can misinterpret the octet in the highest timeslot as belonging to timeslot zero. For example, in a channelized T1 link, the octet in timeslot 24 can be misinterpreted as belonging to timeslot zero. In a channelized E1 link, the octet in timeslot 31 can be misinterpreted as belonging to timeslot zero.

As the result of this error, the receive HDLC channel associated with the highest timeslot may encounter FCS error, octet alignment error or both.

This problem is more likely to occur in designs that involve 16 or more channelized T1 links that share a common receive clock and use a slower SYSCLK such as 25 MHz.

Workarounds:

For each channelized T1 or E1 link, the RCAS should be programmed such that timeslot zero is enabled and assigned to the same HDLC channel as timeslot 24 (for T1) or timeslot 31 (for E1).

Performance with workaround:

FREEDM-32 operates normally. Note that timeslot zero is normally unused when operating with channelized links. Consequently, the proposed workaround should not generate any side effect or limitation.

Performance without workaround:

In a channelized T1 or E1 link, the receive HDLC channel associated with the highest timeslot may encounter FCS error, octet alignment error or both.

2.5. Two Channel, Asynchronous HSSI SYSCLK frequency.

Description:

When a FREEDM-32, operating with a 33MHz SYSCLK, terminates two asynchronous HSSI links; if both links operate at their maximum 52 MHz Datarate, data corruption can occur.

Note that all other modes of operation, including two synchronous 52 MHz HSSI links, are error free.

Workarounds:

If two channel, asynchronous HSSI operation is desired, a 35 MHz SYSCLK reference clock should be used, rather than the 33 MHz SYSCLK specified in the datasheet.

Performance with workaround:

FREEDM-32 operates normally.

Performance without workaround:

If both asynchronous HSSI links operate at the maximum 52 MHz datarate, data corruption can occur.

2.6. PCI bus fails to disconnect when multi-phase read extends beyond PCI address Space.

Description:

If a multi-phase read transaction on the PCI bus attempts to read a register address beyond the 4K addresses reserved for the FREEDM-32 registers, the FREEDM will not disconnect from the PCI bus causing it to hang.

Workarounds:

It is recommended that all read transactions, including multi-phase reads, remain within the 4K address range.

Performance with workaround:

The FREEDM-32 operates normally.

Performance without workaround:

If read operations extend beyond the reserved address space, the FREEDM-32 will not disconnect from the PCI bus.

3. DOCUMENTATION ERRORS

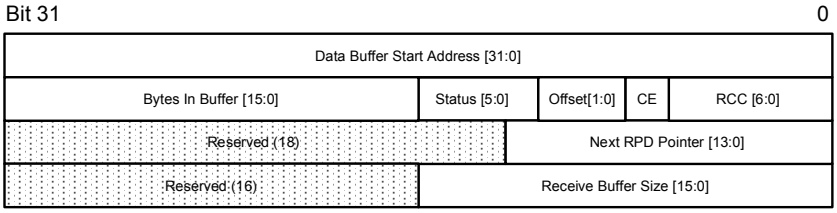
This section lists documentation errors found in issue 6 of PMC-960758 FREEDM-32 Datasheet:

3.1. Receive Packet Descriptor, Buffer Size Restriction

Description:

The Receive Buffer Size [15:0] field of the RPD was incorrectly specified in the FREEDM-32 Datasheet.

Figure 3.1: Receive Packet Descriptor.



In Table 6 "Receive Packet Descriptor Fields" of, Receive Buffer Size [15:0] is currently specified as:

Field	Description
Receive Buffer Size [15:0]	The Receive Buffer Size [15:0] bits indicate the size in bytes of the current RPD's data buffer. This field is expected to be configured by the Host during initialization. The Receive Buffer Size must be a non-zero integer multiple of four and less than or equal to 32764. The Receive Buffer Size is valid in all RPDs.

Correction:

The correct description of Receive Buffer Size [15:0] is shown below.

Field	Description
Receive Buffer Size [15:0]	The Receive Buffer Size [15:0] bits indicate the size in bytes of the current RPD's data buffer. This field is expected to be configured by the Host during initialization. ~~The Receive Buffer Size must be a non-zero integer multiple of four and less than or equal to 32764.~~ The Receive Buffer Size must be a non-zero integer multiple of 16 and less than or equal to 32752. The Receive Buffer Size is valid in all RPDs.

NOTES

PMC-1980429r6 Issue date: Nov, 2001.