PM4344/PM6344

TQUAD/EQUAD WITH QDSX REFERENCE DESIGN

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2 OVERVIEW

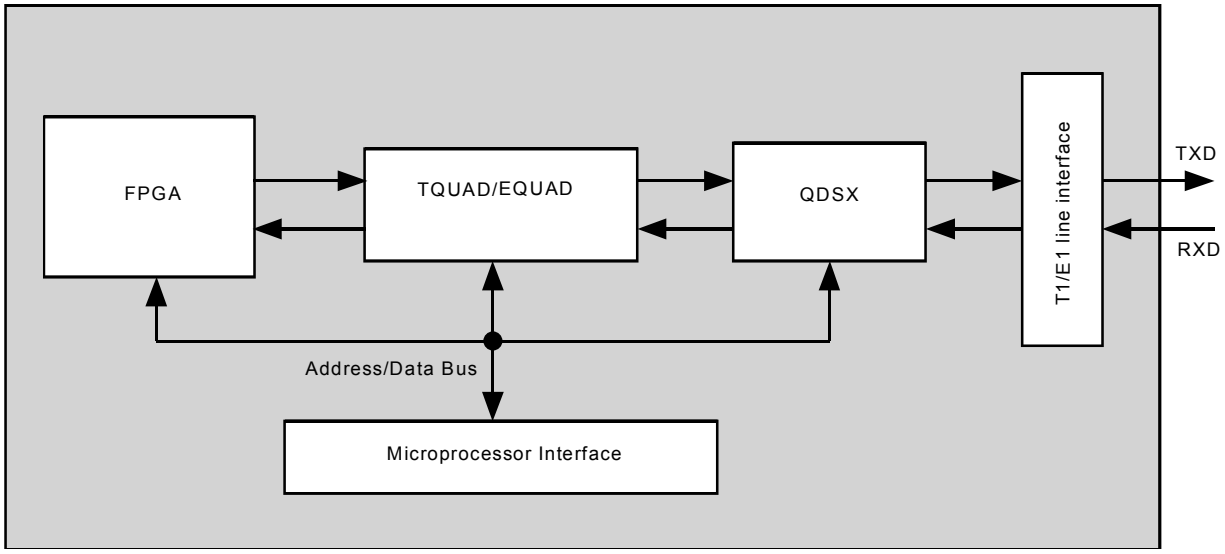
The TQUAD/EQUAD with QDSX reference design demonstrates PMC-Sierra's TQUAD and EQUAD chipsets. This reference design embodies PMC-Sierra's guidelines and suggestions for designing a four port DSX-1/E1 interface card.

This design shows the simplicity of combining the TQUAD and EQUAD into one design, capable of interfacing to T1 or E1 signals. The TQUAD and EQUAD are pin-to-pin compatible, allowing both to be designed into the same footprint. By simply interchanging the TQUAD and EQUAD, and changing some resistors, the board can be converted between T1 and E1 mode.

The TQUAD/EQUAD with QDSX reference design has both line and system side loopback capabilities. This permits the user to evaluate the performance of PMC-Sierra's TQUAD, EQUAD, and QDSX chipsets in an applications environment.

An FPGA provides access to various timing options available within the TQUAD/EQUAD. These timing options allow the backplane to be timed to a number of different sources. The timing may be sourced from on-board oscillators or from clocks recovered within the TQUAD/EQUAD. The following figure gives an overview of the TQUAD/EQUAD with QDSX reference design.

Figure 1 High-Level Block Diagram



This reference board receives and transmits up to four T1/E1 signals. The line interface circuitry consists of the transformers, connectors, and passive networks

necessary to interface the QDSX device to cables carrying G.703-compliant signals.

The PM4314 QDSX is a quad line interface unit with integrated DSX-1 and CEPT E1 interfaces. In this reference design, PMC Sierra's QDSX is being used to provide a T1/E1 interface for the four duplex serial data streams.

The TQUAD/EQUAD is a quadruple T1/E1 framer. Each individual receiver performs clock recovery (optional), performs jitter attenuation (optional), finds frame alignment, monitors performance, extracts facility datalink and signaling bits, and retimes the signal to a backplane clock via the elastic store. Each individual transmitter receives the signal to be transmitted from the backplane, inserts framing, facility datalink, signaling, and other overhead bits, performs jitter attenuation, and transmits the digital signal to the line side.

An on-board LED display indicates alarm conditions detected by the TQUAD/EQUAD. This LED Display is controlled by the microprocessor.

The ACTEL A1460A FPGA provides a PRBS data generator, loopback schemes, timing options and extra logic required by the LED display. All necessary signals needed for microprocessor access to the FPGA have been provided.

The microprocessor interface carries all the signals required to connect the TQUAD/EQUAD with QDSX reference design to a host 8-bit multiplexed microprocessor bus. This connector provides access to the full set of registers in the TQUAD/EQUAD and QDSX.

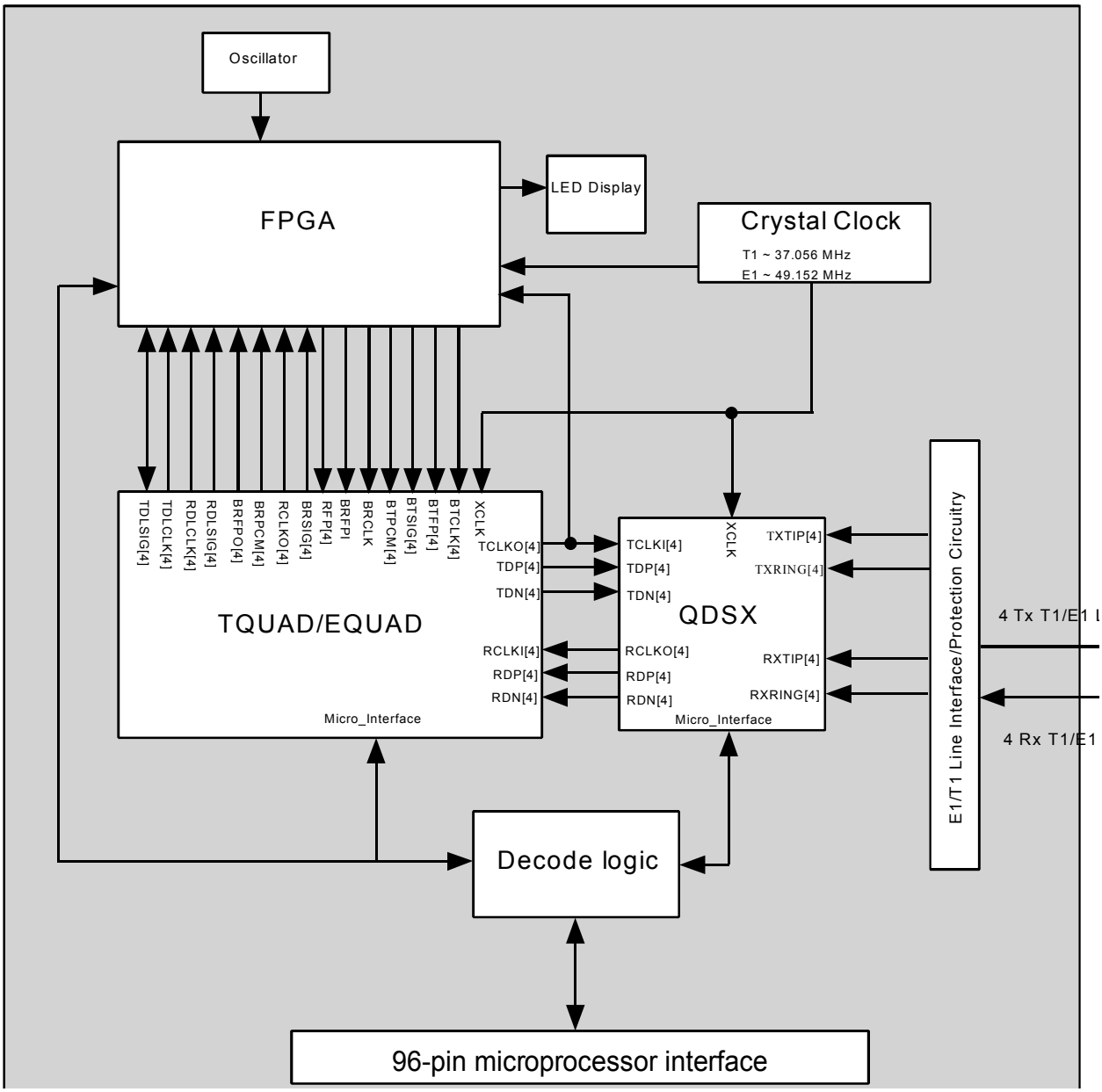
3 FUNCTIONS AND IMPLEMENTATION

The following sections provide a functional description of the components on board.

3.1 Block Diagram

The TQUAD/EQUAD with QDSX reference design consists of nine main functional blocks. There are two external interfaces: the T1/E1 Line Interface and the 96-pin microprocessor interface. The FPGA provides system loopbacks, PRBS generation, LED logic, and several timing options. The microprocessor interface provides external access for a microprocessor to initialize and monitor the performance of the TQUAD/EQUAD and the QDSX. The microprocessor has access to the FPGA to control the alarm LEDs and select various operating options. Each individual block is explained below.

Figure 2 Block Diagram



3.2 TQUAD/EQUAD

The 128 pin TQUAD and EQUAD chips are pin-to-pin compatible, which allows the two chips to be designed into the same footprint.

3.2.1 PM4344 TQUAD

The TQUAD is a quadruple T1 framer. Each individual receiver performs clock recovery (optional), performs jitter attenuation (optional), finds frame alignment, monitors performance, extracts facility datalink and signaling bits, and retimes the signal to a backplane clock via the elastic store. Each individual transmitter receives the signal to be transmitted from the backplane, inserts framing, facility datalink, signaling, and other overhead bits, performs jitter attenuation, and transmits the digital signal to the line side. Multiplexing and demultiplexing of the backplane data and signaling bits from the transmit and receive sides of the four T1 framers is supported but not available in this reference design.

The full register set of the TQUAD, including Test Mode registers, are accessible to the host microprocessor.

For a full description of the TQUAD, refer to the TQUAD Data book.

3.2.1.1 Configuring the TQUAD from Reset

The microprocessor must first determine whether the TQUAD/EQUAD with QDSX reference board contains the TQUAD or the EQUAD. As the ID register is the same on both the TQUAD and the EQUAD, Register 006H must be used instead. The bit to check is shown in the following table.

Table 1 TQUAD Register – Address: 006H

Bit	Bit Value
4	0

After TQUAD power up, a software reset should be performed on the TQUAD to put it in a default state. A software reset is performed by setting the RESET bit (register 0DH) and then clearing it.

Table 2 TQUAD Default Settings

Setting	Receiver Section	Transmitter Section
Framing Format	SF	SF
Line Code	B8ZS	AMI

Setting	Receiver Section	Transmitter Section
DS1 Interface	Pins RDP/RDD[x] and RDN/RCLV[x] active as digital inputs RDP[x] and RDN[x] and used for clock and data recovery	TDP[x], TDN[x] outputs NRZ data updated on falling TCLKO[x] edge
System Backplane	1.544MHz data rate BRPCM[x], BRSIG[x] active BRFPO[x] indicates frame pulses	1.544MHz data rate BTPCM[x] active BTSIG[x] inactive BTFP[x] indicates frame alignment
Data Link	internal RFDL disabled RDLSIG[x] and RDLCLK[x] outputs held low	internal XFDL disabled TDLCLK[x] output held low, TDLSIG[x] input ignored
Options	ELST not bypassed RFP help low PMON accumulates OOFs (not COFAs)	Signaling alignment disabled F, CRC, FDL, bit bypass disabled
Timing Options	Not applicable	Digital jitter attenuation enabled, with TCLKO[x] referenced to BTCLK[x]
Diagnostics	All diagnostic modes disabled	All diagnostic modes disabled

In the following tables the “Addr Offset” is the address relative to each framer. The base addresses are given in Table 3.

Table 3 Base Addresses for the TQUAD and EQUAD

Quadrant	Base Address
0	000H
1	080H
2	100H
3	180H

To configure the TQUAD for ESF framing format, after a reset, the registers should be written with the values indicated in Table 4.

Table 4 ESF Frame Format

Action	Addr Offset	Data	Effect
Write CDRC Configuration Register	10H	00H	Select B8ZS line code for receiver
Write XBAS Configuration Register	44H	3XH	Select B8ZS, enable for ESF in transmitter (bits defined by 'X' determine the FDL data rate & Zero Code suppression algorithm used)
Write FRMR Configuration Register	20H	1XH 5XH 9XH	Select ESF, 2 of 4 OOF threshold Select ESF, 2 of 5 OOF threshold Select ESF, 2 of 6 OOF threshold (bits defined by 'X' determine the FDL data rate, should be the same as those written to XBAS)
Write RBOC Enable Register	2AH	00H or 02H	Enable 8 out of 10 validation Enable 4 out of 5 validation
Write ALMI Configuration Register	2CH	1XH	Select ESF (bits defined by 'X' determine the ESF YELLOW data rate, should be the same as those written to FRMR)
Write IBCD Configuration Register	3CH	00H	Enable Inband Code detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	1XH	Select ESF (bits defined by 'X' should be the same as those written to FRMR)

To Configure the TQUAD for SLC®96 framing format, after a reset, the registers should be written with the values indicated in Table 5.

Table 5 SLC®96 Frame Format

Action	Addr Offset	Data	Effect
Write CDRC Configuration Register	10H	80H	Select AMI line code for receiver
Write XBAS Configuration Register	44H	08H	Select AMI, enable for SLC®96 in transmitter
Write FRMR Configuration Register	20H	08H 48H 88H	Select SLC®96, 2 0f 4 OOF threshold Select SLC®96, 2 0f 5 OOF threshold Select SLC®96, 2 0f 6 OOF threshold
Write ALMI Configuration Register	2CH	08H	Select SCL®96
Write IBCD Configuration Register	3CH	00H	Enable Inband Code Detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	08H	Select SLC®96

To configure the TQUAD for SF framing format, after a reset, the following registers should be written with the indicated values:

Table 6 SF Frame Format

Action	Addr Offset	Data	Effect
Write CDRC Configuration Register	10H	80H	Select AMI line code for receiver
Write XBAS Configuration Register	44H	00H	Select AMI, enable for SF in transmitter

Action	Addr Offset	Data	Effect
Write FRMR Configuration Register	20H	00H 40H 80H	Select SF, 2 of 4 OOF threshold Select SF, 2 of 5 OOF threshold Select SF, 2 of 6 OOF threshold
Write ALMI Configuration Register	2CH	00H	Select SF
Write IBCD Configuration Register	3CH	00H	Enable Inband Code detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	00H	Select SF

To configure the TQUAD for T1DM framing format, after a reset, the registers should be written with the indicated values:

Table 7 T1DM Frame Format

Action	Addr Offset	Data	Effect
Write CDRC Configuration Register	10H	80H	Select AMI line code for receiver
Write XBAS Configuration Register	44H	04H or 0CH	Select AMI, enable for T1DM in transmitter
Write FRMR Configuration Register	20H	04H 44H 84H	Select T1DM, 2 of 4 OOF threshold Select T1DM, 2 of 5 OOF threshold Select T1DM, 2 of 6 OOF threshold
Write ALMI Configuration Register	2CH	04H 0CH	Select T1DM with standard RED integration Select T1DM with alternate RED integration
Write IBCD Configuration Register	3CH	00H	Enable Inband Code detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern

Action	Addr Offset	Data	Effect
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	04H	Disable robbed bit signaling extraction

3.2.2 PM6344 EQUAD

The EQUAD is a quadruple E1 framer. Each individual receiver performs clock recovery (optional), performs jitter attenuation (optional), finds frame alignment, monitors performance, extracts facility datalink and signaling bits, and retimes the signal to a backplane clock via the elastic store. Each individual transmitter receives the signal to be transmitted from the backplane, inserts framing, facility datalink, signaling, and other overhead bits, performs jitter attenuation, and transmits the digital signal to the line side. Multiplexing and demultiplexing of the backplane data and signaling bits from the transmit and receive sides of the four E1 framers is supported but not available in this reference design.

The full register set of the EQUAD, including Test Mode registers, are accessible to the host microprocessor.

For a full description of the EQUAD, refer to the EQUAD Data book.

3.2.2.1 Configuring the EQUAD from reset

The microprocessor must first determine whether the TQUAD/EQUAD with QDSX reference board contains the TQUAD or the EQUAD. As the ID register is the same on both the TQUAD and the EQUAD, Register 006H must be used instead. The bit to check is shown in the following table.

Table 8 EQUAD Register – Address: 006H

Bit	Bit Value
4	1

After EQUAD power up, a software reset should be performed on the EQUAD to put it in a default state. A software reset is performed by setting the RESET bit (register 0DH) and then clearing it. The recommended initial configuration is given in Table 9.

The base addresses for the EQUAD are the same as those for the TQUAD, which are given in Table 3.

Table 9 EQUAD Recommended Configuration

Offset Register Address (hex)	Recommended Configuration
06	TXSA4EN=1 Default value.
09	RXSA4EN=0 This allows TS16 to be extracted for D-Channel processing.
10	AMI=X Setting this bit disables the HDB3 decoding. ALGSEL=1 This selects a clock recovery algorithm with the best tolerance of high frequency jitter.
11	LOSE=1 This enables changes in the status of the LOS detection circuit to generate interrupt indications on the EQUAD'S INTB output pin.
19	N1[7:0]=FF The value in this register must be the same as in Register 1AH when the transmit timing reference is at the line rate.
1A	N2[7:0]=FF This sets the DJAT transfer function for maximum jitter attenuation.
1B	CENT=1 This allows the DJAT FIFO to center itself thereby providing maximum room to absorb phase differences between the input and output transmit clocks. SYNC=0 This bit should be cleared whenever Register 1AH does not contain its default value (2FH). LIMIT=0 This function should be disabled so that the DJAT FIFO does disrupt the DJAT PLL operation. With the hardware connections recommended in this document, the FIFO should never reach a condition where LIMIT would be useful.
20	CRCEN=1 This enables the MFAS alignment circuitry in the FRMR. CASDIS=1 This disables the CAS multiframe alignment circuitry in the FRMR. REFCRCE=1 This enables the CRC error monitor to force a reframe if an excessive CRC error condition is detected.

Offset Register Address (hex)	Recommended Configuration
21	BIT2C=1 This enables the EQUAD to declare OOF if Bit 2 of TS0 of NFAS frames is received incorrectly for three consecutive frames.
22	OOFE=1 This enables changes in the status of the FAS alignment circuit to generate interrupt indications on the EQUAD'S INTB output pin. OOCMFE=1 This enables changes in the status of the MFAS alignment circuit to generate interrupt indications on the EQUAD'S INTB output pin.
23	RRAE=1 This enables changes in the status of the RAI detection circuit to generate interrupt indications on the EQUAD'S INTB output pin. REDE=1 This enables changes in the status of the RED detection circuit to generate interrupt indications on the EQUAD'S INTB output pin. AISE=1 This enables changes in the status of the AIS circuit to generate interrupt indications on the EQUAD'S INTB output pin.
30	IND=1 This enables indirect accessing of the Transmit Per-Channel Serial Controller (TPSC) registers within the EQUAD.
44	SIGEN=0 This disables the transmission of Channel-Associated Signaling in TS16. DLEN=0 This disables the transmission of Channel-Associated Signaling in TS16. GENCRC=1 This enables the generation of the CRC multiframe.

3.2.3 Internal Loopbacks

The TQUAD/EQUAD provides three internal loopback modes to aid in network and system diagnostics. The network loopbacks (PAYLOAD and LINE) can be initiated at any time via the microprocessor interface, but are usually initiated once an inband loopback activate code is detected. The system loopback

(Diagnostic) can be initiated at any time by the system, via the microprocessor interface, to check the path of the system data through the framer.

For more information on internal loopback modes see the TQUAD/EQUAD Data book.

3.3 QDSX

The QDSX is a full-featured quadruple T1/E1 line interface unit that provides a G.703-compliant interface for 1544 kbit/s and 2048 kbit/s rates.

The full register set of the QDSX, including Test Mode registers, are accessible to the host microprocessor. For a full description of these registers, refer to the QDSX Data book.

In this reference design, the QDSX is being used to provide a T1/E1 interface for four duplex T1/E1 serial data streams.

3.3.1.1 Configuring the QDSX from Reset

After QDSX power up, a software reset should be performed on the QDSX to put it in a default state. The software reset is performed by setting the RESET bit (register 07H) and then clearing it. The initial configuration is given in Table 10 as well as the offset registers from the base address of each quadrant of the QDSX.

The base addresses for the QDSX are given in Table 10.

Table 10 Base Addresses for the PM4314 QDSX

Quadrant	Base Address
0	000H
1	040H
2	080H
3	0C0H

Table 11 QDSX Register Configuration

Offset Register Address (hex)	Register Configuration
000	RDUAL = 1 Sets the receive section to output dual-rail data. If the XIBC or the PRSG are in the receive path, they will be bypassed. CEPT = 0 Receive section configured for T1 applications. CEPT = 1 Receive section configured for E1 applications. All CEPT bits in all four quadrants, in both transmit and receive sections, should be set to the same value.
001	TDUAL = 1 Sets the transmit section to receive dual-rail data. CEPT = 0 Transmit section configured for T1 applications. CEPT = 1 Transmit section configured for E1 applications.

Additional features, such as setting the transmit pulse template, are not within the scope of this document. For more information, see the QDSX data book.

3.4 Microprocessor Interface

The 96-pin connector carries all the signals required to connect the TQUAD/EQUAD with QDSX reference design to a host 8-bit multiplexed microprocessor bus. The pin description for the Microprocessor interface is given in Table 12.

Table 12 Microprocessor Interface Pin Descriptions

Signal Name	Type	Pin	Function
ALE	I	C1	Address latch enable. When high, identifies that address is valid on AD[7:0]. This signal is used for demultiplexing the microprocessor bus.
E	I	C2	External data access indication. Active high.
RWB	I	C3	Active low write enable, active high read enable.
RSTB	I	C4	Active low hardware RESET. This is connected to all devices providing a hardware RESET pin.

Signal Name	Type	Pin	Function
A[15]	I	C5	Address bus bit 15
A[14]	I	C6	Address bus bit 14
A[13]	I	C7	Address bus bit 13
A[12]	I	C8	Address bus bit 12
A[11]	I	C9	Address bus bit 11
A[10]	I	C10	Address bus bit 10
A[9]	I	C11	Address bus bit 9
A[8]	I	C12	Address bus bit 8
AD[7]	I/O	C13	Multiplexed address/data bus bit 7
AD[6]	I/O	C14	Multiplexed address/data bus bit 6
AD[5]	I/O	C15	Multiplexed address/data bus bit 5
AD[4]	I/O	C16	Multiplexed address/data bus bit 4
AD[3]	I/O	C17	Multiplexed address/data bus bit 3
AD[2]	I/O	C18	Multiplexed address/data bus bit 2
AD[1]	I/O	C19	Multiplexed address/data bus bit 1
AD[0]	I/O	C20	Multiplexed address/data bus bit 0
PA3	I	C21	68HC11 Processor Port A bit 3
PA4	I	C22	68HC11 Processor Port A bit 4
PA5	I	C23	68HC11 Processor Port A bit 5
PA6	I	C24	68HC11 Processor Port A bit 6
PD2	O	C25	Master In Slave Out (MISO) of 68HC11 Port D bit 2 acting as SPI. Pulled up on motherboard.
PD3	I	C26	Master Out Slave In (MOSI) of 68HC11 Port D bit 3 acting as SPI. Pulled up on motherboard.
PD4	I	C27	Serial Clock (SCK) of 68HC11 Port D bit 4 acting as SPI. Pulled up on motherboard.
PD5	I	C28	Slave Select (SS) of 68HC11 Port D bit 5 acting as SPI active low. Pulled up on motherboard.
IRQB	O	C29	Maskable 68HC11 interrupt. Pulled up on motherboard.

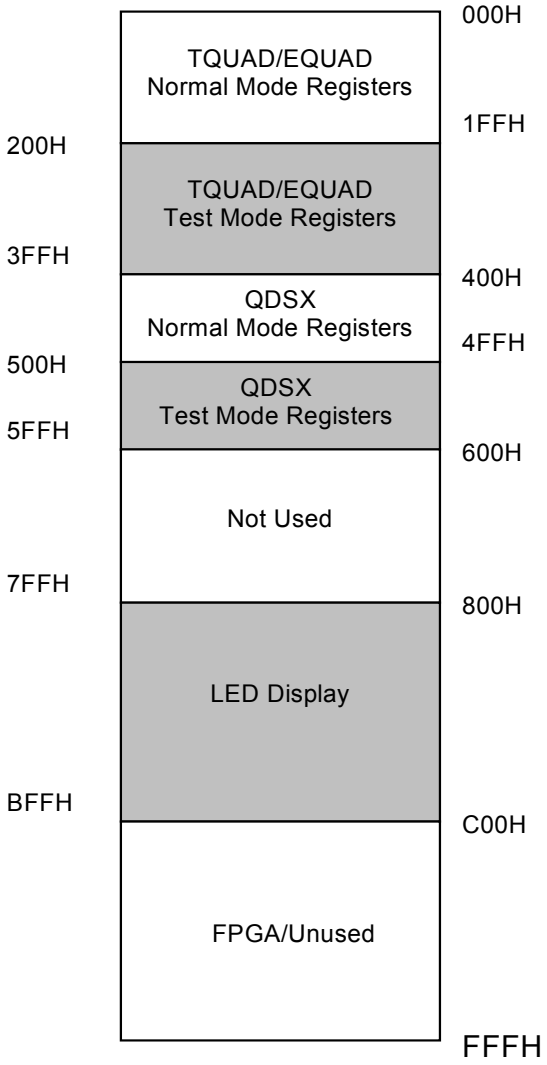
Signal Name	Type	Pin	Function
XIRQB	O	C30	Non-Maskable 68HC11 interrupt. Pulled up on motherboard.
DISB	O	C31	EVMB memory disable. Pulling this signal low will disable MPU access to the EVMB's on board RAM and EPROM. Pulled up on motherboard
SP	I	C32	Spare
GND	GND	A1-A28	Ground
+5 V	PWR	A29-A32	+5 Volts

3.4.1 Decode Logic

The decode logic functional block provides the chip select decoding and the memory mapping from the microprocessor to the TQUAD/EQUAD with QDSX reference design.

The PM1501 Evaluation Motherboard provides address space for external hardware (ie. the TQUAD/EQUAD with QDSX reference design), starting at C000H to CFFFH. The memory map for this design is shown in Figure 3.

Figure 3 Memory Map



3.5 Line Side Interface

The line interface circuitry consists of the transformers, connectors and passive networks necessary to interface the QDSX device to cables carrying G.703-compliant 1544 kbit/s and 2048 kbit/s signals.

3.5.1 Protection Circuitry

Circuitry has been added to provide secondary line protection against faults such as lightning surges, AC power faults and various maintenance related hazards.

This protection circuitry has been designed to meet both ETS 300 046 and FCC Part 68 Standards. The protection circuit is shown in the following figure.

Figure 4 Protection Circuitry

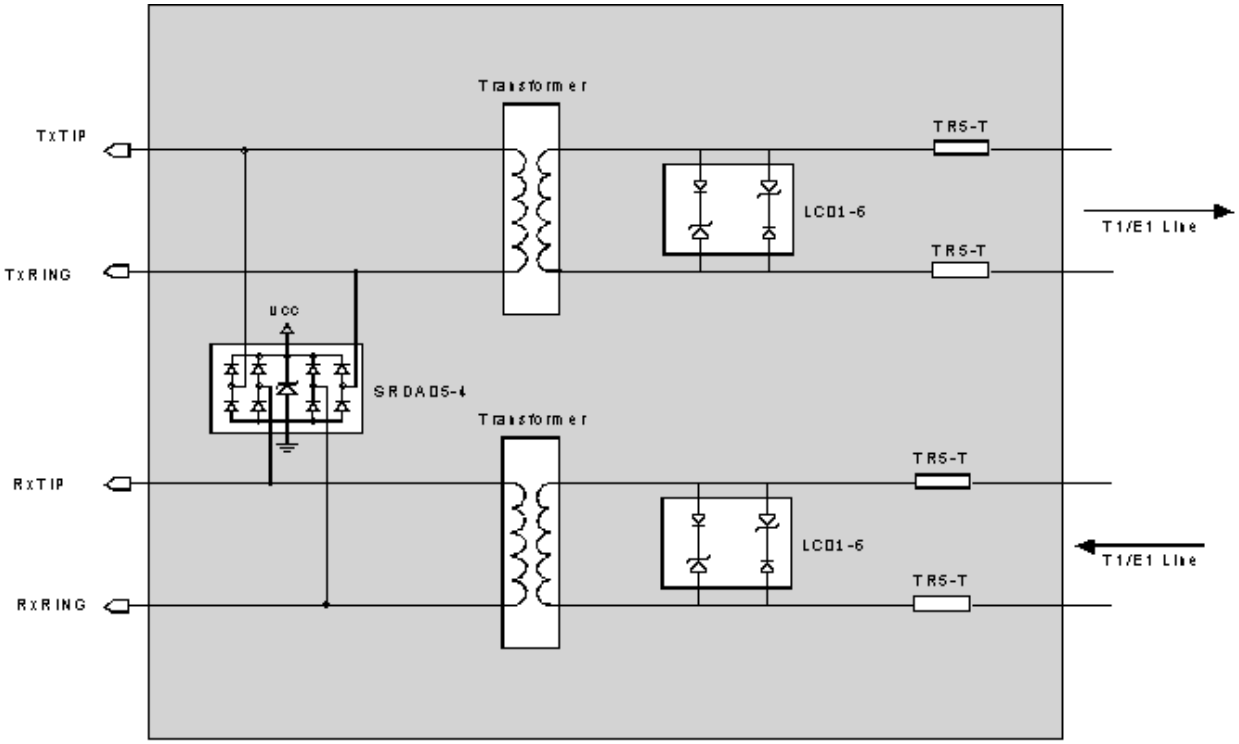


Table 13 Protection Circuitry

Component	Description	Part	Manufacturer
U10, U14-20	6V, TVS diode	LC01-6	SEMTECH
TR1-TR16	PTC	TR250-180U	Raychem
U21-24	5V, Surge Rated Diode Array	SRDA05-4	SEMTECH

The LC01-6 is a low capacitance, surface mount, transient voltage suppressor. This device is designed to protect high speed communication lines from voltage surges caused from electrostatic discharge, electrical fast transients, and induced lightning.

The PTCs provide the 120V intra-building AC power cross protection required for customer premises equipment.

The SRDA05-4 provides voltage clamping within ± 300 mV of 5V without distorting the output pulse shape.

3.5.2 Resistor Population Options

Certain passive circuit elements of the TQUAD/EQUAD with QDSX reference design are specific to either T1 or E1 operation. Table 14 shows the differences in the passive circuit elements of the two modes.

Table 14 Resistor Population Options

Resistor	T1 Mode (Ω)	E1 Mode (Ω)
R11, R30, R32, R34	22	47
R9, R15, R16, R17	0	2.7
R21, R22, R24, R26	309	357
R10, R12, R13, R14	93.1	121
R73	4.7k	not populated
R74	not populated	4.7k

3.6 Power and Ground Connections

The TQUAD/EQUAD with QDSX reference design card requires a +5V power supply. This power may be supplied by the PM1501 EVMB via the microprocessor interface connector or by an external power supply. Solder bridges are provided to allow connection to the EVMB's power supply.

3.7 Crystal Clock

This clock provides timing for many portions of the TQUAD/EQUAD and the QDSX. The high-speed timing for the TQUAD and QDSX combination is sourced from a 37.056 MHz crystal oscillator. The high-speed timing for the EQUAD and QDSX combination is sourced from a 49.152 MHz crystal oscillator.

3.8 Oscillator Y2

This oscillator provides an 2.048MHz clock to the FPGA. It is a clock source that provides extra timing options on the TQUAD/EQUAD with QDSX reference design. This clock may be selected and routed, by the FPGA, to the system side of the TQUAD/EQUAD.

3.9 FPGA

The ACTEL A1460A FPGA provides a PRBS generator, loopback capabilities, logic for alarm LEDs, and several timing options. The code for the FPGA is provided in Appendix D.

3.9.1 Minimum Requirements

The system loopback functions, provided by the FPGA, must be programmed to use the TQUAD/EQUAD with QDSX reference design. The backplane signals that must be looped back are described in the following paragraphs.

BRPCM[4:1] are the backplane receive PCM serial data streams. These signals must be looped back to BTPCM[4:1].

BRSIG[4:1] are the backplane receive Signaling serial data streams which indicate the extracted robbed-bit signaling information of each PCM timeslot on BRPCM[4:1]. These signals must be looped back to BTSIG[4:1].

The FPGA must select a 1.544 MHz/2.048 MHz clock source for BRCLK to time the receive section. BRCLK is common to all four framers. The TQUAD/EQUAD may be configured to ignore the BRCLK and use the RCLKO[4:1] signal in its place when the Elastic Store is bypassed.

A suitable framing pulse must be generated by the FPGA to frame align the received data to the system backplane. A pulse at least 1 BRCLK cycle wide must be provided on BRFPI every 256 bit periods. BRFPI is common to all four framers.

BRFPO[4:1] must be looped back to the BTFP[4:1]. BRFPO[4:1] indicates the frame alignment of the BRPCM[4:1] data

A 1.544 MHz/2.048 MHz clock must be provided to the BTCLK[4:1] to provide timing to the transmit section of the TQUAD/EQUAD. Other timing options may be selected in the FPGA but are not required for the operation of the TQUAD/EQUAD with QDSX reference design. Additional timing options are described in the Timing Options section.

3.9.2 Additional Features

A PRBS data generator has been provided to facilitate line side loopbacks. The PRBS pattern generated is 2^{23}-1.

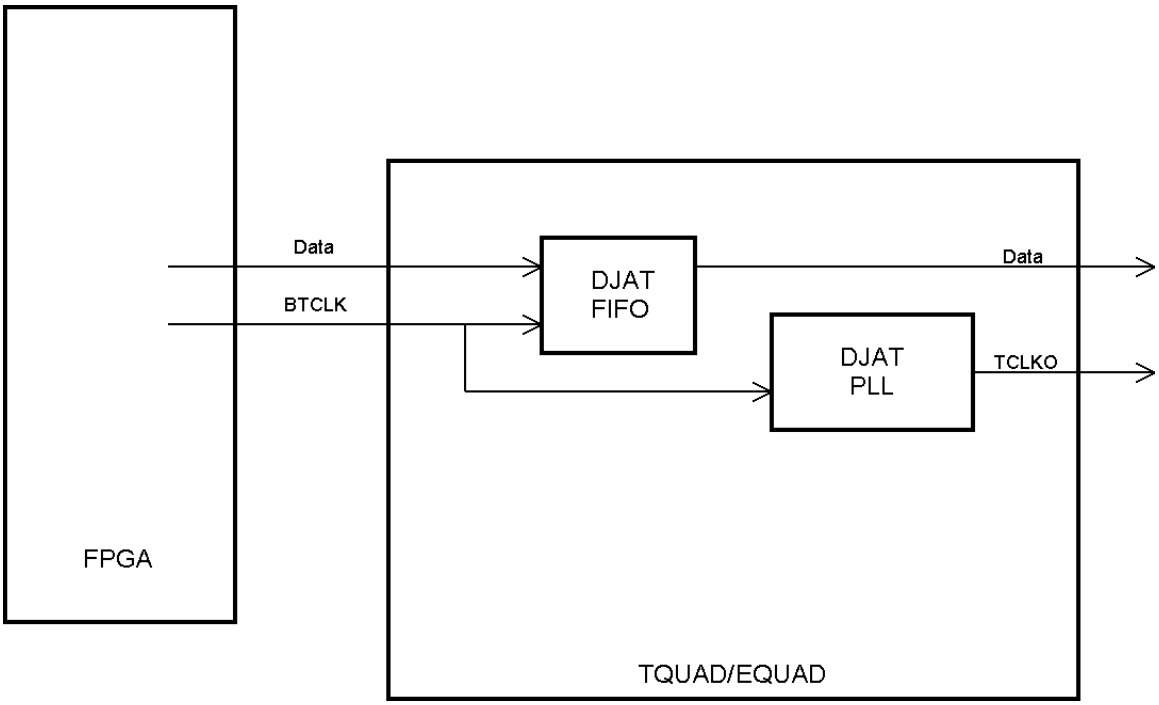
The FPGA provides timing options such as Flow Through Timing, Common Backplane Timing, and External Timing.

3.9.3 Timing Options

The FPGA provides timing options such as Flow Through Timing, Common Backplane Timing, and External Timing.

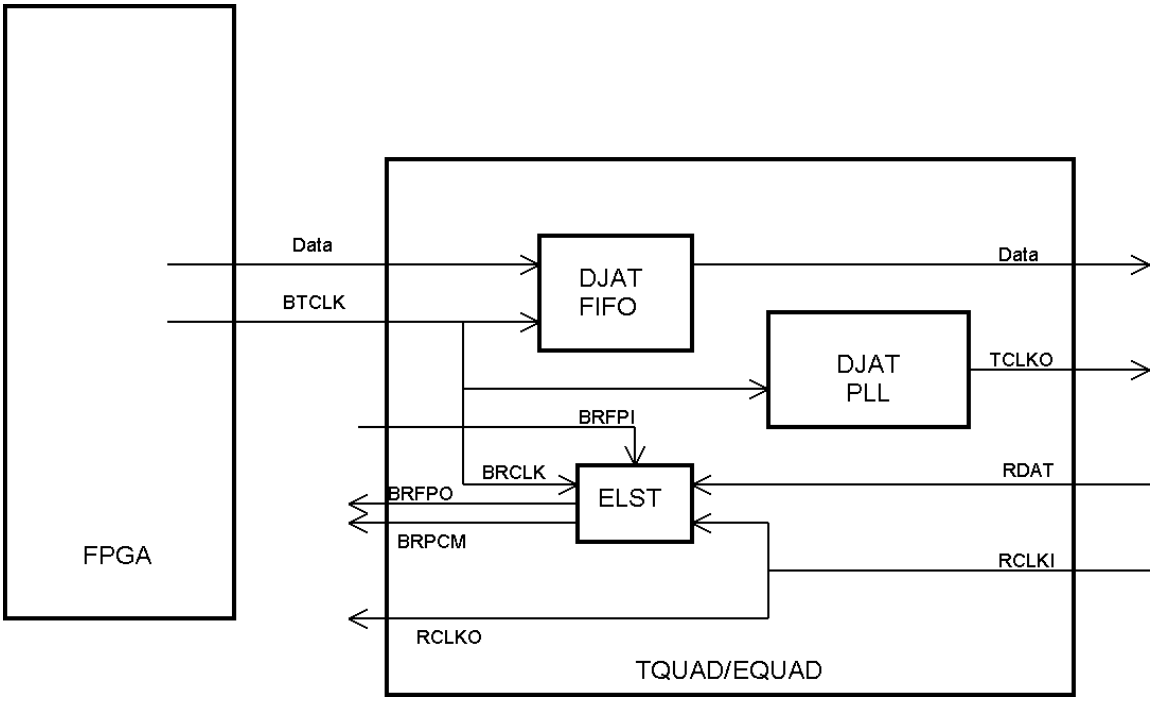
Flow Through Timing uses the 1.544/2.048 MHz clock to source timing for the BTCLK[4..1]. The data streams are stored in the FIFO timed to the BTCLK[4..1]. The BTCLK[4..1] is received by the Jitter Attenuator, where the BTCLK[4..1] is smoothed out, and transmitted as TCLKO[4..1]. Flow Through Timing is shown in Figure 5.

Figure 5 Flow Through Timing



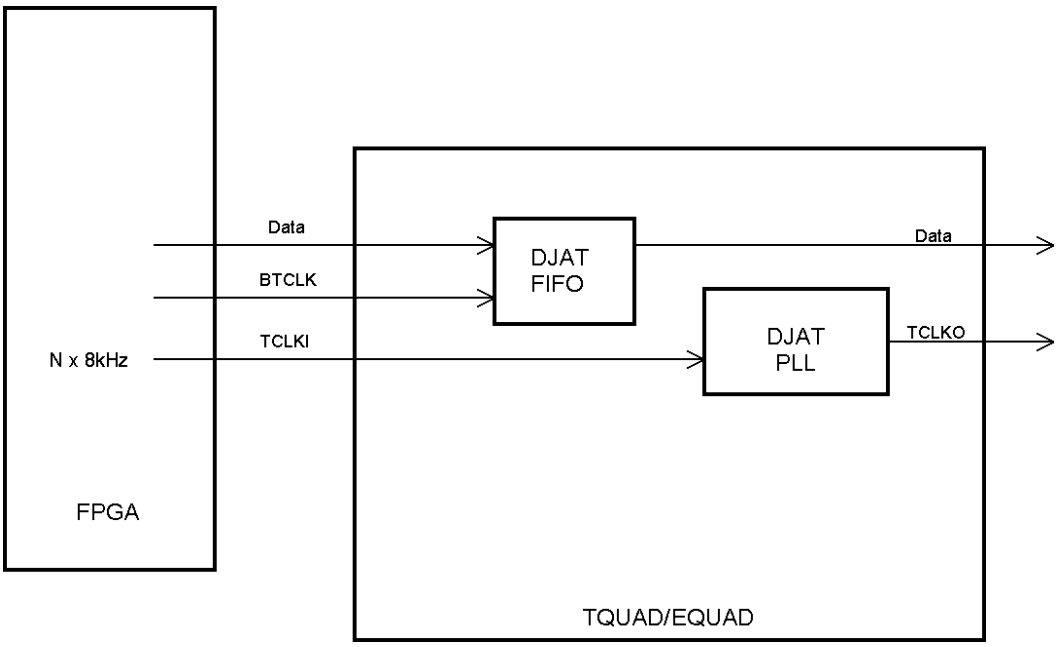
Common Backplane Timing is similar to Flow Through Timing except it uses the same clock to time BTCLK and BRCLK. It allows for use of the 2.048MHz oscillator for timing the backplane (T1 mode only). Common Backplane Timing is shown in Figure 6.

Figure 6 Common Backplane Timing



External Timing facilitates the use of any N*8 kHz external clock, where N is an integer, to generate the TCLKO[4..1] clock signal. Provided TCLKI[4..1] is jitter free when divided down to 8 kHz, then it is possible to derive TCLKO[4..1] from TCLKI[4..1] when TCLKI[4..1] is a multiple of 8 kHz. The specified maximum frequency for TCLKI[4..1] is 3.096 MHz. External Timing is shown in Figure 7.

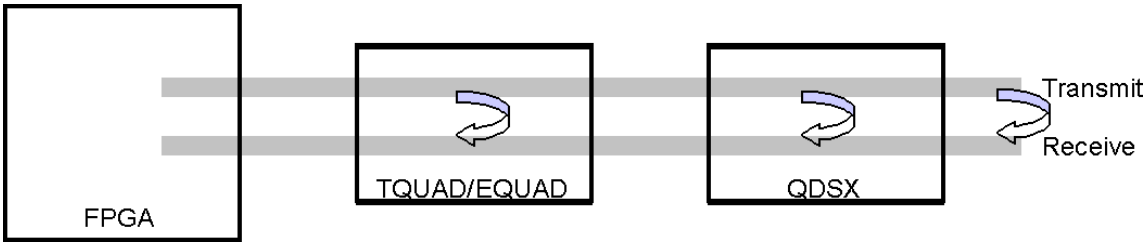
Figure 7 External Timing



3.9.4 Loopbacks

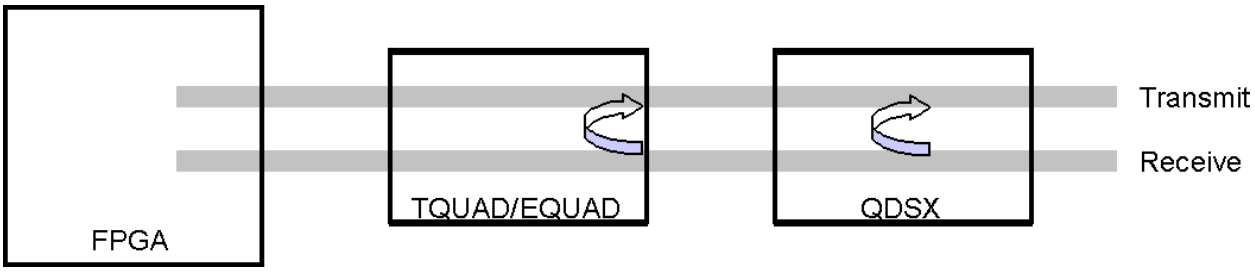
Three diagnostic loopbacks are available to aid in network diagnostics and problem isolation. Data generated in the FPGA can be looped back via the TQUAD/EQUAD, QDSX, or physically via the cable. Diagnostic loopbacks are shown in Figure 8.

Figure 8 Diagnostic Loopbacks



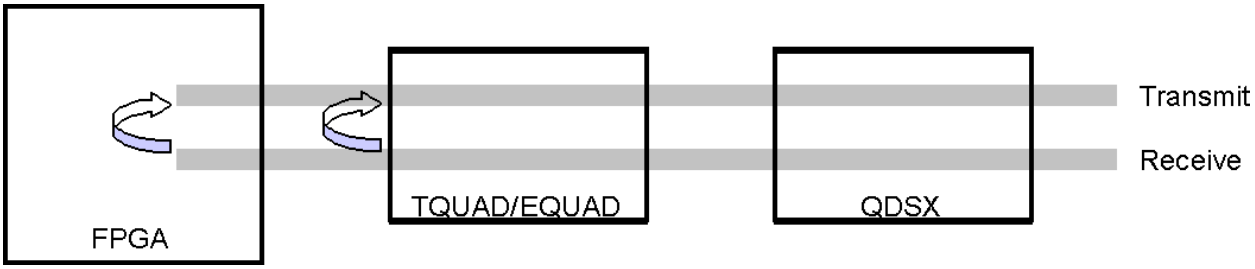
Also, two line side loopbacks, as shown in Figure 9, are available for looping back external data. External data can be looped back via the TQUAD/EQUAD or QDSX.

Figure 9 Line Side Loopbacks



As well, two backplane loopbacks are available, as shown in Figure 10. Data can either be looped back via the TQUAD/EQUAD or FPGA.

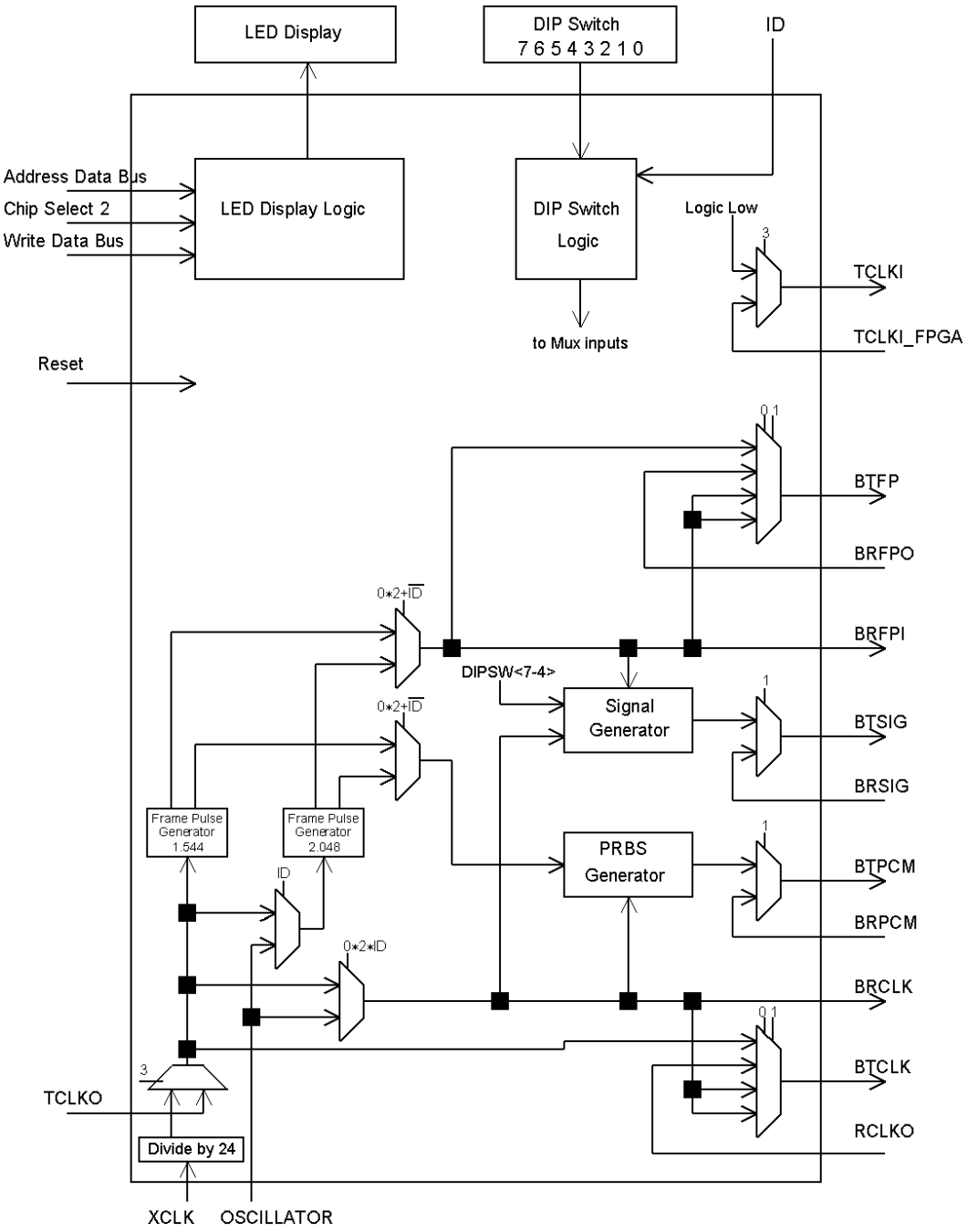
Figure 10 Backplane Loopbacks



3.9.5 VHDL Code

The FPGA must be able to loopback data streams, signaling, frame pulses, and clocks. These loopbacks are required for the TQUAD/EQUAD with QDSX reference design to work properly. Additional features have been designed into the FPGA which allow the user to obtain access to the many features of the TQUAD and EQUAD. VHDL, a hardware description language, has been used to create the digital circuit used inside the FPGA. A block diagram of the VHDL code is shown in the following figure.

Figure 11 Digital Circuit in FPGA



The XCLK, a 37.056/49.152 MHz clock for T1/E1 respectively, is divided by 24 to produce a suitable clock for timing the receive section of the TQUAD/EQUAD.

The divided clock is also required to generate a framing pulse used in the receive section for frame alignment. The frame pulse is output once every 256 clock cycles for the EQUAD, or once every 193 clock cycles for the TQUAD (thus always producing an 8kHz pulse).

DIP Switch 0 is used to select between timing options. A '0' selects Flow Through Timing and a '1' selects Common Backplane Timing.

A 2^{23}-1 PRBS generator allows the TQUAD/EQUAD with QDSX reference design to loopback the line side T1/E1 signals. The PRBS generator is selected by DIP Switch 1. A '0' selects the receive data, from BRPCM, to be sent to the transmit section, whereas a '1' selects the PRBS data to be sent to the transmit section.

DIP Switch 2 is used when the auxiliary oscillator is installed on the board (2.048MHz), in order to time the backplane to it. This feature is only available when using Common Backplane Timing (DIP Switch 0 set to '1').

DIP Switch 3 is used to set TCLKI to either an external oscillator or to hold it low.

DIP Switches 4 through 7 are the signaling bits of the backplane. They are converted to serial form within the FPGA and put out on the backplane.

Some extra logic is provided to enable microprocessor control of an on board LED display. When chip select 2 and write data byte signals are low and make the transition to high, the data on the multiplexed address-data bus is clocked into flip flops. When a '0' value is clocked into the flip flop, the LED in question turns on. A '1' must be clocked to turn the LED off.

The code for the FPGA is provided in Appendix D: VHDL Code.

3.10 Alarms

An on-board LED display is available to indicate the status of four alarm conditions: RED Alarm, Alarm Indication Signal (AIS), Out Of Frame (OOF), and Remote Alarm Indication (RAI). The LED display is intended to be controlled by the microprocessor via communication with the FPGA, however the code for this has not been developed at this time. Table 15 shows the intended LEDs and their corresponding alarms.

Table 15 LED Display

LED	Alarm Condition
1	RED Alarm
2	Alarm Indication Signal
3	Out Of Frame
4	Remote Alarm Indication
5	Spare
6	Spare

3.10.1 EQUAD Alarms

The EQUAD supports the detection of various alarm conditions such as loss of signal, loss of frame, loss of signaling multiframe, loss of CRC multiframe, reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and timeslot 16 alarm indication signal. The EQUAD detects and indicates the presence of remote alarm and AIS patterns, and also integrates Red and AIS alarms as per industry specifications.

3.10.2 TQUAD Alarms

The TQUAD supports the detection of various alarm conditions such as Loss of Signal, Pulse Density Violation, Red Alarm, Yellow Alarm, and AIS alarm. The TQUAD detects the presence of Yellow and AIS patterns and integrates Yellow, Red and AIS alarms as per industry specifications.

3.10.3 Interrupts

The only efficient way of processing events that may have a low frequency of occurrence is to use interrupt driven routines (instead of polling). The events (alarm conditions, timers, datalink servicing) on the TQUAD/EQUAD with QDSX reference design will, on average, be low frequency.

When the host microprocessor detects an interrupt indication on its external interrupt input pin, it must determine the source of the interrupt. The microprocessor polls the TQUAD/EQUAD and the QDSX to determine the source of the interrupt. Then the appropriate device’s registers must be polled to determine the event that caused the interrupt.

Once the interrupt source has been determined, the microprocessor can jump to a routine specific to that interrupt. The code has not been developed for interrupt handling as of this document's release date.

4 LAYOUT DESCRIPTIONS

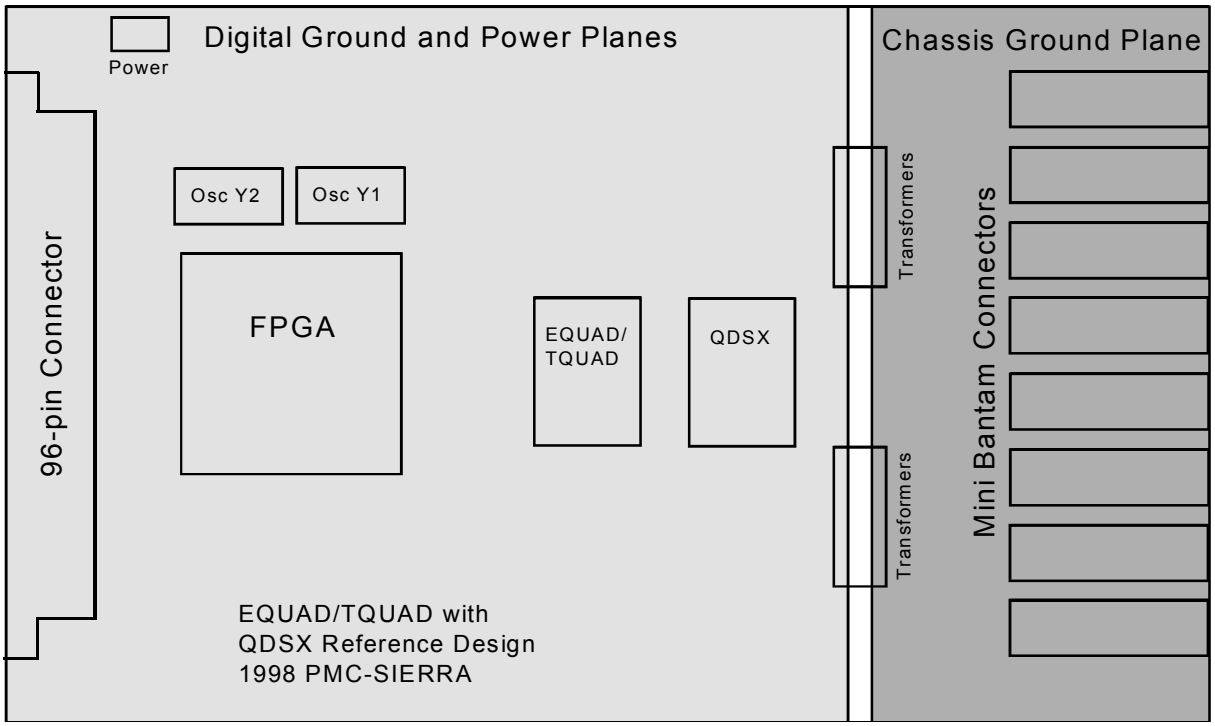
4.1 Component Placement

The overall placement strategies of the components are:

- Place the analog circuitry away from the digital circuitry.
- Keep the transformers as close to the bantam connectors as possible. This will insure that the transformer suppresses the common-mode noise riding on the traces coming from the connectors before it can radiate.

The overall placement is as follows:

Figure 12 Main Component Placement Diagram



In addition, the following rules are used:

- Noise on an oscillator's power supply will cause jitter on the output, and therefore the oscillators are placed in a quiet digital section. The oscillator itself generates noise that may affect sensitive analog circuits. The oscillators will be placed along the top of the board near the power supply where there is

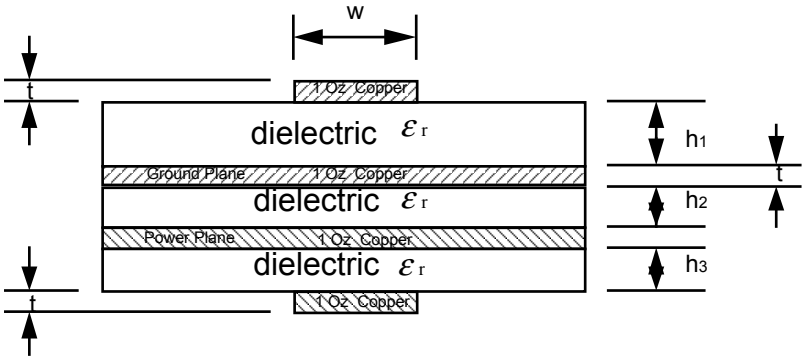
clean power and so that return currents are not running underneath any sensitive circuitry.

- All source termination resistors are placed near the outputs and load termination resistors are placed near the inputs. There are only a few high speed lines on the board that require controlled impedance traces and terminations.
- All pull down resistors are placed near the output pins.
- All decoupling capacitors are placed near the power supply pins. The bulk decoupling capacitors are placed near the power entrance, specifically the upper left corner.

4.2 Layer Stacking and Transmission Line Impedance Control

The TQUAD/EQUAD Reference Design card has four layers: layers 1 and 4 for signals, layer 2 for ground, and layer 3 for power. The layer configurations are shown below:

Figure 13 PCB Cross Section



where

ε_r = relative dielectric constant, nominally 5.0 for G-10 fibre-glass epoxy

t = thickness of the copper, fixed according to the weight of copper selected. For 1 oz copper, the thickness is 1.4 mil. This thickness can be ignored if w is great enough.

h1, h2, h3 = thickness of dielectric.

w = width of copper

The PCB related parameters are shown in the following table:

Parameters	Nominal
Board Thickness (mil)	62 (including copper thickness)
dielectric thickness between layers 1 and 2 (mil) (h1)	10
dielectric thickness between layers 2 and 3 (mil) (h2)	33
dielectric thickness between layers 3 and 4 (mil) (h3)	10
Relative dielectric constant	4.2

To reduce signal degradation due to reflection and radiation, the traces that carry high speed signals should be treated as micro strip transmission lines with controlled impedance and matched resistive termination. The trace impedance is calculated using the formula:

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

Parameter	Data
ε_r	4.2
h1 (mil)	10
t (mil, 2 Oz copper)	2.88
Zo (Ω)	50
W (mil)	16

Given a characteristic impedance Zo, the dielectric thickness h1 is proportional to the trace width. A small h1 will result in the traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board for a given trace impedance and adequate trace width should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication.

For example, using the same dielectric thickness, copper trace thickness, and dielectric constant, a 16 mil trace has a characteristic impedance of approximately 50 Ohms while a 6 mil trace has a characteristic impedance of 75 Ohms.

4.3 Power and Ground

A ground plane and power plane cover the entire board, except for the line interface area. The introduction of ground slots within the ground plane must be

avoided as they will increase trace inductance and increase crosstalk. These slots can be accidentally created by making clear-out holes too large.

The line interface area that connects the bantam connectors to the transformers has its own separate chassis ground plane. This chassis ground plane is formed on the same layer of the board as the main ground and power plane, except is separated from these planes in an entire section of the board, underneath the transformers. Signals will not cross from one ground plane to another, except across the transformers. This setup isolates the T1/E1 lines from the rest of the board.

The placement of the digital ground and power planes, as well as the chassis ground plane, can be seen in Figure 12.

4.4 Routing

- All power and ground traces are as wide and short as possible to minimize trace inductance.
- All high speed traces are routed over continuous image planes (power or ground planes).
- All traces carrying transmit and receive line rate data should be routed on the same side and kept as short as possible.
- Both signals of a differential pair are of equal length and routed close to each other.

5 REFERENCES

1. PMC-Sierra, PMC-910501, “PMC Device Evaluation Motherboard Engineering Document”, May 1991, Issue 3

2. PMC-Sierra, PMC-950857, Data Book (Issue 4), “PM4314 QDSX Quadruple T1/E1 Line Interface Device”

3. PMC-Sierra, PMC-940910, Data Book (Issue 5), “PM4344 TQUAD Quadruple T1 Framer”

4. PMC-Sierra, PMC-951013, Data Book (Issue 4), “PM6344 EQUAD Quadruple E1 Framer”

APPENDIX A: BILL OF MATERIALS

NO.	COMPONENT DESCRIPTION	Package Type	REF DES	Qty
1	49FCT805_SOIC-BASE	SOIC20W	U6	1
2	74HC04BLK_SOIC-BASE	SOIC14	U12	1
3	74XXX00_SOIC-HCMOS	SOIC14	U11	1
4	74XXX138_SOIC-HCMOS	SOIC16	U3	1
5	74XXX139_SOIC-HCMOS	SOIC16	U4	1
6	74XXX245_SOIC-HCMOS	SOIC20W	U2	1
7	74XXX541_SOIC-HCMOS, 74HC541	SOIC20W	U1, U7	2
8	A1460-208	PQFP208	U9	1
9	BANTAM-BASE	BANTAM	J17-J24	8
10	CAPACITOR POL-10UF, 16V, TANT THE	SMDTANCAP_C	C16	1
11	CAPACITOR-0.001UF	SMDCAP805	C40-C42, C45	4
12	CAPACITOR-0.01UF, 50V, X7R_805	SMDCAP805	C17-C33, C70, C73, C75, C77, C79, C96	23
13	CAPACITOR-0.047UF, 50V, X7R_1206	SMDCAP1206	C12-C15	4
14	CAPACITOR-0.1UF, 50V, X7R_1206	SMDCAP1206	C1-C7, C38, C39, C43, C44, C46-C55, C61-C68, C93	30
15	CAPACITOR-0.47UF, 25V, TANT TEH	SMDTANCAP_A	C8-C11	4
16	CAPACITOR-0.68UF, 35V, TANT TEH	SMDTANCAP_B	C34-C37	4
17	CAPACITOR-1UF, 16V, TANT TEH	SMDTANCAP_A	C71, C72, C74, C76, C78, C80	6
18	CAPACITOR-47UF, 10V, TANT TEH	NEC_D	C94	1
19	DIN96_MALE-BASE	AMP_650473-5	P2	1

20	DIPSW8-BASE	DIP16	SW1	1
21	EQUAD-BASE	PQFP128	U8	1
22	FUSE__SMD-3.000A, NANO	NANO_SMF	F1	1
23	HEADER2_JUMPER-BASE	JUMPER2	J2	1
24	HEADER5_100 MIL-BASE	SIP5	J1	1
25	LC01_6_SOIC-BASE	SOIC16WB	U10, U14-U20	8
26	LED-SUPER_GREEN, SURFACE MOUNT	LED_11	D1-D7	7
27	OSC_TTL_DIP-2.048MHZ , 50 PPM, CHA	CRYS14	Y2	1
28	OSC_TTL_DIP-49.152MH Z, 32/50 PPA	CRYS14	Y1	1
29	PWRBLOCK_2-BASE	CONN2END	P1	1
30	QDSX-BASE	PQFP128	U5	1
31	RESISTOR-100, 5%, 805	SMDRES805	R37-R43, R49	8
32	RESISTOR-10K, 5%, 805	SMDRES805	R1, R44, R53, R70	4
33	RESISTOR-121, 1%, 805	SMDRES805	R10, R12-R14	4
34	RESISTOR-2.7, 5%, 805	SMDRES805	R9, R15-R17	4
35	RESISTOR-316K, 1%, 805	SMDRES805	R3-R6	4
36	RESISTOR-330, 5%, 805	SMDRES805	R69	1
37	RESISTOR-357, 1%, 805	SMDRES805	R21, R22, R24, R26	4
38	RESISTOR-4.7K, 5%, 805	SMDRES805	R2, R18, R73, R74	4
39	RESISTOR-47, 5%, 805	SMDRES805	R11, R30, R32, R34	4
40	RESISTOR-49.9, 1%, 805	SMDRES805	R7, R8, R19, R20, R23, R25, R27-R29, R31, R33, R64	12
41	RESISTOR-75, 1%, 805	SMDRES805	R35, R36, R45-R48, R50-52, R54-63, R63-68, R71, R72	25
42	RES_ARRAY_15_SMD-10K	SOIC16	RN1, RN2	2

43	RES_ARRAY_8_SMD-10K	SOIC16	RN3	1
44	RES_ARRAY_8_SMD-330	SOIC16	RN5	1
45	RES_ARRAY_8_SMD-4.7K	SOIC16	RN4	1
46	SBRIDGE2	?	SB1, SB2	2
47	SRDA3_3_4	SOIC8	U21-U24	4
48	T1008-BASE	YB32	T1, T2	2
49	THERMISTOR	SMDRES805	TR1-TR16	16
50	TST_PT-BASE	TST_PT_1	TP1-TP6	6
51	TST_PT-BASE	TST_PT_1	TP21	1
52	TST_PT-BASE	TST_PT_1	TP22	1
53	ZENERDIODE-6.2V_1W	MLL41	D8	1

APPENDIX B: SCHEMATICS

REVISIONS				
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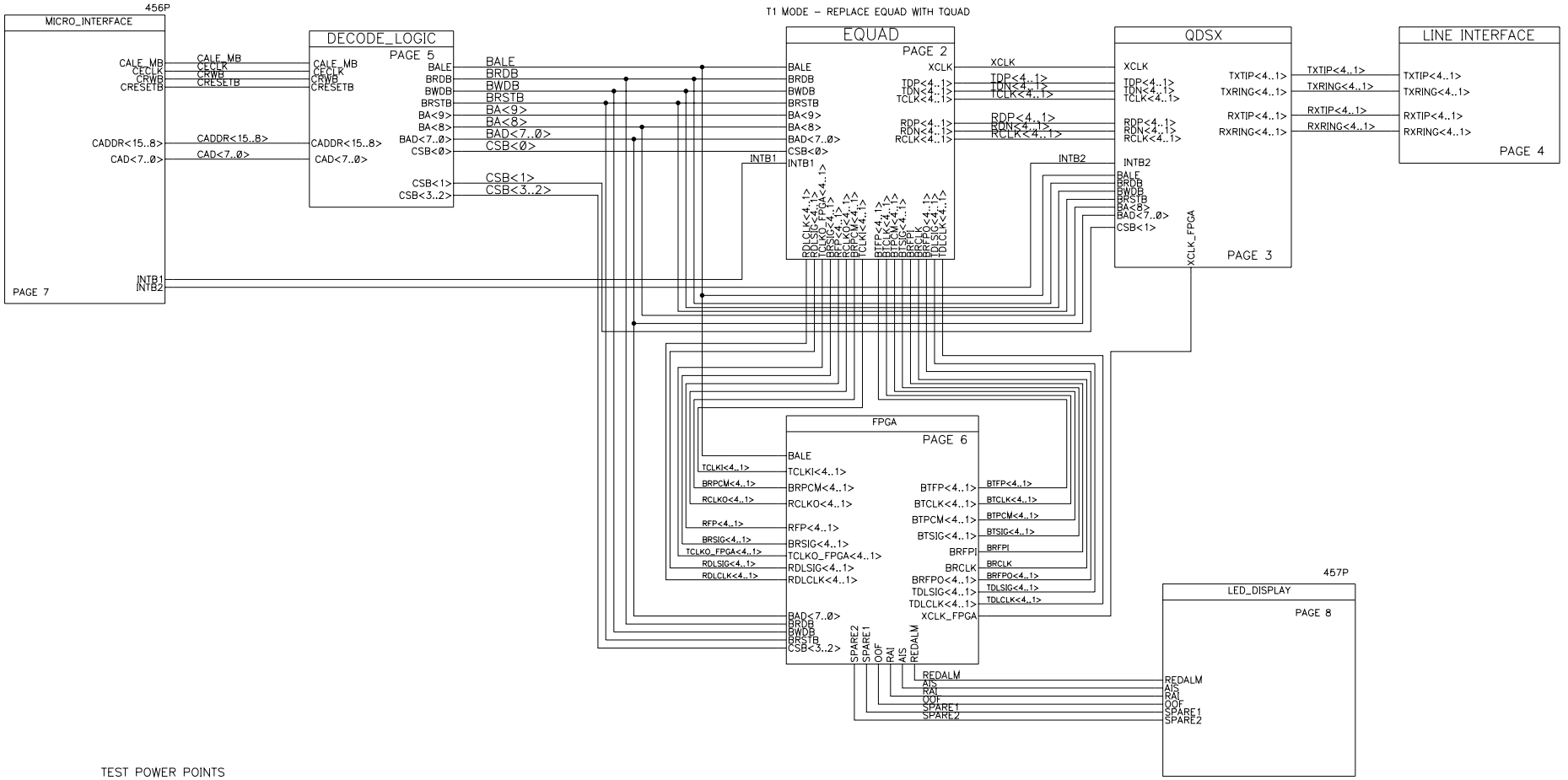
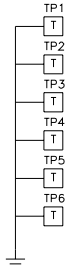


TEST POWER POINTS



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PMC-Sierra, Inc.

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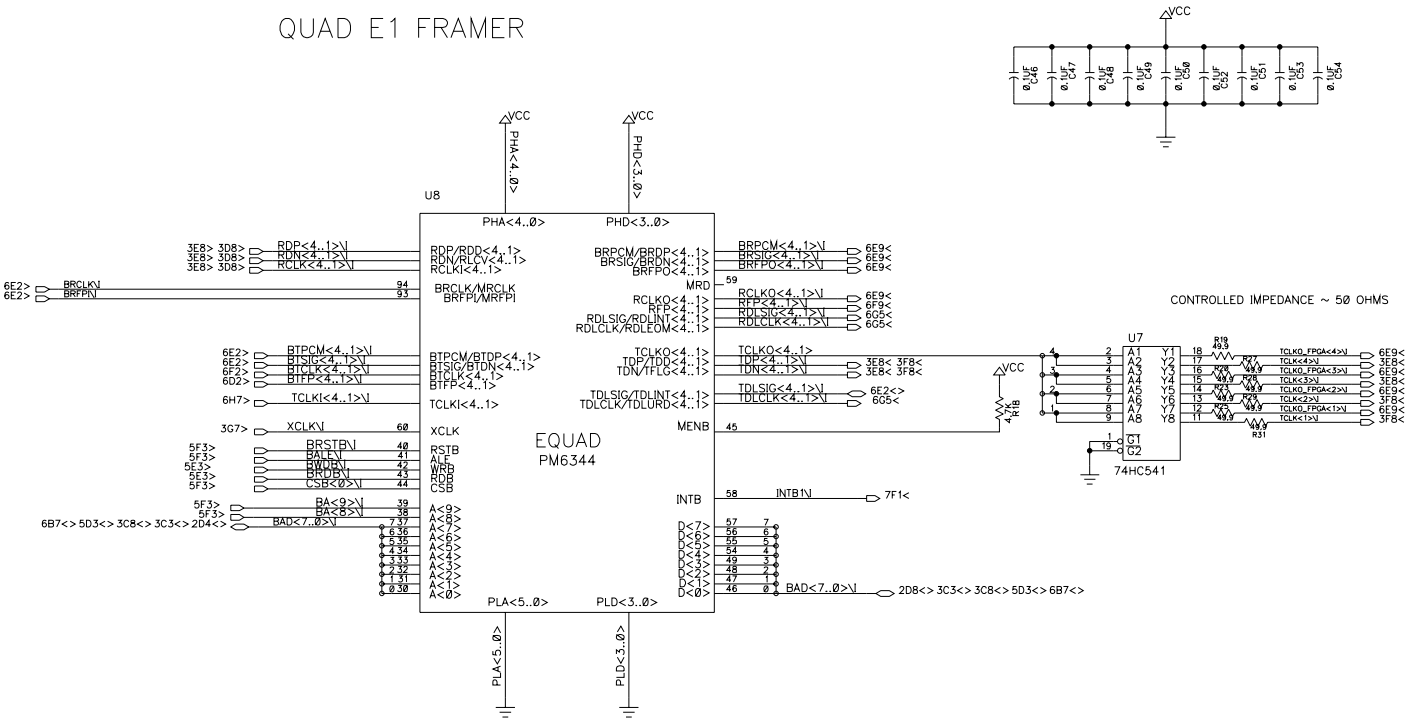
TITLE: TQUAD/EQUAD WITH QDSX REFERENCE DESIGN ROOT DRAWING	DATE: FEB 9,1998
ENGINEER: PMC-SIERRA, INC.	PAGE: 1 OF 8

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

NOTE: PLACE ALL DECOUPLING CAPS NEAR POWER PINS

QUAD E1 FRAMER



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ENGINEER: PMC-SIERRA, INC.	PAGE: 2 OF 8

REVISIONS				
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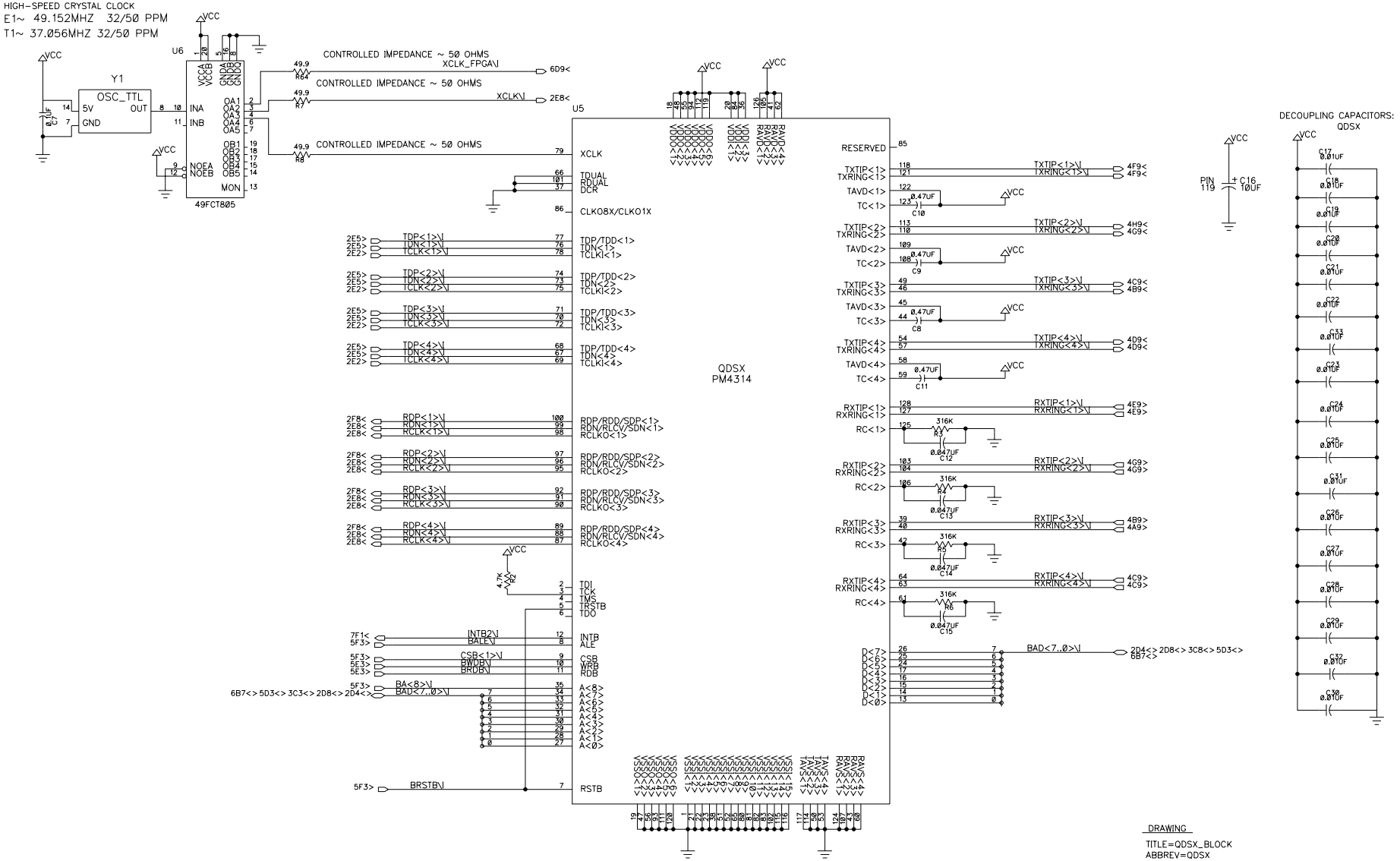
QDSX



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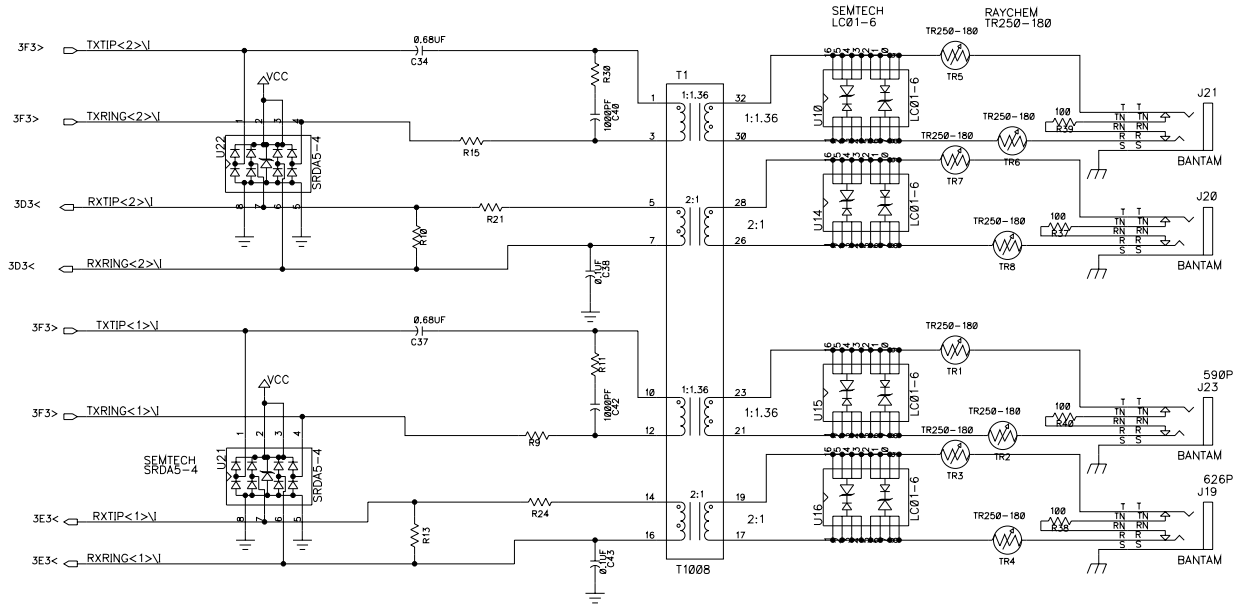
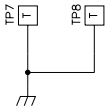
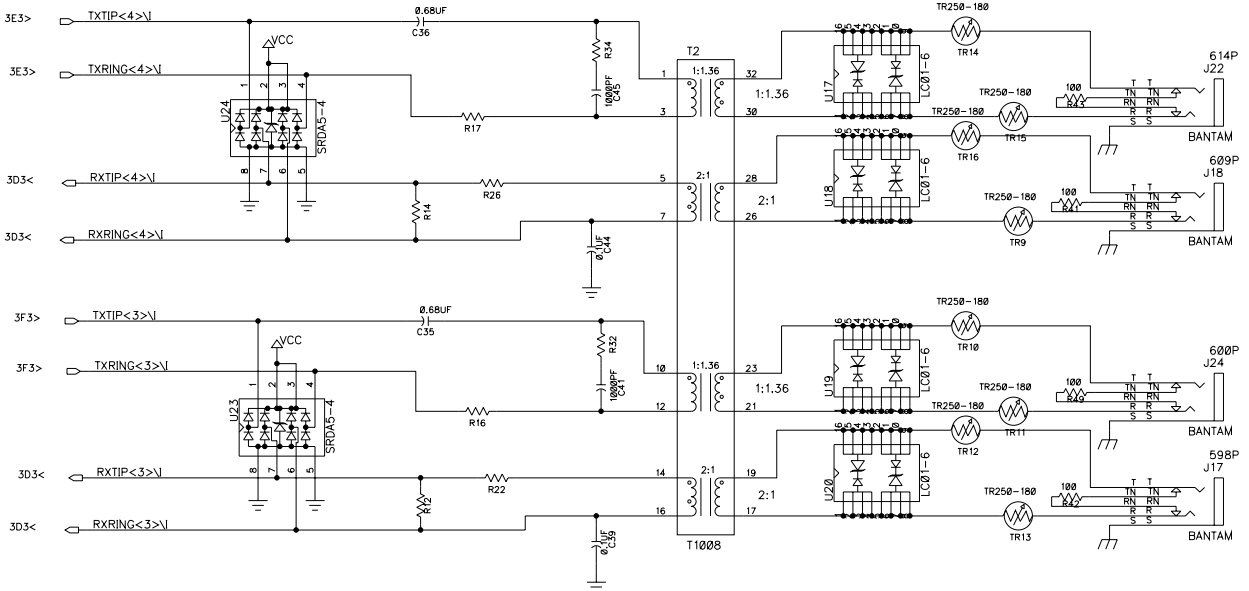


TABLE OF RESISTOR VALUES

RESISTOR	VALUE – E1	VALUE – T1
R11,R30,R32,R34	47	22
R9,R15,R16,R17	2.7	0
R21,R22,R24,R26	357	309
R10,R12,R13,R14	121	93.1



LINE INTERFACE TRANSMIT/RECEIVE



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ENGINEER: PMC-SIERRA, INC.	PAGE: 4 OF 8

REVISIONS				
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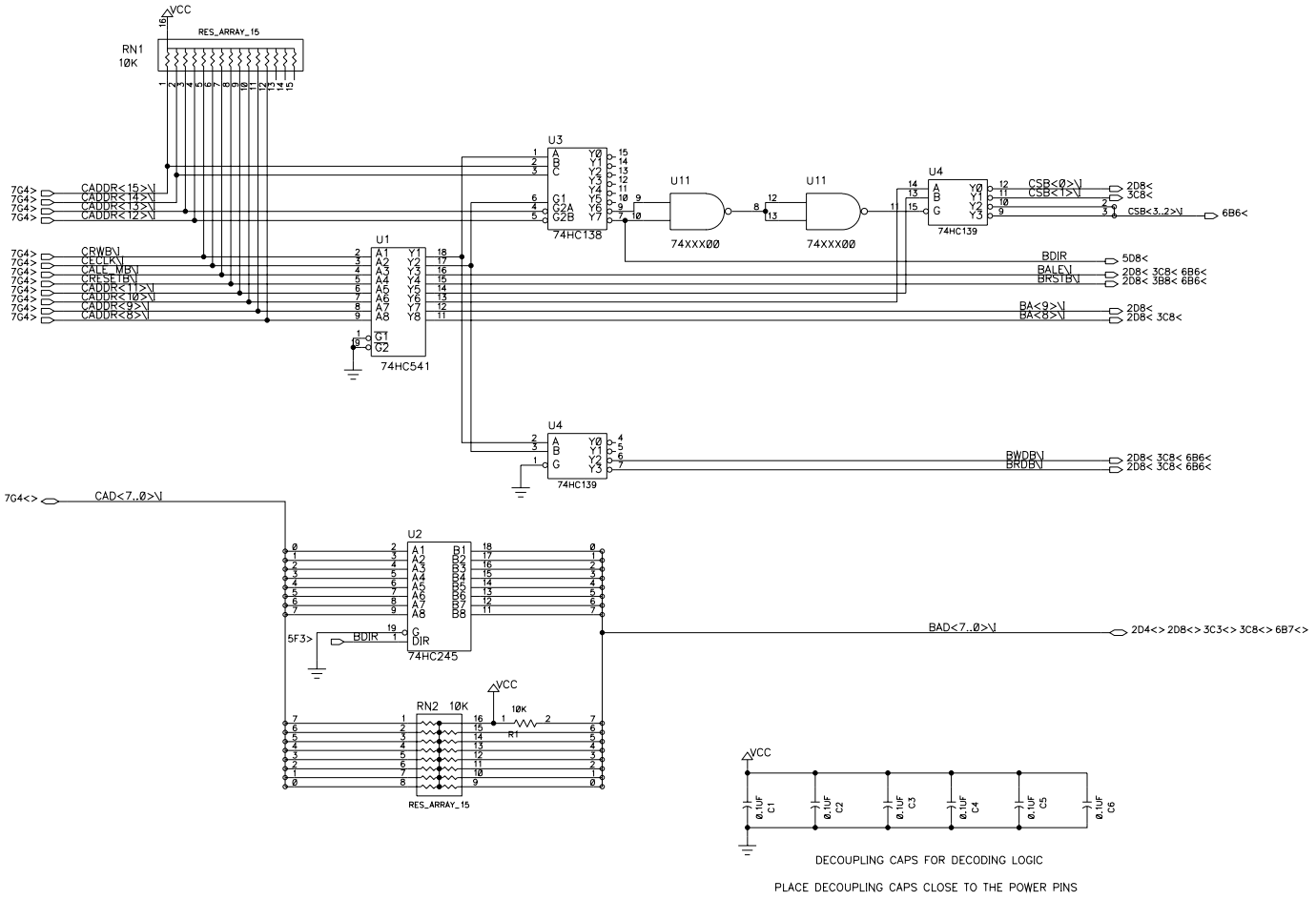

DECOUPLING CAPS FOR DECODING LOGIC

PLACE DECOUPLING CAPS CLOSE TO THE POWER PINS

DRAWING

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PMC-Sierra, Inc.

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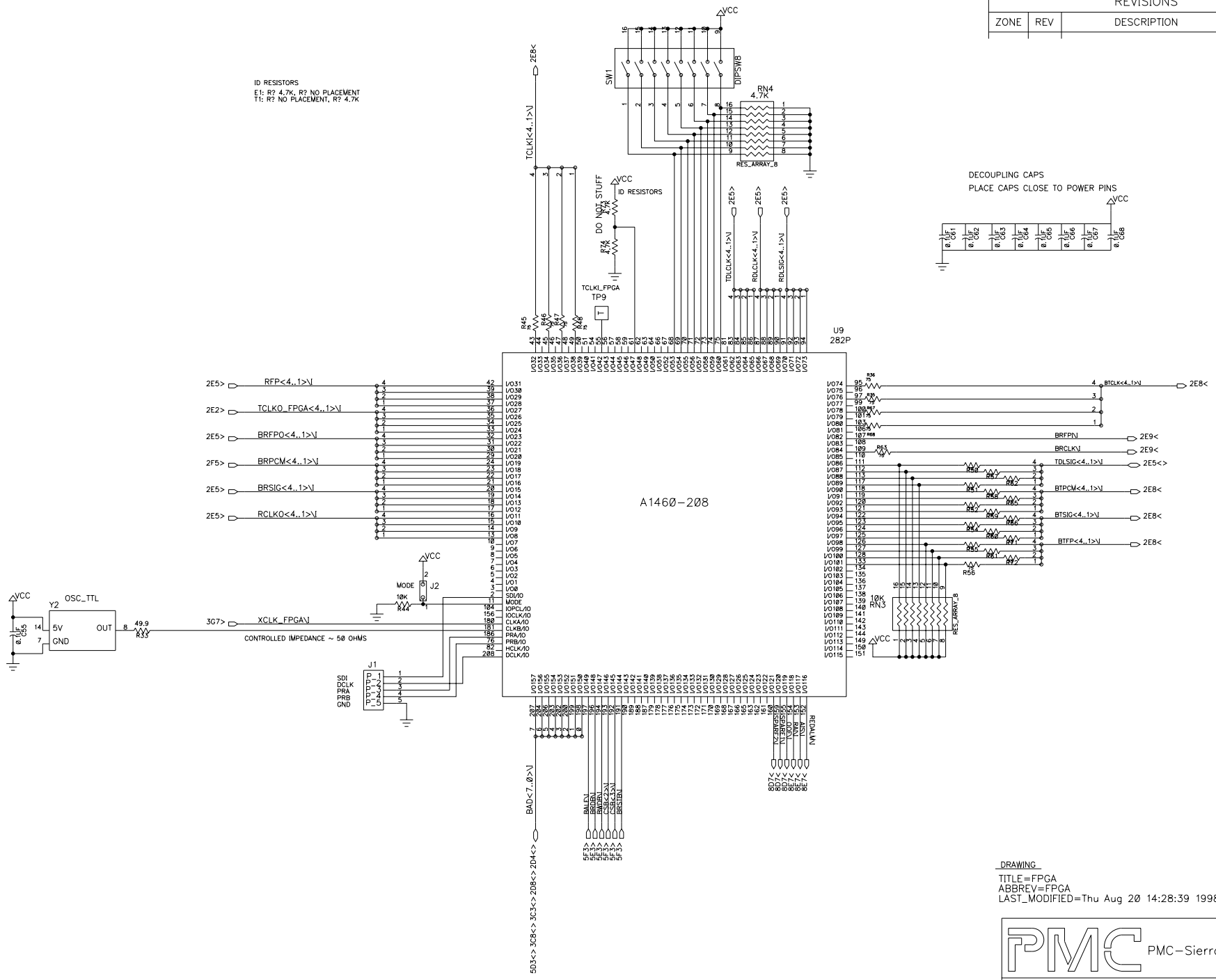
ENGINEER: PMC-SIERRA, INC.	PAGE: 5 OF 8

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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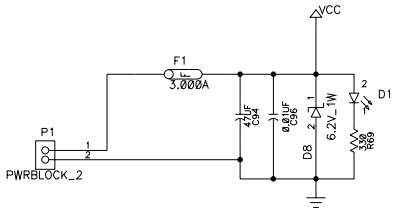
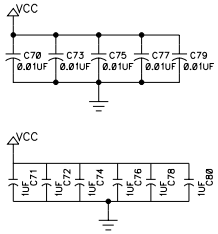
ENGINEER: PMC-SIERRA, INC.	PAGE: 6 OF 8

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

POWER



MIRCOPROCESSOR CONNECTOR



EXTRA DECOUPLING CAPACITORS

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PMC-Sierra, Inc.

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ENGINEER: PMC-SIERRA, INC.	PAGE: 7 OF 8

REVISIONS				
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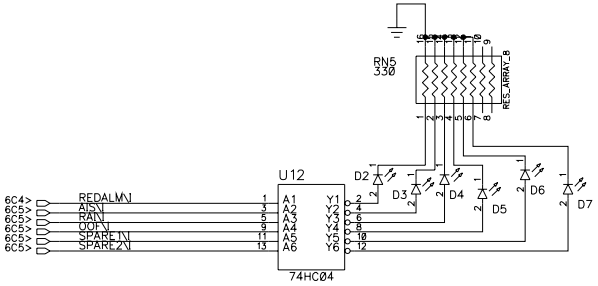

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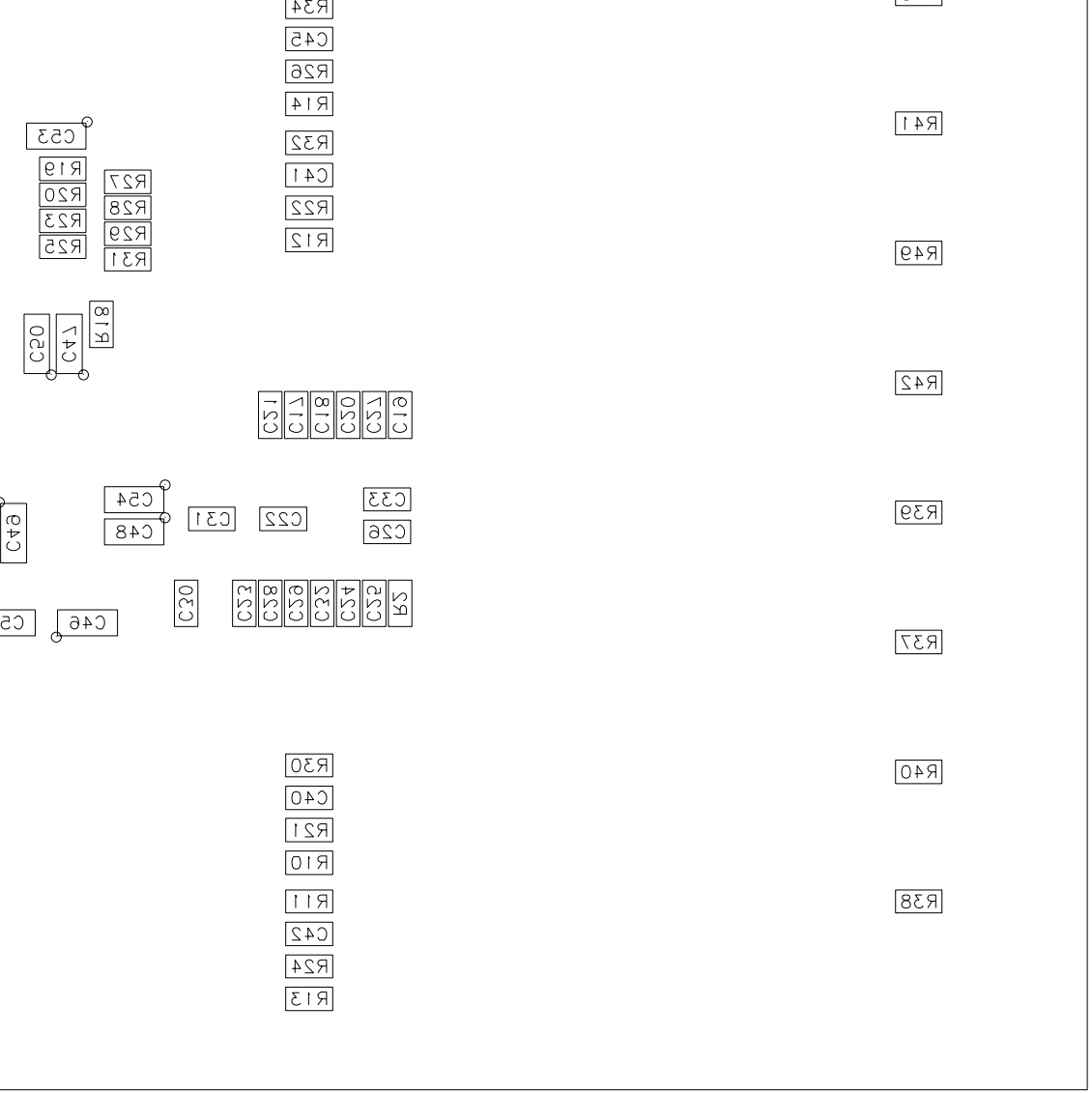
ENGINEER: PMC-SIERRA, INC.	PAGE: 8 OF 8

APPENDIX C: LAYOUT

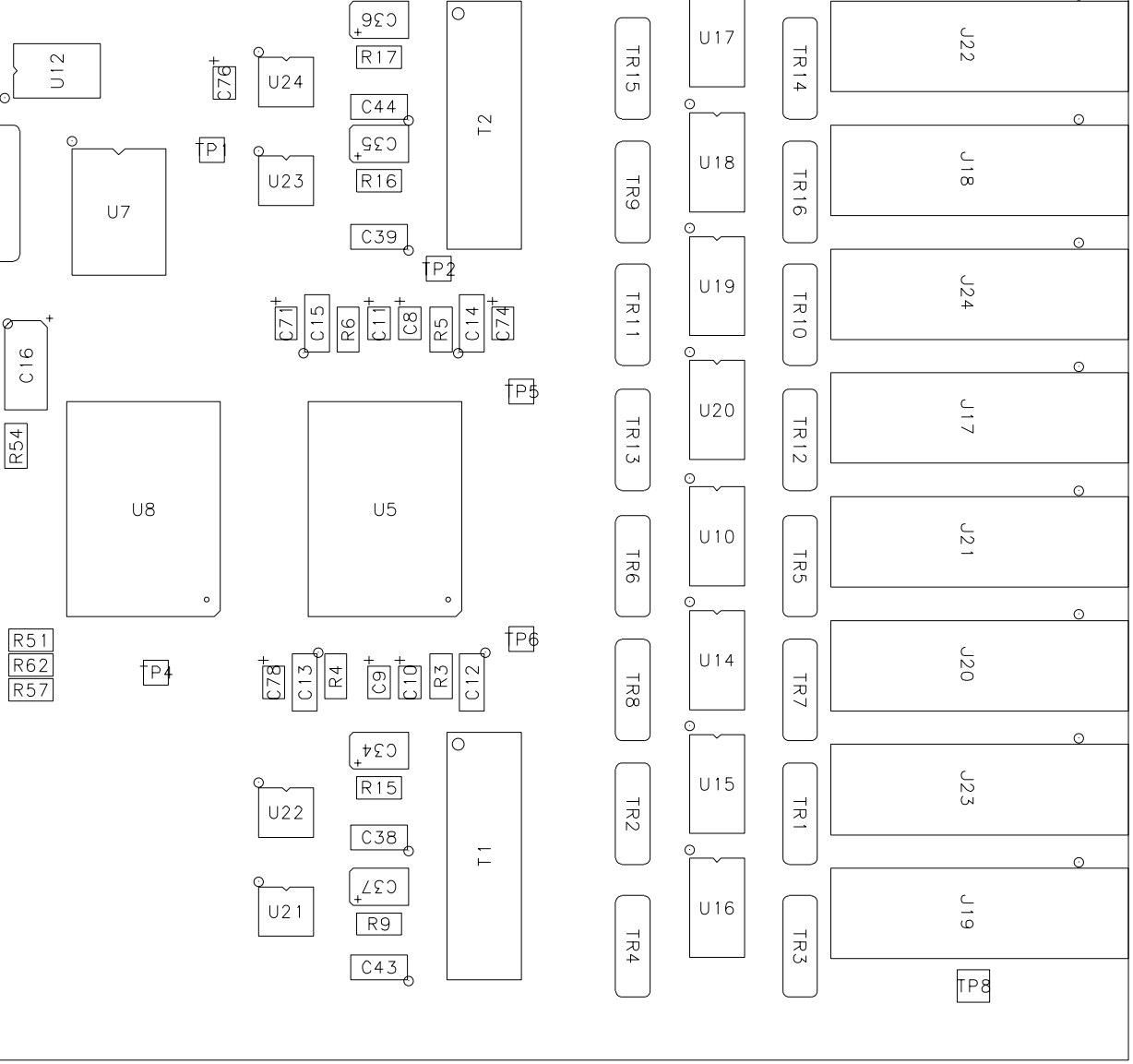


OM SOLDER SIDE

	DATE			DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SHOWN	
	Y	M	D	TOLERANCE (UNLESS OTHERWISE SHOWN)	.XX ± / .XXX ± / .XXXX ± / ANGLES ±
DRAWN PVM	98	06	26	CONFIDENTIAL - NOT FOR PUBLICATION THIS IS A CONFIDENTIAL DOCUMENT, AND IN ACCEPTING IT, THE RECIPIENT ACKNOWLEDGES THAT IT IS PROVIDED UNDER THE DISTINCT CONDITION THAT IT IS FOR HIS CONFIDENTIAL USE ONLY, AND THAT HE SHALL NOT ALLOW IT TO BE REPRODUCED OR ITS CONTENTS DISCLOSED IN ANY MANNER WHATSOEVER IN WHOLE OR IN PART WITHOUT SPECIAL PERMISSION IN WRITING FROM MPR Teltech Ltd.	
CHECKED					
ENGINEER AS				PACIFIC DESIGN ENGINEERING LTD.	
ENGINEER					
CHECKED				EQUAD/TQUAD ASSEMBLY DRAWING	
APPROVED					
APPROVED					
NEXT ASSEMBLY DWG.				DWG. No. PM4344	SIZE B
				SCALE NTS	SHEET 2 OF 2

7 8 9 10 11 12 13 14 15 16 17

C D E F G H J K L

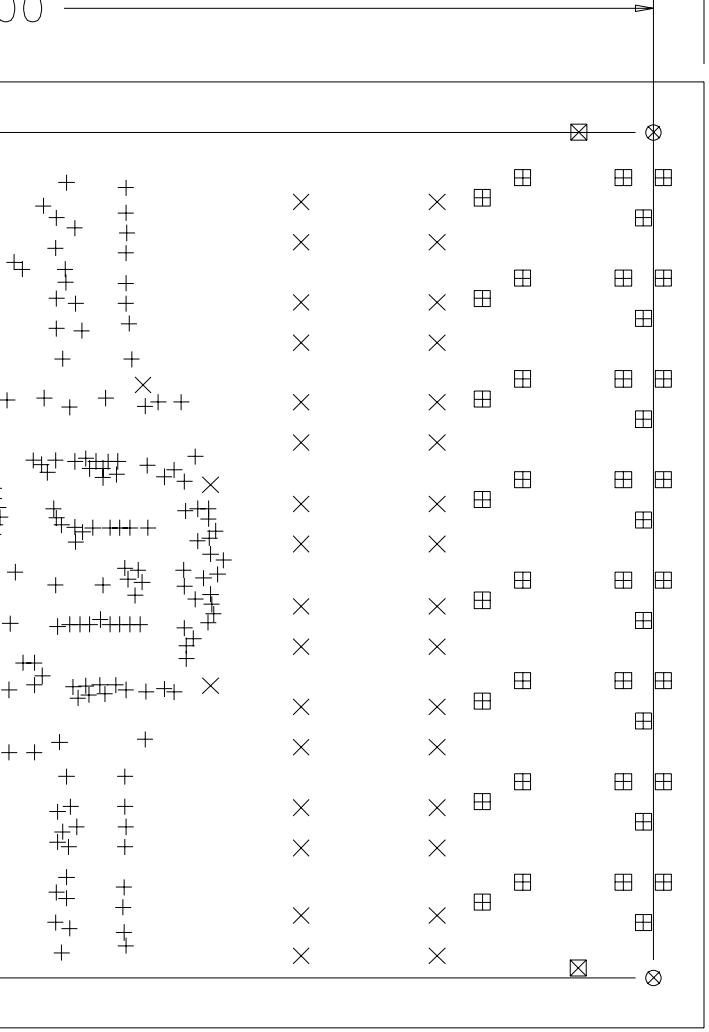


M COMPONENT SIDE

		DATE			DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SHOWN				
		Y	M	D	TOLERANCE (UNLESS OTHERWISE SHOWN)	.XX	.XXX	.XXXX	ANGLES
DRAWN	PVM	98	06	26		±	±	±	±
CHECKED					CONFIDENTIAL - NOT FOR PUBLICATION THIS IS A CONFIDENTIAL DOCUMENT, AND IN ACCEPTING IT, THE RECIPIENT ACKNOWLEDGES THAT IT IS PROVIDED UNDER THE DISTINCT CONDITION THAT IT IS FOR HIS CONFIDENTIAL USE ONLY, AND THAT HE SHALL NOT ALLOW IT TO BE REPRODUCED OR ITS CONTENTS DISCLOSED IN ANY MANNER WHATSOEVER IN WHOLE OR IN PART WITHOUT SPECIAL PERMISSION IN WRITING FROM MPR Teltech Ltd.				
ENGINEER	AS								
ENGINEER					PACIFIC DESIGN ENGINEERING LTD.				
CHECKED									
APPROVED					EQUAD/TQUAD ASSEMBLY DRAWING				
APPROVED									
NEXT ASSEMBLY DWG.					DWG. No. PM4344				SIZE B
					SCALE NTS	SHEET 1 OF 2			

7 8 9 10 11 12 13 14 15 16 17

C D E F G H J K L



CONTROLLED IMPEDANCE

ALL HOLES SHALL HAVE 0.001 IN. MINIMUM COPPER WALL THICKNESS.

5. MAXIMUM WARP AND TWIST OF FINISHED PCB SHALL NOT EXCEED 0.010 IN./IN. PER IPC-D-300.
6. FOR DILECTRIC THICKNESS SEE DETAIL B. DILECTRIC CONSTANT IS 4.5 +/- 10%.
7. SOLDER MASK IS TO BE LIQUID PHOTO IMAGEABLE.
8. MARKING MASTER TO BE SCREENED IN NONCONDUCTIVE WHITE BASED INK.
9. COPPER THICKNESS SHALL BE 1 OZ. ON ALL LAYERS.
10. ARTWORK MASTERS ARE:.

	DESCRIPTION	ISS.	ISS.	ISS.
C1	COMPONENT SIDE (LAYER 1)	1		
C2	GROUND PLANE (LAYER 2)	1		
C3	VCC PLANE (LAYER 3)	1		
C4	SOLDER SIDE (LAYER 4)	1		
MC	MARKING MASTER (COMP. SIDE)	1		
MS	MARKING MASTER (SOLDER SIDE)	1		
RC	SOLDER RESIST (COMP. SIDE)	1		
RS	SOLDER RESIST (SOLDER SIDE)	1		
DT	DRILL TAPE/DISK	1		

ONENT SIDE

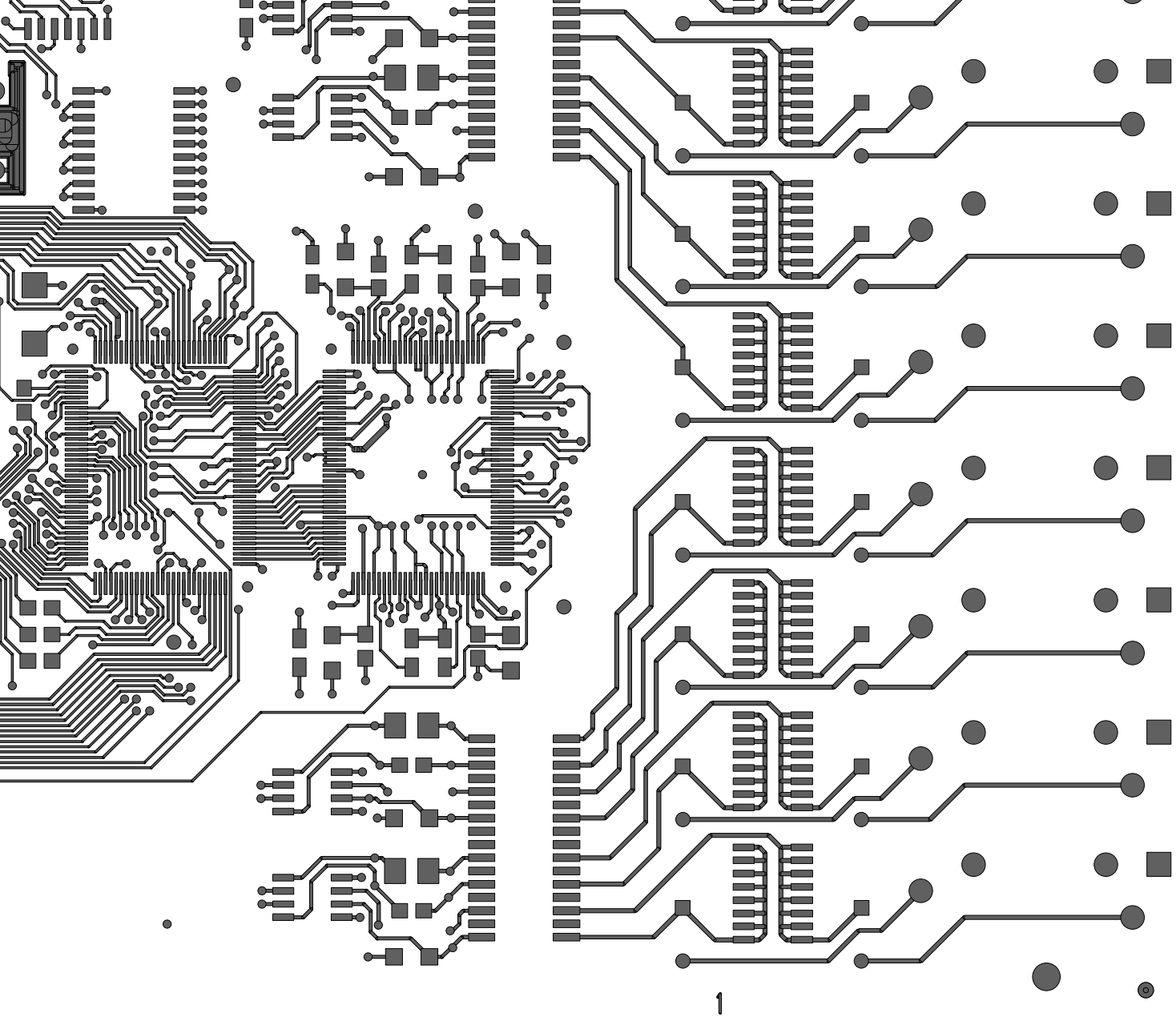
BOARD's DRILL SCHEDULE

TOOL	DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
T1	+	.016	528	YES	+/-.003
T2	×	.036	150	YES	+/-.003
T3	✳	.042	12	YES	+/-.003
T4	⊞	.052	40	YES	+/-.003
T5	⊠	.064	4	YES	+/-.003
T6	⊠	.04	2	NO	+/-.003
T7	⊕	.11	2	NO	+/-.003
T8	⊗	.125	4	NO	+.002

	DATE Y	M	D	DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SHOWN
DRAWN MWM	98	06	26	TOLERANCE (UNLESS OTHERWISE SHOWN): .XX ±0.015 .XXX ±0.003 .XXXX ± ANGLES ±
CHECKED				CONFIDENTIAL - NOT FOR PUBLICATION. THIS IS A CONFIDENTIAL DOCUMENT, AND IN ACCEPTING IT, THE RECIPIENT ACKNOWLEDGES THAT IT IS PROVIDED UNDER THE DISTINCT CONDITION THAT IT IS FOR HIS CONFIDENTIAL USE ONLY, AND THAT HE SHALL NOT ALLOW IT TO BE REPRODUCED OR ITS CONTENTS DISCLOSED IN ANY MANNER WHATSOEVER IN WHOLE OR IN PART WITHOUT SPECIAL PERMISSION IN WRITING FROM MPR Teltech Ltd.
ENGINEER				
ENGINEER	98	06	26	PACIFIC DESIGN ENGINEERING LTD.
CHECKED				
APPROVED				EQUAD/TQUAD FABRICATION DRAWING
APPROVED				
NEXT ASSEMBLY DWG.				DWG. No. PM4344 SIZE B
				SCALE NTS SHEET 1 OF 1

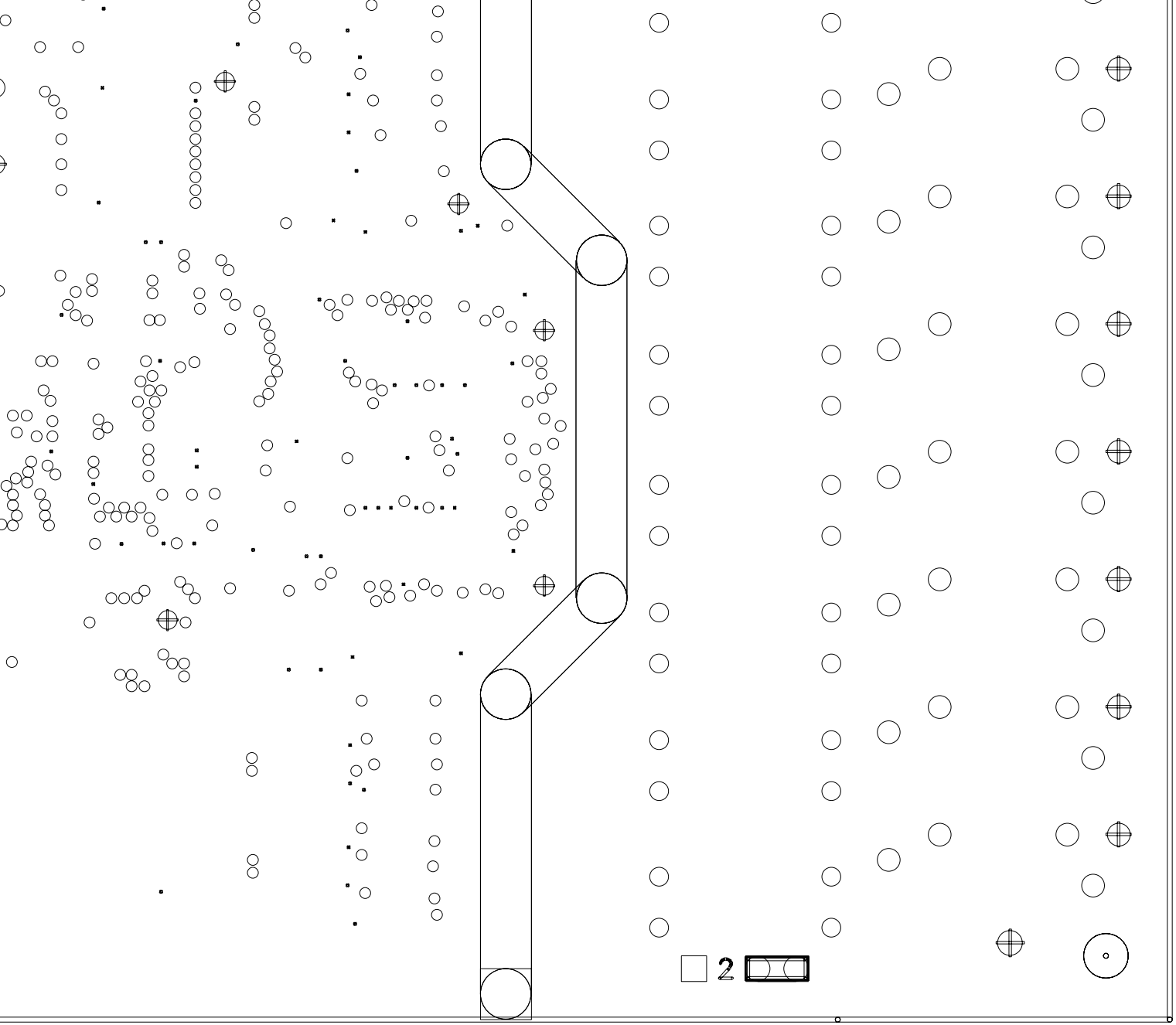
7 8 9 10 11 12 13 14 15 16 17

C D E F G H J K L



ITH QDSX REFERENCE

1 98-08-20



ITH QDSX REFERENCE
PLANE REV 1 98-08-20

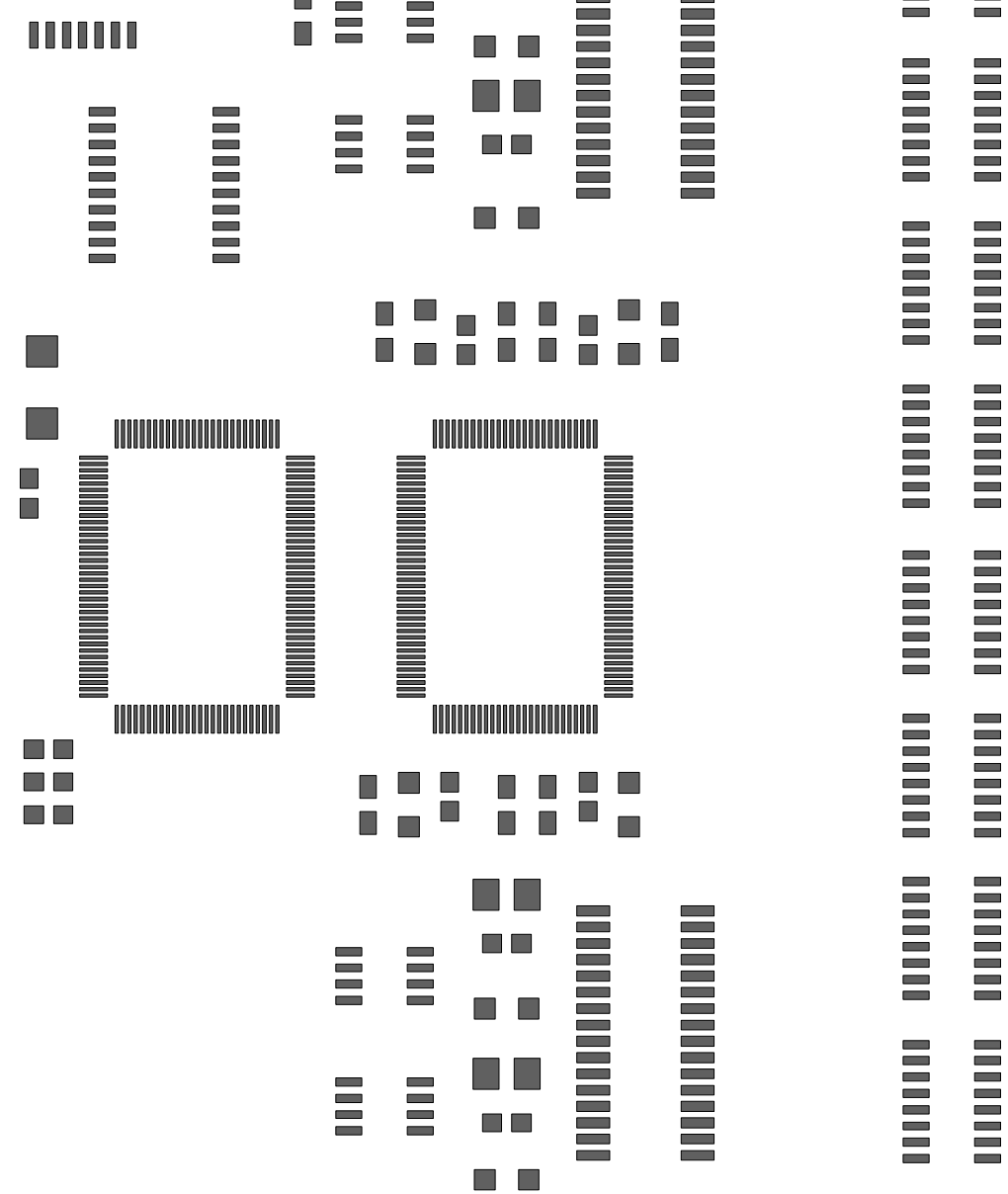
(C3) INNER LAYER VCC PLANE REV 1 98-08-20
PMC PM4344 EQUAD/TQUAD QITH QDSX REFERENC

4

PMC PM4344 EQUAD/TQUAD WITH QDSX REFERENC

(C4) SOLDER SIDE REV 1 98-08-20

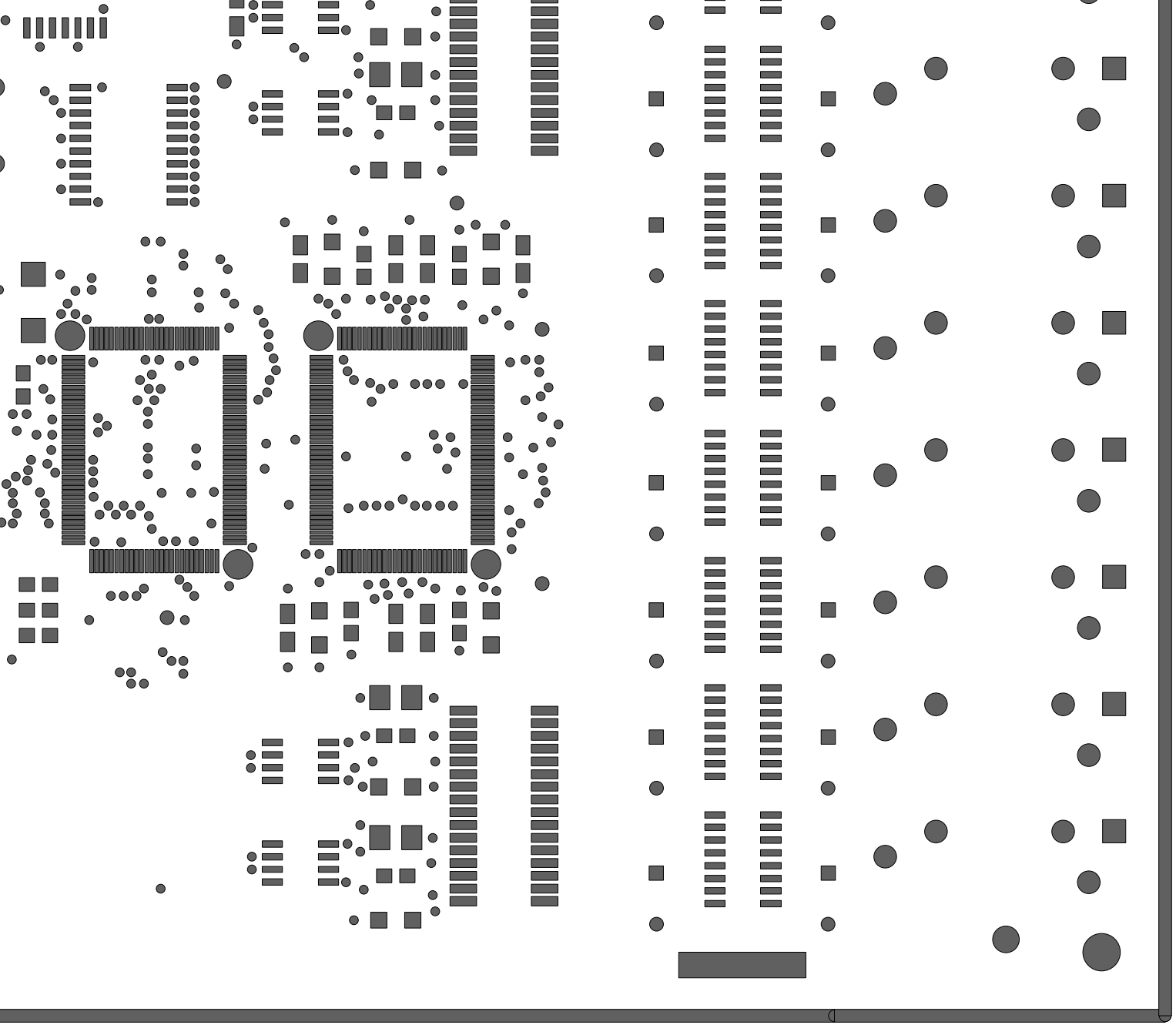
(PS) PASTE MASK (SOLDER SIDE) REV 1 98-0
PMC PM4344 EQUAD/TQUAD WITH QDSX REFERENC



ITH QDSX REFERENCE

NT SIDE) REV 1 98-08-20

PMC PM4344 EQUAD/TQUAD WITH QDSX REFERENC
(RS) SOLDERMASK SOLDER SIDE REV 1 98-08-

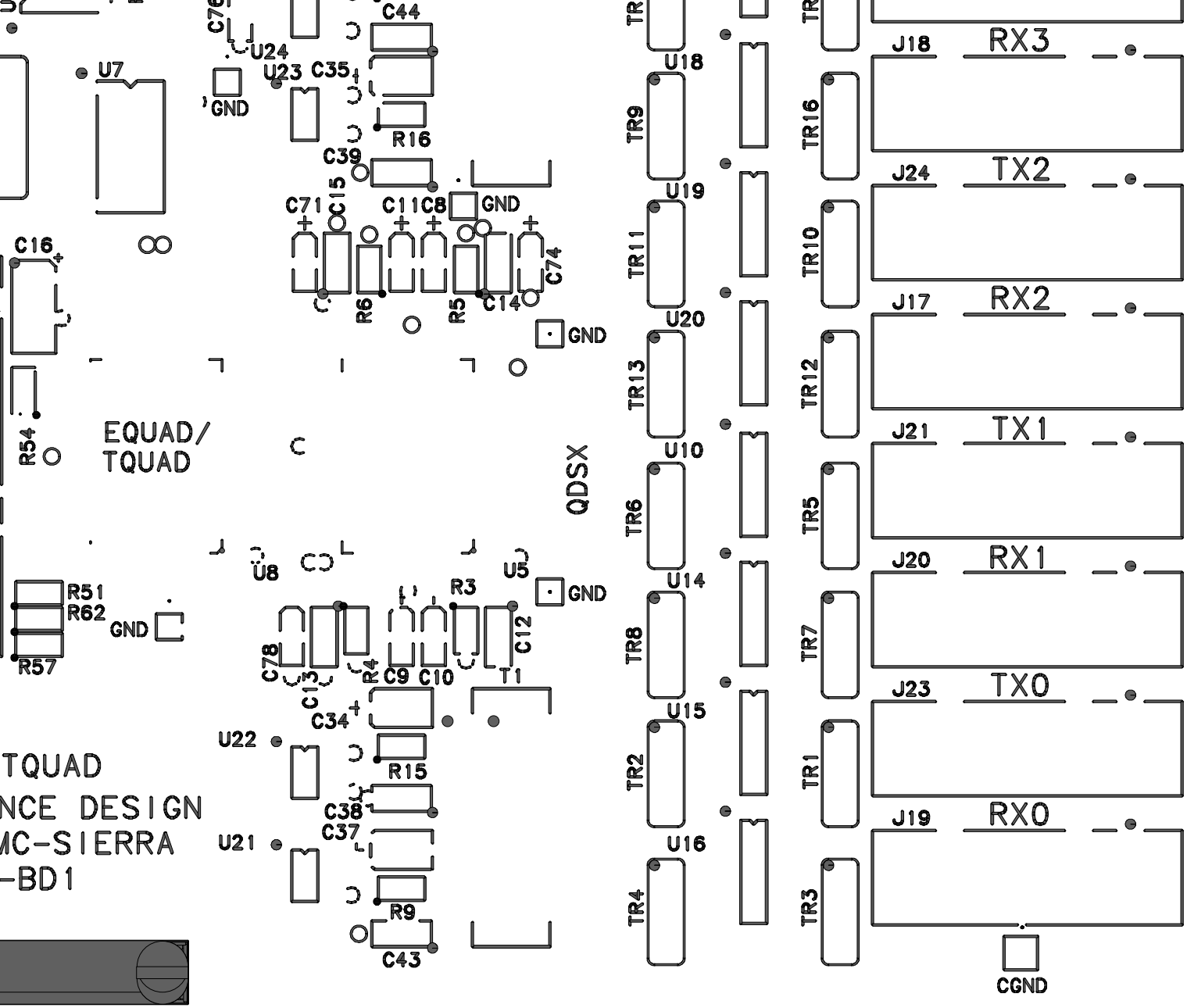


ITH QDSX REFERENCE

T SIDE REV 1 98-08-20

ITH QDSX REFERENCE

DER SIDE) REV 1 98-08-20



TQUAD
NCE DESIGN
MC-SIERRA
-BD1

ITH QDSX REFERENCE
PONENT SIDE) REV 1 98-08-20

APPENDIX D: VHDL CODE

APPENDIX E: LAYOUT ERROR

NOTE:

The footprint for parts U10, U14-20 (SEMTECH LC01-6) are too narrow on the PCB. These parts are used for line protection again power surges, and were omitting on the boards built for this reference design.

PMC-980328 (R1) ref PMC-951013 (R5) Issue date: October 1998

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PMC-980328 (R1) ref PMC-951013 (R5) Issue date: October 1998