# PM6388
# EOCTL

# TECHNICAL OVERVIEW

**November, 1997 Issue 1**

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# OVERVIEW

The PM6388 EOCTL is a feature-rich octal E1 framer ideal for data communication equipment requiring high density E1 line interfaces. This document provides an overview of the EOCTL. A complete description of this device is contained in PMC-971007, *Octal E1 Framer Datasheet*.

The EOCTL integrates eight E1 framers in a single device to terminate eight duplex E1 signals. Each of the eight E1 framers can be independently configured, monitored and controlled in software. Device drivers written for E1XC and EQUAD can be easily ported to work with EOCTL. The EOCTL is PMC-Sierra's third generation E1 framer following the successful leads of PM6341 E1XC and PM6344 EQUAD.

The EOCTL is implemented using low power 3.3V CMOS technology to minimize power consumption. It has 5V tolerant inputs to interface with 5V devices. To allow for a dramatic increase in board level density, the EOCTL is packaged in a 128 pin PQFP with a physical dimension of 14 mm by 20mm.

A simplified EOCTL block diagram is shown in Figure 1. On the line side, the EOCTL provides jitter attenuation in both the receive and transmit directions. Each framer can be configured to process the data streams in G.704 Basic, CRC-4 Multiframe, or in bypass format. V5 interfaces are fully supported with three HDLC controllers integrated in each of the eight E1 framers. On the system side, the EOCTL supports several timing modes to seamlessly interface to an HDLC controller or different types of system backplanes such as PCM, MVIP or Mitel ST®.

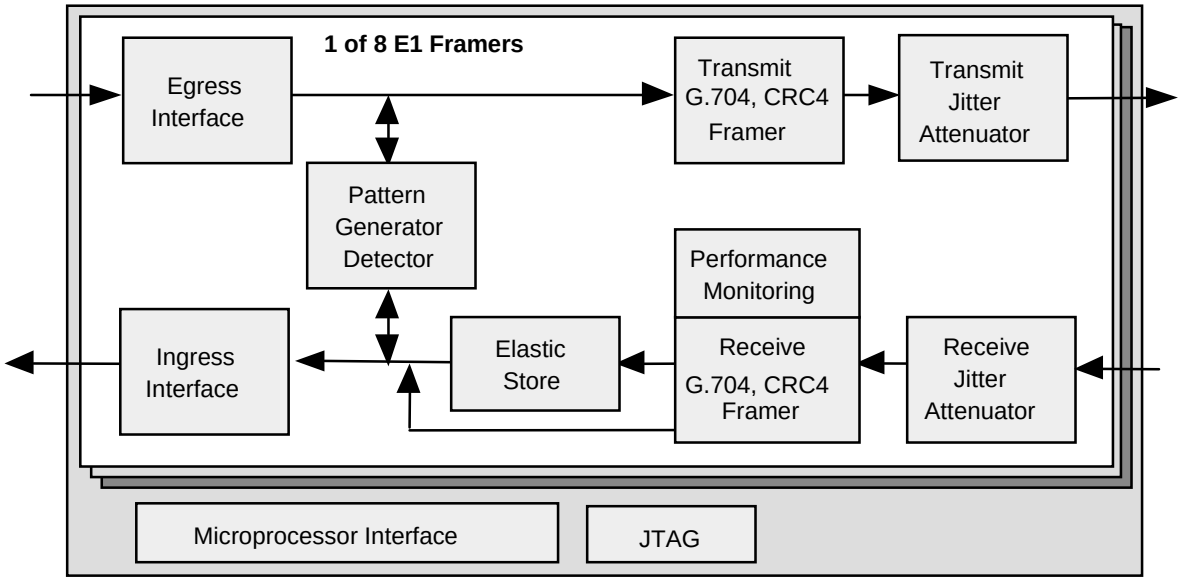


Figure 1. A simplified EOCTL Block Diagram

# FEATURES

- Integrates eight E1 framers in a single device for terminating duplex E1 signals.
- Supports transfer of PCM data to/from 2.048 MHz system-side devices. Also supports a fractional E1 system interface with independent ingress/egress fractional E1 rates.
- Provides an optional backplane interface which is compatible with Mitel ST®-bus and MVIP PCM backplanes, supporting data rates of 2.048 Mbit/s, 4.096 Mbit/s, and 8.192 Mbit/s. Up to four links may be byte interleaved on each interface bus with no external circuitry.
- Extracts/inserts up to three HDLC links from/to arbitrary time slots to support the D-channel for ISDN Primary Rate Interfaces and the C-channels for V5.1/V5.2 interfaces as per ITU-T G.964, ITU-T G.965, ETS 300-324-1, and ETS 300-347-1.
- Processes ETS 300-233 four-bit codewords in the E1 National Use bits.
- Provides jitter attenuation in the receive and transmit directions.
- Provides per-channel line loopback and per link diagnostic and line loopbacks.
- Provides an integral pattern generator/detector that may be programmed to generate and detect common pseudo-random (as recommended in ITU-T O.151) or repetitive sequences. The programmed sequence may be inserted/detected in the entire E1 frame, or on a fractional E1 basis, in both the ingress and egress directions. Each framer possesses its own independent pattern generator/detector, and each detector counts pattern errors using a 32-bit saturating error counter.
- Provides signaling extraction and insertion on a per-channel basis.
- Software compatible with the PM6341 E1XC Single E1 Transceiver, the PM6344 EQUAD Quad E1 Framer, the PM4388 TOCTL Octal T1 Framer, and PM4351 COMET Combined E1/T1 Transceiver.
- Seamless interface to the PM4314 QDSX Quad Line Interface.
- Provides an IEEE P1149.1 (JTAG) compliant test access port (TAP) and controller for boundary scan test.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 3.3V CMOS technology with 5V tolerant inputs.
- Available in a 128 pin PQFP (14 mm by 20 mm) package.
- Provides a -40°C to +85°C Industrial temperature operating range.

Each one of the eight receiver sections

- Frames to ITU-T G.704 basic and CRC-4 multiframe formatted E1 signals. The framing procedures are consistent with ITU-T G.706, ETS TBR 4, ETS TBR 12 and ETS TBR13 specifications.
- Provides AIS detection as per ITU-T G.775.
- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Optionally, updates the performance monitoring counters

and interrupts the microprocessor once per second, timed to the receive line. Accumulators are provided for counting CRC errors, FEBE events, and framing bit errors events.

- Provides an optional elastic store for backplane rate adaptation. It may be used to time the ingress streams to a common clock and frame alignment, or to facilitate per-channel loopbacks.
- Provides a digital phase locked loop to reduce jitter on the receive clock.
- Supports polled or interrupt-driven servicing of the HDLC interface.
- Optionally extracts a datalink in the E1 national use bits.
- Extracts four-bit codewords from E1 National Use bits to ETS 300-233.
- Extracts up to three HDLC links from arbitrary time slots to support the D-channel for ISDN Primary Rate Interfaces and the C-channels for V5.1/V5.2 interfaces.
- Frames to the E1 signaling multiframe alignment when enabled and extracts channel associated signaling. Alternatively, a common channel signaling data link may be extracted from timeslot 16.
- Can be programmed to generate an interrupt on change of signaling state.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Provides per link diagnostic loopback and line loopback and per-channel line loopback.
- Provides programmable idle code substitution, data inversion, and A-Law or μ-Law digital milliwatt code insertion on a per-channel basis.
- Optionally outputs N*DS0 formatted backplane.
- Optionally outputs Mitel ST®-bus and MVIP formatted backplanes

Each one of the eight transmitter sections

- Transmits G.704 basic and CRC-4 multiframe formatted E1 signals.
- Supports unframed mode and framing bit, CRC, or data link by-pass.
- May be timed to its associated receive clock (loop timing) or may derive its timing from a common egress clock or a common transmit clock; the transmit line clock may be synthesized from an N*8kHz reference.
- Provides a 128 byte buffer to allow insertion of the facility data link using the host interface.
- Optionally inserts a datalink in the E1 national use bits.
- Inserts four-bit codewords on the E1 National Use bits to ETS 300-233.
- Inserts up to three HDLC links into arbitrary time slots to support the D-channel for ISDN Primary Rate Interfaces and the C-channels for V5.1/V5.2 interfaces.
- Provides a digital phase locked loop for generation of a low jitter transmit clock.
- Provides programmable idle code substitution, data inversion, signaling insertion, and A-Law or μ-Law digital milliwatt code insertion on a per-channel basis.

- Accepts N*DS0 formatted backplane.
- Accepts Mitel ST®-bus and MVIP formatted backplanes

# APPLICATION EXAMPLES

The EOCTL is ideal for Access Equipment aggregating large numbers of E1 lines. On the line side, it can interface to E1 line interface units (LIUs) or 16 E1s can be multiplexed/demultiplexed onto a E3 facility using an E13 scheme as shown in Figure 2. Access product manufacturers will be able to use the EOCTL to achieve greater than 50% savings in board space and greater than 50% reduction in power while improving product reliability over less integrated solutions.

On the system side, the EOCTL can interface directly to a high density HDLC controller to terminate data encapsulated in HDLC protocol. The EOCTL supports transfer of PCM data to and from 2.048 Mbit/s backplane buses and supports fractional E1 backplane interface with asymmetric transmit/receive NxTS (NxTimeSlot) rates.

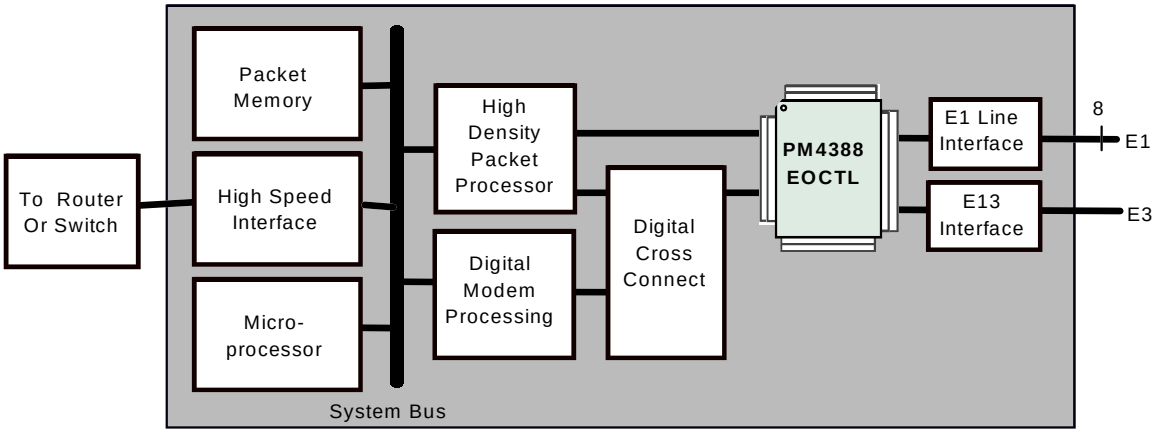


Figure 2: EOCTL in a Typical Access Equipment Architecture.

The EOCTL can seamlessly interface to two PM4314 QDSX to support eight E1 links as shown in Figure 3. The QDSX integrates four full-featured T1/E1 duplex DSX-1 compatible line interface circuits in a single device. The QDSX is currently in production and is packaged in a 128 PQFP. A complete information on the QDSX is contained in PMC-950847, *QUAD T1/E1 Line Interface Device Telecom Standard Product Datasheet.*

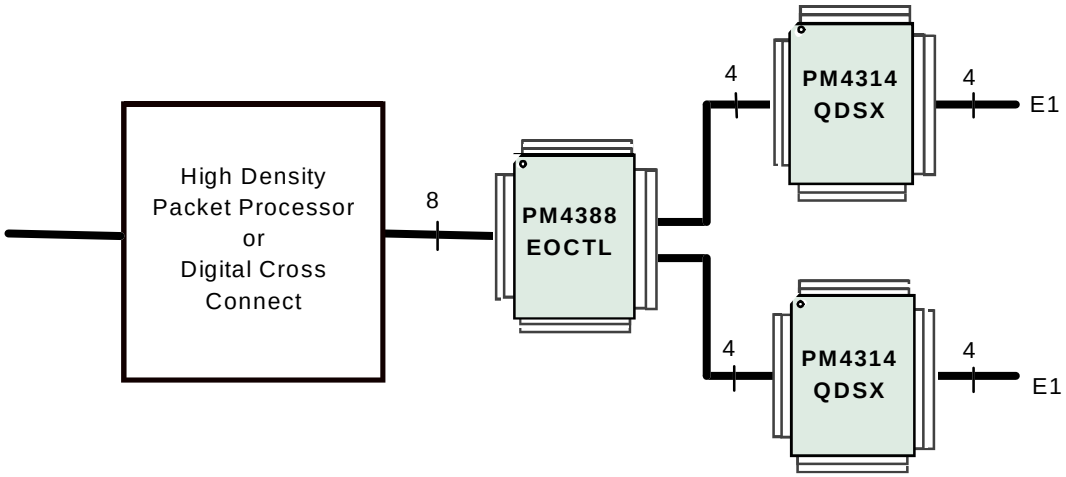


Figure 3: 8 Channel E1 Interface for Frame Relay or Internet Access Equipment.

Two EOCTLs can be used with four PM4314 QDSXs to implement a V5.2 interface as shown in Figure 4. The EOCTL's three HDLC controllers per channel (24 per device) allow full compliance to both V5.1 and V5.2 interfaces. Housekeeping, signaling and control protocols carried in the control channels of the V5.2 interface and can be processed to dynamically allocate a physical user port to any of the timeslots within the 16 span V5.2 interface. The V5 interface specifications can be found in ETSI 300-324 and ETSI 300-347. ITU has also standardized on these interfaces which can be found in ITU G.964 and ITU G.965.

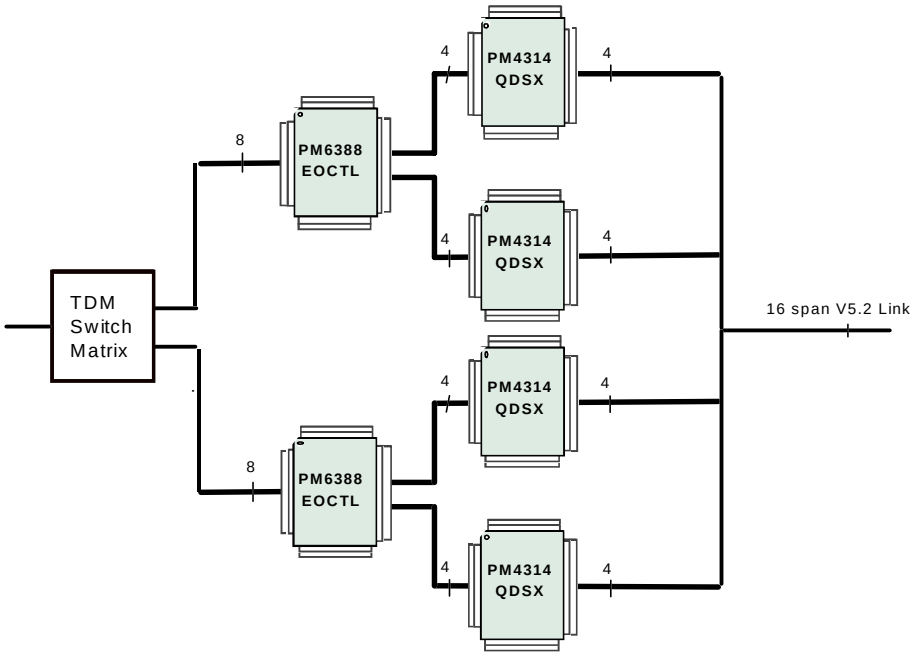

Figure 4: V5.2 Interface using two EOCTLs and 4 QDSXs.

# FUNCTIONAL DESCRIPTION

## Transmit and Receive Jitter Attenuators

Each framer in the EOCTL contains two separate jitter attenuators: one between the receive line data and the ingress interface and the other between the egress interface and the transmit line data. Each digital jitter attenuator provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. These jitter attenuators meet the transfer requirements of TBR4, TBR12, TBR13 and ETSI 300-011 specifications.

## Transmit and Receive Framers

In the receive direction, the EOCTL examines the incoming data to establish synchronization with the selected framing format. If enabled, signaling is extracted from the appropriate channels and can be provided via a serial stream on the *ingress signaling* (ISIG[x]) pin or via software access by the external microprocessor. The EOCTL provides user control over signaling freezing, signaling bit fixing and signaling debounce on a per-channel basis.

The EOCTL indicates the presence or absence of the OOF and AIS alarm conditions. They are integrated in accordance with the consequent action requirements of I.431. The alarm is removed when the condition has been absent for 104 ms (±6 ms). An external microprocessor can integrate the alarm conditions using any system specific algorithm.

In the transmit direction, the EOCTL inserts frame generation, CRC multiframe generation, channel associated signaling (CAS) multiframe generation, and datalink information into the 2.048 Mbit/s stream. Frame insertion may optionally be bypassed. The framer provides per-channel control over idle code substitution, data inversion, digital milliwatt substitution, selection of the signaling source and CAS data

The EOCTL supports the per-channel insertion and detection of pseudo-random or repetitive patterns. The EOCTL provides three loopback modes to assist in network and system diagnostics:

- line loopback,
- diagnostic digital loopback,
- per-channel loopback.

## Non-Multiplexed Ingress Interface

The EOCTL's ingress interface allows the received line data to be presented to the system using one of four possible modes:

- Clock Master: Full E1
- Clock Master : NxTS (NxTimeSlot)
- Clock Slave: ICLK Reference
- Clock Slave: External Signaling

**1) Clock Master: Full E1**

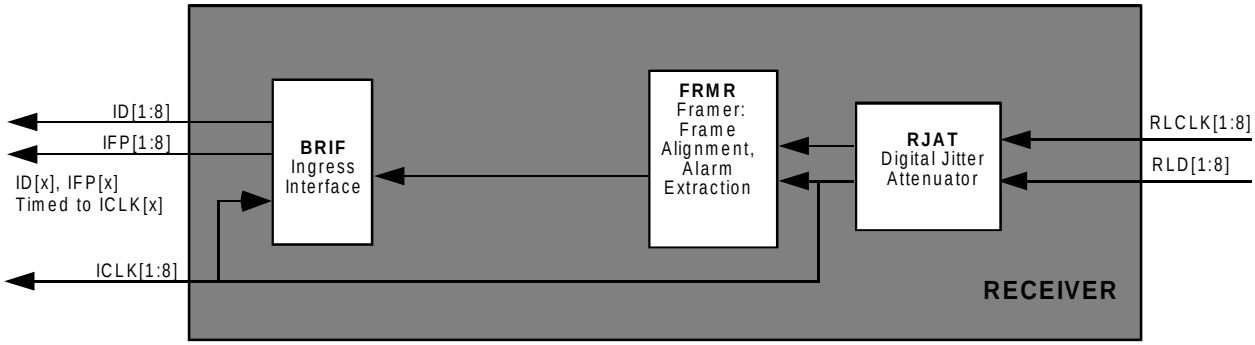


Figure 5: Ingress Clock Master: Full E1 Mode.

In *Clock Master: Full E1* mode, each recovered E1 *receive line data* (RLD[x]) is passed through the receive jitter attenuator and the receive framer using the *receive line clock* (RLCLK[x]). Minimal transmission delay is incurred on the data stream as the elastic store is bypassed.

The received data appears on *ingress data* (ID[x]) timed to the *ingress clock* (ICLK[x]). ICLK[x] is a jitter attenuated version of the RLCLK[x]. The ingress frame alignment is indicated by the *ingress frame pulse* (IFP[x]) signal. When the EOCTL is the clock master in the ingress direction, then the elastic store is used to buffer between the ingress and egress clocks to facilitate per-channel loopback.

**2) Clock Master: NxTS**

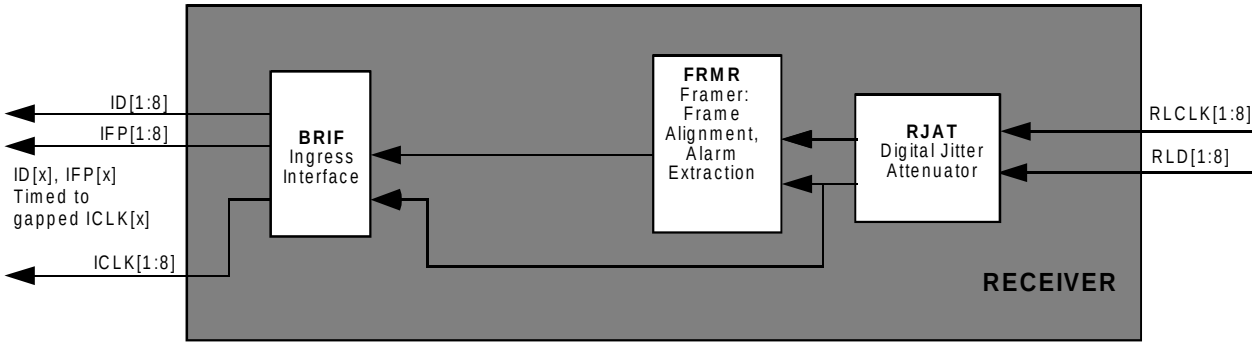


Figure 6: Ingress Clock Master: NxTS mode.

In *Clock Master: NxTS* mode, ICLK[x] is derived from RLCLK[x], and is gapped on a per channel (per TimeSlot) basis so that a subset of the 32 channels in the E1 frame is extracted on ID[x]. Channel extraction is controlled by the RPSC block. The number of ICLK[x] pulses is controllable from 0 to 256 pulses per frame on a per-channel basis.

In this mode, data passes through the EOCTL unchanged during out-of-frame conditions. The parity functions are not usable in NxTS mode. When the EOCTL is the clock master in the ingress direction, then the elastic store is used to buffer between the ingress and egress clocks to facilitate per-channel loopback.

**3) Clock Slave: ICLK Reference**

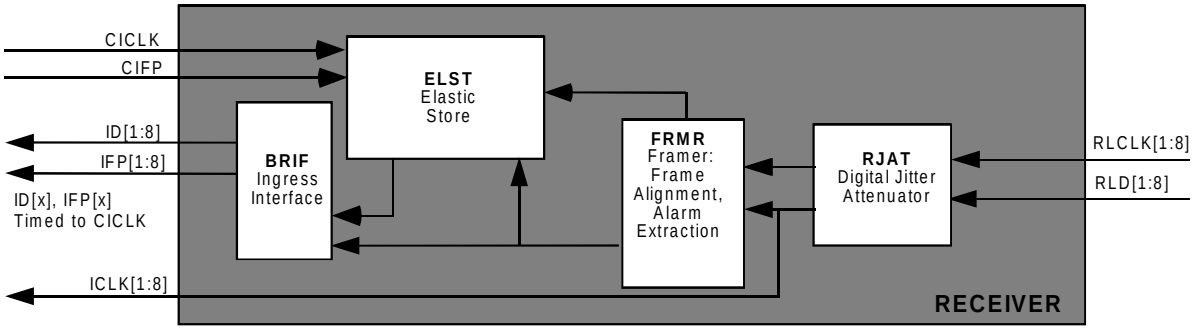


Figure 7: Ingress Clock Slave: ICLK Reference mode.

In the *Clock Slave: ICLK Reference* mode, the elastic store is enabled to permit CICLK to specify the ingress-side timing. The ingress data on ID[x] is bit aligned to the 2.048 MHz common ingress clock (CICLK) and is frame aligned to the common ingress frame pulse (CIFP). ICLK[x] can be enabled to be either a 2.048 MHz jitter attenuated version of RLCLK[x] or an 8 kHz version of RLCLK[x] (by dividing RLCLK[x] by 256). IFP[x] indicates either the frame, signaling multiframe, CRC multiframe, or both signaling and CRC multiframe alignment of ID[x].

**4) Clock Slave: External Signaling.**

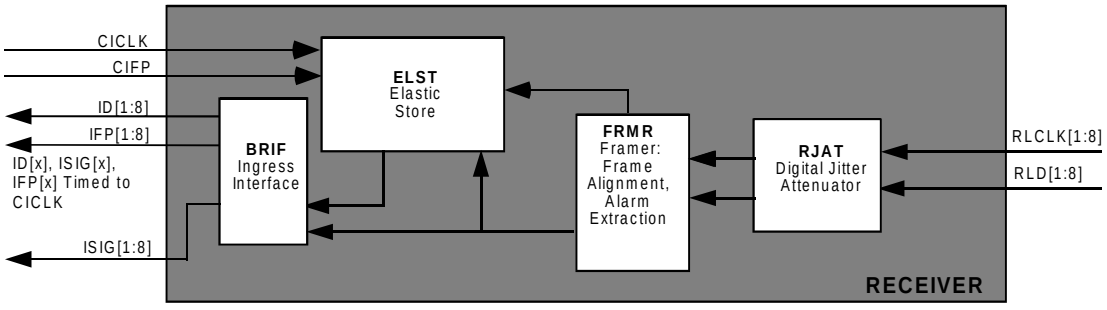


Figure 8: Ingress Clock Slave: External Signaling Mode.

In the *Clock Slave: External Signaling* mode, the elastic store is enabled to permit CICLK to specify the ingress-side timing. The ingress data on ID[x] and signaling ISIG[x] are bit aligned to the 2.048 MHz common ingress clock (CICLK) and are frame aligned to the common ingress frame pulse CIFP. ISIG[x] contains the TS16 common channel signaling states (ABCD) in the lower four bits of each channel.

Note that the ICLK[x] pins, used in *Clock Slave: ICLK Reference* mode, are the same pins used for ISIG[x].

## Multiplexed Ingress Interface

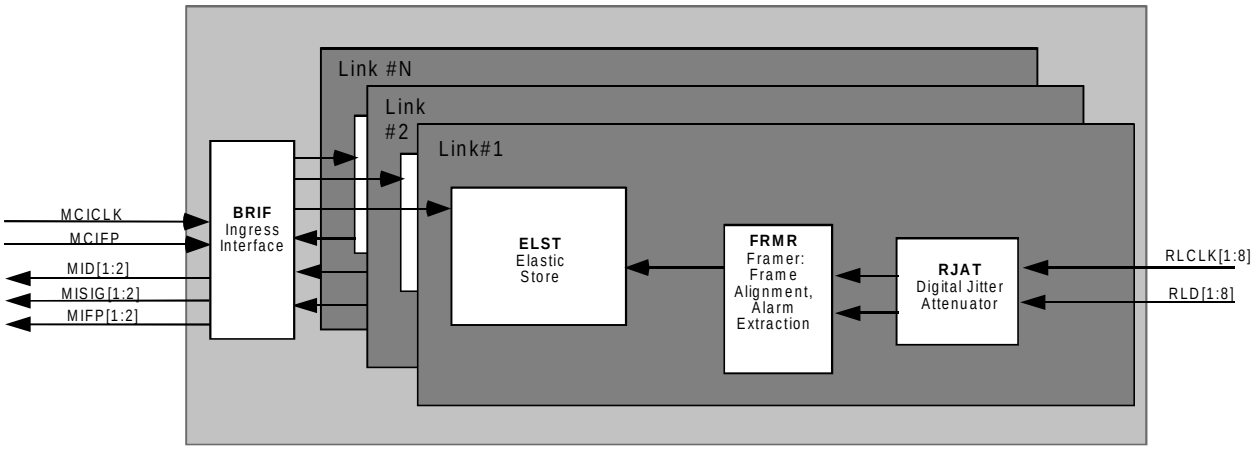


Figure 9: Multiplexed Ingress Interface

When the Multiplexed bus structure is enabled on the ingress side, the Backplane Receive Interface allows byte-interleaved data to be presented to a backplane on one of two 2.048Mbit/s, 4.096Mbit/s, or 8.192Mbit/ serial streams.

All receive backplane signals are synchronous to CICLK. When configured for a multiplexed backplane, the data and signaling streams for each selected link are byte interleaved into the 2.048 Mbit/s, 4.096 Mbit/s or 8.192 Mbit/s serial streams MID[1:2] and MISIG[1:2] respectively. Frame alignment for each selected link is given on MIFP[1:2]. As a programming option, the data stream bit and timeslot alignment relative to MIFP[1:2] can be modified for Concentration Highway Interface (CHI) applications.

## Non-Multiplexed Egress Interface

The EOCTL's egress interface allows data to be inserted into the transmit line using one of four possible modes:

- Clock Master: Full E1
- Clock Master: NxTS (NxTimeSlot)
- Clock Slave: EFP Enabled
- Clock Slave: External Signaling

**1) Clock Master: Full E1**

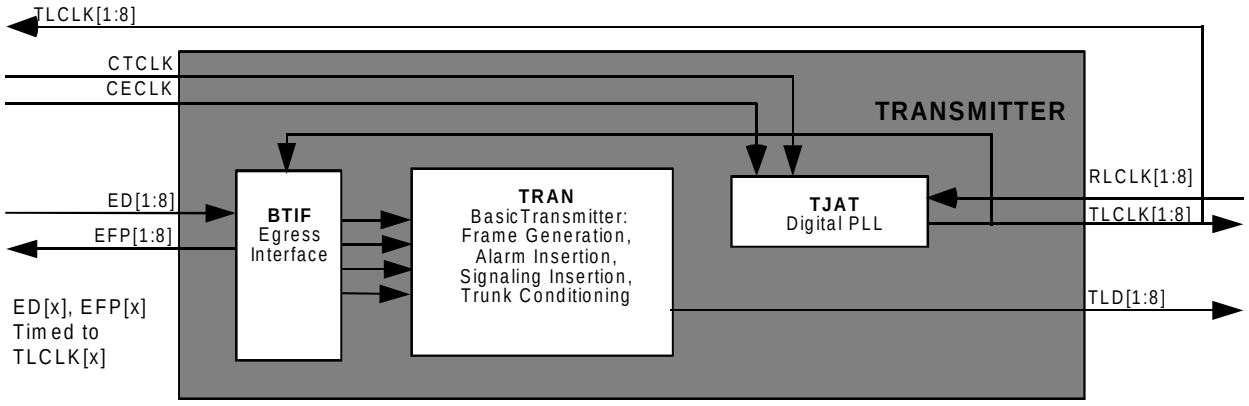


Figure 10: Egress Clock Master: Full E1 Mode.

In the *Clock Master: Full E1* mode, the transmit clock output (TLCLK[x]) "pulls" data from an upstream data source. The frame alignment is indicated to the upstream data source using EFP[x]. TLCLK[x] may be generated by the TJAT PLL, referenced to CECLK, CTCLK, or RLCLK[x]. TLCLK[x] may also be derived directly from CTCLK or XCLK. The CEFP input is unused in this mode, and has no effect.

**2) Clock Master: NxTS**

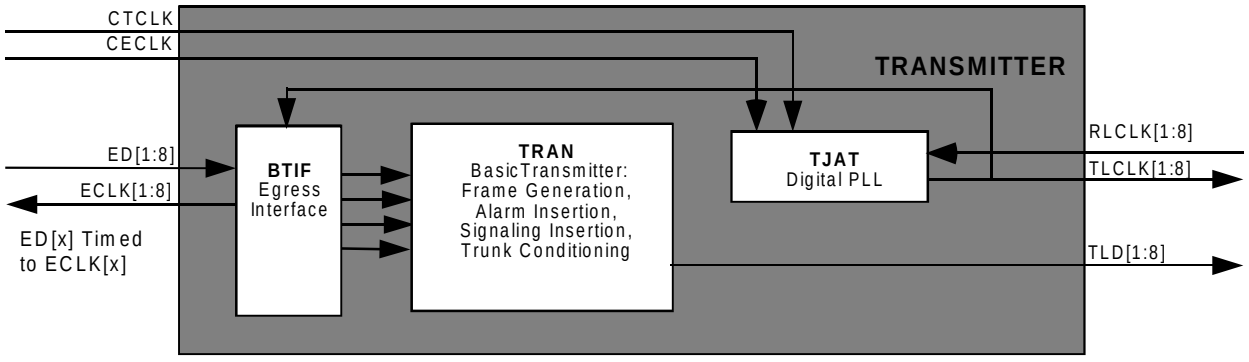


Figure 11: Egress Clock Master: NxTS Mode.

The *Clock Master: NxTS* mode is identical to the full E1 mode except that the frame alignment is not indicated to the upstream device. Instead, ECLK[x] is gapped on a per channel basis so that a subset of the 32 channels in the E1 frame is inserted on ED[x]. Channel insertion is controlled by the IDLE_TS bits in the

TPSC block's Egress Control Bytes. The number of ECLK[x] pulses is controllable from 0 to 256 pulses per frame on a per-channel basis. The parity functions should not be enabled in NxTS mode. The CEFP input is unused in this mode, and has no effect.

**3) Clock Slave: EFP Enabled.**

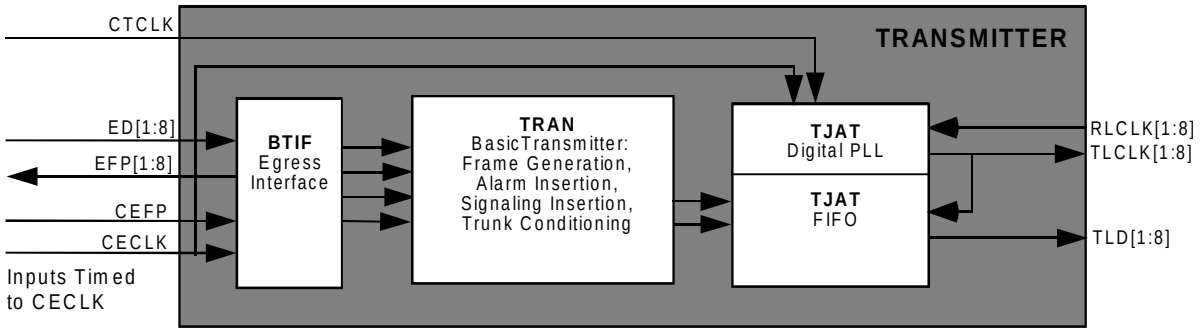


Figure 12: Egress Clock Slave: EFP Enabled Mode

In the *Clock Slave: EFP Enabled* mode, the egress interface is clocked by the common egress clock (CECLK). The transmitter is either frame-aligned or Signaling and CRC multiframe-aligned to the common egress frame pulse (CEFP). EFP[x] is configurable to indicate the basic frame alignment or the Signaling and CRC multiframe alignment of ED[x].

**4) Clock Slave: External Signaling.**

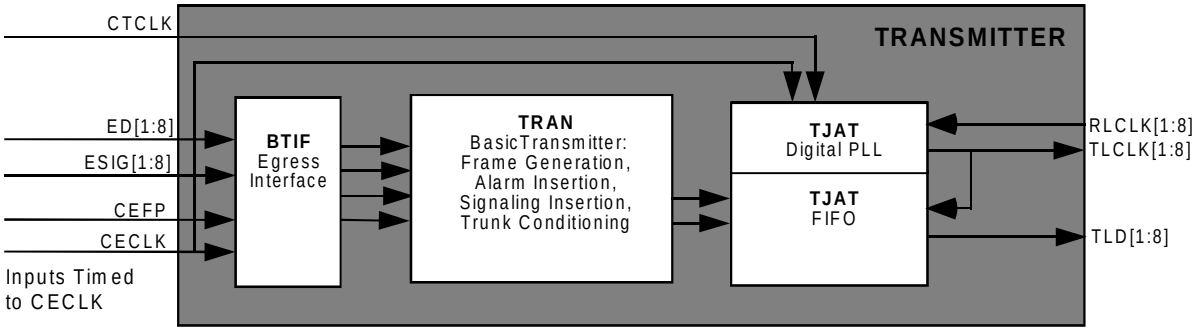


Figure 13: Egress Clock Slave: External Signaling Mode.

In the *Clock Slave: External Signaling* mode the egress interface is clocked by the common egress clock (CECLK). The transmitter is either frame-aligned or Signaling and CRC Multiframe-aligned to the common egress frame pulse (CEFP). The ESIG[x] contain the robbed-bit signaling data to be inserted into TLD[x], with the four least significant bits of each channel on ESIG[x] representing the TS16 common channel signaling state (ABCD). EFP[x] is not available in this mode.

## Multiplexed Egress Interface

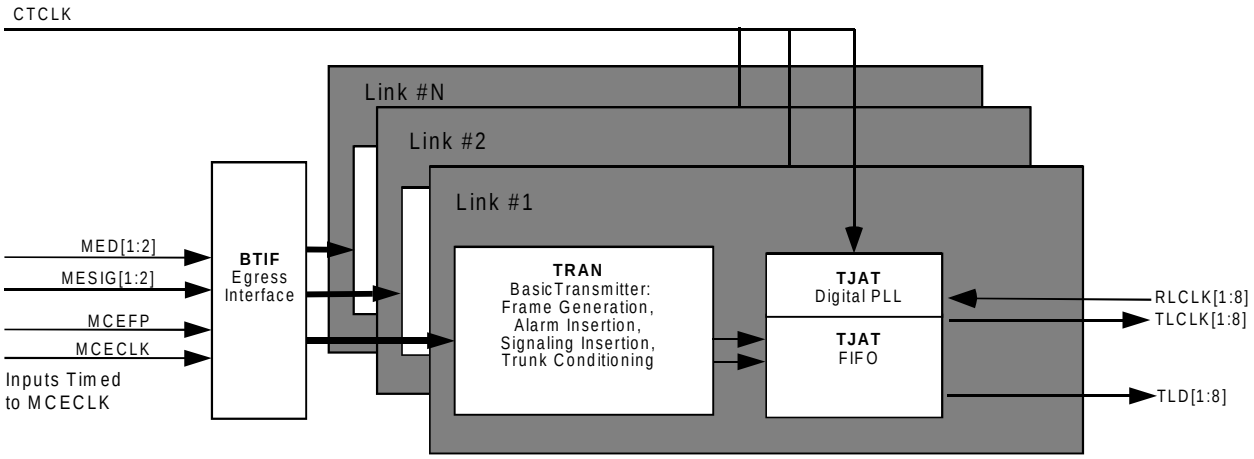


Figure 14: Multiplexed Egress Interface

When the Multiplexed bus structure is enabled on the egress side, the Backplane Transmit Interface allows byte-interleaved data to be taken from timeslots of one of two multiplexed bus structures of 2.048 Mbit/s, 4.096 Mbit/s, or 8.192 Mbit/s. Each stream allows up to 4 links to be transmitted.

All transmit backplane signals are synchronous to MCECLK. When configured for a multiplexed backplane, the data and signaling streams can be configured to be routed to any one of the 8 egress links. Data is taken from the MED[1:2] stream. Signaling is taken from the MESIG[1:2] stream. Timeslot alignment on the bus is taken from the MCEFP signal.

## Performance Monitoring

The Performance Monitor Counters function is provided by the PMON block. The block accumulates CRC error events, Frame Synchronization bit error events, and FEBE events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second). When the transfer clock signal is applied, the PMON transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If the holding registers are not read between successive transfer clocks, an OVERRUN register bit is asserted.

## V5 Interface Subchannel Processing

Use of up to three timeslots per E1 channel for carrying performance information and control signals across the network interface is specified in ETSI 300-324 for V5.1 interfaces and ETSI 300-347 for V5.2 interfaces. These timeslots can carry message-oriented signals using a V5 envelope protocol is similar to the LAPD protocol shown in figure 15.

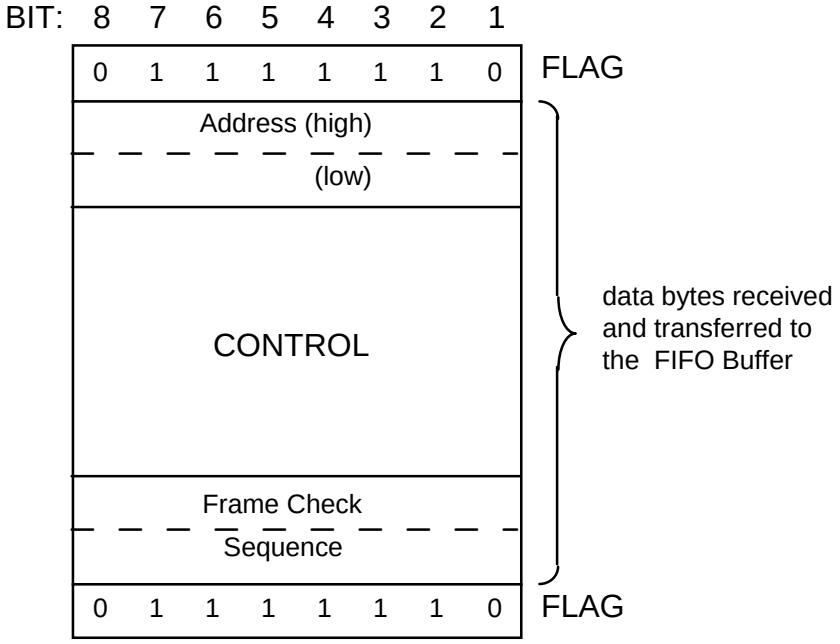


Figure 15: Message-Oriented Frame Structure.

The EOCTL is able to receive and transmit message-oriented data carried in three timeslots for each of the E1 channels, for a total of 24 timeslots. While the EOCTL has the ability to process HDLC data in any timeslot from TS0 to TS31 in these E1 channels, the ETSI and ITU V5 specifications stipulate timeslots TS15, TS16 and TS31 for allocation of V5 control traffic. In the transmit direction, the message report to be transmitted is written into the *Transmit Data* register by a microprocessor. The EOCTL transmits the message, performs zero-bit stuffing and generates the CRC-CCITT *frame check sequence* (FCS). Zero stuffing by the transmitter

prevents the occurrence of the flag pattern (01111110) in the bits between the opening and closing flags of a frame. This is accomplished by inserting a zero after any sequence of five consecutive ones.

In the receive direction, the EOCTL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data and validates the FCS. Received message is placed into a 128 byte FIFO buffer to be accessed by the microprocessor.

## Pattern Generator/Detector (PRBS)

Advanced access products require the ability to support E1 diagnostic testing. In typical E1 framers, this function is implemented using external *pseudo random binary sequence* (PRBS) devices. The EOCTL provides a 32-bit fully programmable PRBS generator and detector for each E1 framer. The PRBS function enables a service provider to conduct line testing and verification during service installation and enables ongoing line quality monitoring. It also permits the generation and detection of fractional E1 loopback codes.

To test the reliability of a digital communication link, a specific test pattern is generated at the source, carried through the network, and compared at the destination. The *bit error ratio* (BER) can be measured at the destination by comparing the received data with the expected test patterns.

In EOCTL, each one of the eight framers has a built in *pattern generator/detector* (PRGD) block. The PRGD block is capable of generating and detecting pseudo-random and repetitive patterns including those defined in ITU-T O.151. At the source, one or more channels in an E1 link can be configured to carry the test patterns. If multiple channels are selected, as in the case of a fractional E1 or a full E1, they are collectively treated as a single data stream and BER testing is conducted on the aggregate data stream. If a subset of the E1 link is selected for error monitoring, the remaining channel timeslots can continue to carry data. Therefore, it is not necessary to take down the entire E1 link in order to perform BER testing.

PRGD can be used to test the integrity of the system backplane. To accomplish this, the received data is substituted with test patterns generated by the PRGD block. The data is looped from the *ingress data* (ID[x]) pin through the system backplane to the *egress data* (ED[x]) pin where the received data can be compared by the PRGD block against expected test patterns.

## Microprocessor Interface

The EOCTL provides a parallel microprocessor interface for controlling the operation of the EOCTL device.

## JTAG

The EOCTL supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1. The boundary scan register allows testing of board inter-connectivity by making all inputs visible and all outputs controllable via the standard 5-pin JTAG port.

# A COMPARISON OF EOCTL AND EQUAD

This is a high-level comparison between PM6388 EOCTL and PM6344 EQUAD.

## EOCTL Functions Not Available in EQUAD

This section outlines the new features added to EOCTL that are not available on the EQUAD. Specifically, the EOCTL includes the following new functions not available in EQUAD:

- 8 channel device instead of 4 (in the same 128 PQFP package).
- Improved HDLC handling with 128 byte FIFO to lower microprocessor overhead.
- Programmable PRBS generator/detector at per channel or per link rates.
- Low power 3.3V device with 5V tolerant inputs.
- JTAG boundary scan testing.
- Per-channel loopbacks to allow for circuit testing.
- Maskable interrupt generated on the detection of signaling change of state.
- Jitter attenuation in both receive and transmit directions.
- Full V5.1/V5.2 interface compatibility with three HDLC controllers per channel
- Full compatibility with MVIP and Mitel ST®-backplanes at rates up to 8.192Mbit/s. This will support byte interleaving up to the MVIP rates.

## EQUAD Functions Not Available in EOCTL

This section lists the features that are supported in the EQUAD but not in the EOCTL. Specifically, the EOCTL does not support the following features found in EQUAD:

- No dual rail NRZ data, clock recovery or HDB3/AMI line. These functions are supported by PMC's PM4314 QDSX. Dual rail I/Os are not required where E1 interfaces to an E13 multiplexer/demultiplexer.
- No DMA servicing of HDLC data.
- No bit-interleaved multiplexed backplane data stream mode.
- No 16.387 MHz crystal option for the *crystal clock input* (XCLK). Only 49.152 MHz is supported.
- No hardware access to TS16 signaling unless the receive streams are referenced to a common ingress clock AND the transmit streams are referenced to a common egress clock. TS16 signals are always accessible via software access from an external microprocessor.

# CONTACTING PMC-SIERRA

The PM6388 EOCTL package includes a data book, application notes, and a short form data sheet. Please contact PMC-Sierra for additional information:

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**NOTES:**

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